HYBRID PRODUCTS DATABOOK

NATIONAL SEMICONDUCTOR CORPORATION

ACTIVE FILTERS
A-D, D-A CONVERTERS
ANALOG SWITCHES
FIBER-OPTICS
LINEAR AMPLIFIERS
POWER DRIVERS
PRECISION REFERENCES

HYBRID PRODUCTS DATABOOK

The Hybrid Products Databook is the only National Semiconductor publication that contains complete information on all of our hybrid semiconductor products.

Included are precision thin film and thick film products which provide the user with standard functions from operational amplifiers to converters with capabilities beyond those of current monolithic technology.

Product selection guides and an application section are also included. For information on new products, contact your local National Semiconductor sales office.

Edge Index by Function

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Section 1

Operational Amplifiers

Section 1. Operational Amplifiers

Features	Input Offset Voltage Max. (mV)	Input Offset Voltage Drift Typ. (μV/°C)	Input Offset Current Max. (nA)	Input Bias Current Max. (nA)	Voltage Gain Min. (Volts/mV)	Bandwidth $A_V = 1$ Typ. (MHz)	Slew Rate $A_V = 1$ Typ. (V/μs)	Output Current (mA)	Supply Voltage Min. (V)	Supply Voltage Max. (V)	Temperature Range −55°C to 125°C	Temperature Range −25°C to 85°C	Temperature Range 0°C to 70°C	Page No.
Wideband	3.0	4.0	200	2000	15	30	30	±100	±5.0	±20	LH0003	LH0003C		1-4
High Voltage	1.0	4.0	20	100	30	1.0	0.25	±15	±5.0	±45	LH0004			1-6
	1.5	4.0	45	120		1.0	0.25	±15	±5.0	±45		LH0004C		1-6
Wideband	3.0	10	5.0	25	4.0	30(1)	20(1)	±50	±9.0	±20	LH0005A			1-9
	10	20	20	50	2.0	30(1)	20(1)	±50	±9.0	±20	LH0005			1-9
	10	25	25	100	2.0	30(1)	20(1)	±50	±9.0	±20		LH0005C		1-12
High Gain Medium Power	2.5	10	50	250	100	1.0	0.25	±40	±5.0	±22	LH0020			1-14
	6.0	10	200	500	50	1.0	0.25	±40	±5.0	±22		LH0020C		1-14
High Power	3.0	3.0	100	300	100	1.0	3.0	±1000	±5.0	±18	LH0021			1-16
	6.0	5.0	200	500	100	1.0	3.0	±1000	±5.0	±18		LH0021C		1-16
	3.0	3.0	100	300	100	1.0	3.0	±200	±5.0	±18	LH0041			1-16
	6.0	5.0	200	500	100	1.0	3.0	±200	±5.0	±18		LH0041C		1-16
	4.0	5.0	100	300	50	15	70	±500	±5.0	±18	LH0061			1-56
	10	5.0	200	500	25	15	70	±500	±5.0	±18		LH0061C		1-56
	10	10	0.25	1.0	50	5.0	10	±2000	±5.0	±22	LH0101			1-65
	10	10	0.25	1.0	50	5.0	10	±2000	±5.0	±22		LH0101C		1-65
	3.0	5.0	0.075	0.3	50	5.0	10	±2000	±5.0	±22	LH0101A			1-65
	3.0	5.0	0.075	0.3	50	5.0	10	±2000	±5.0	±22		LH0101AC		1-65
General Purpose FET Input	4.0	5.0	0.002	0.01	100	1.0	3.0	±10	±5.0	±22	LH0022			1-23
	6.0	5.0	0.005	0.025	75	1.0	3.0	±10	±5.0	±22		LH0022C		1-23
	20	5.0	0.005	0.025	50	1.0	3.0	±10	±5.0	±22	LH0042			1-23
	20	10	0.01	0.05	25	1.0	3.0	±10	±5.0	±22		LH0042C		1-23
	0.5	2.0	0.0005	0.0025	100	1.0	3.0	±10	±5.0	±22	LH0052			1-23
	1.0	5.0	0.001	0.005	75	1.0	3.0	±10	±5.0	±22		LH0052C		1-23
Wideband High Slew Rate	4.0	20	5000	30000	4.0	50	500	±10	±9.0	±18	LH0024			1-30
	8.0	25	15000	40000	3.0	50	400	±10	±9.0	±18		LH0024C		1-30
Wideband FET Input	5.0	25	0.025	0.1	1.0	70	500	±10	±5.0	±18	LH0032			1-33
	15	25	0.05	0.2	1.0	70	500	±10	±5.0	±18		LH0032C		1-33
Precision FET Input	0.05	0.2	5.0	30	500	0.4	0.06	±1.3	±3.0	±20	LH0044			1-39
	0.1	0.2	5.0	30	500	0.4	0.06	±1.3	±3.0	±20		LH0044C		1-39
	0.025	0.1	2.5	15	1000	0.4	0.06	±1.3	±3.0	±20	LH0044A			1-39
	0.025	0.1	2.5	15	1000	0.4	0.06	±1.3	±3.0	±20		LH0044AC		1-39
	0.05	0.2	5.0	30	500	0.4	0.06	±1.3	±3.0	±20		LH0044B		1-39
Medium Speed FET Input	5.0	5.0	0.002	0.01	50	15	70	±6.0	±5.0	±20	LH0062			1-59
	15	10	0.005	0.065	25	15	70	±6.0	±5.0	±20		LH0062C		1-59
Dual Precision	0.3	1.0	0.010	0.050	250	0.8	0.3	±15	±2.5	±20	LH2011			1-78
	0.6	2.0	0.010	0.100	250	0.8	0.3	±15	±2.5	±20	LH2011B			1-78
	1.0	3.0	0.025	0.180	90	0.8	0.3	±15	±2.5	±20		LH2011C		1-78
	2.0	15	10	75	50	1.0	0.5	±5.0	±3.0	±22	LH2101A			1-91
	2.0	15	10	75	50	1.0	0.5	±5.0	±3.0	±22		LH2201A		1-91
	7.5	30	50	250	25	1.0	0.5	±5.0	±3.0	±22			LH2301A	1-91
	0.5	5.0	0.2	2.0	80	1.0	0.3	±1.0	±2.0	±20	LH2108A			1-93
	0.5	5.0	0.2	2.0	80	1.0	0.3	±1.0	±2.0	±20		LH2208A		1-93
	0.5	5.0	1.0	7.0	80	1.0	0.3	±1.0	±2.0	±20			LH2308A	1-93
	2.0	15	0.2	2.0	50	1.0	0.3	±1.0	±2.0	±20	LH2108			1-93
	2.0	15	0.2	2.0	50	1.0	0.3	±1.0	±2.0	±20		LH2208		1-93
	7.5	30	1.0	7.0	50	1.0	0.3	±1.0	±2.0	±20			LH2308A	1-93
Dual Low Power	3.0	—	5.0	15	100	0.25	0.16	±0.75	±1.0	±18	LH2250	LH2250C		1-95
	6.0	—	10	30	75	0.25	0.16	±0.75	±1.0	±18	LH24250	LH24250C		1-95

Note: For information on monolithic operational amplifiers, consult the *Linear Databook*

Note 1: Specified for $A_V = -10$

National Semiconductor

LH0003/LH0003C Wide Bandwidth Operational Amplifier

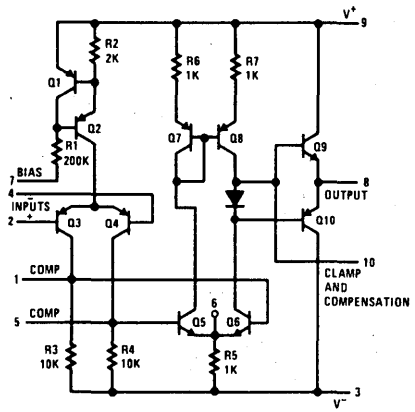
General Description

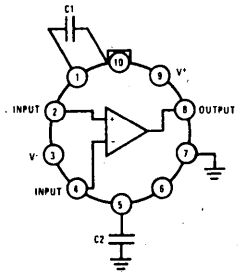
The LH0003/LH0003C is a general purpose operational amplifier which features: slewing rate up to 70 volts/μsec, a gain bandwidth of up to 30 MHz, and high output currents. Other features are:

- Very low offset voltage — Typically 0.4 mV
- Large output swing — > ±10V into 100Ω load
- High CMRR — Typically > 90 dB
- Good large signal frequency response — 50 kHz to 400 kHz depending on compensation

The LH0003 is specified for operation over the −55°C to +125°C military temperature range. The LH0003C is specified for operation over the 0°C to +85°C temperature range.

Schematic and Connection Diagrams





TOP VIEW

Order Number LH0003H or LH0003CH
See Package H10B

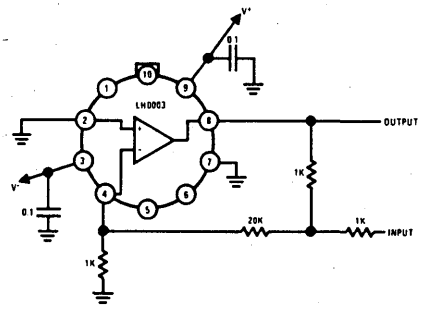
Circuit Gain	C_1 pF	C_2 pF	Slew Rate $R_L > 200\Omega$, V/μsec	Full Output Frequency R_L 200Ω V_{OUT} ±10 V
≥ 40	0	0	70	400
≥ 10	5	30	30	350
≥ 5	15	30	15	250
≥ 2	50	50	5	100
≥ 1	90	90	2	50

kHz

Typical Compensation

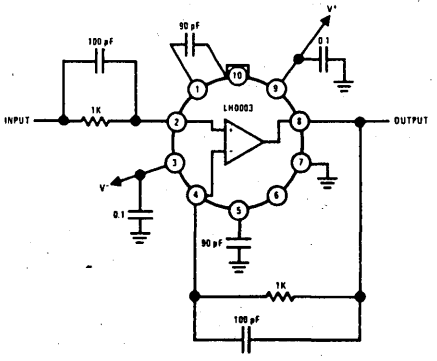
Typical Applications

High Slew Rate Unity Gain Inverting Amplifier



*Previously called NH0003/NH0003C

Unity Gain Follower



Absolute Maximum Ratings

Supply Voltage		±20V
Power Dissipation		See curve
Differential Input Voltage		±7V
Input Voltage		Equal to supply
Load Current		120 mA
Operating Temperature Range	LH0003	−55°C to +125°C
	LH0003C	0°C to+85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

Electrical Characteristics (Notes 1 & 2)

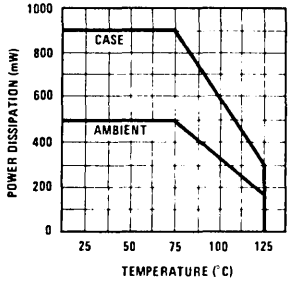
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S < 100\Omega$		0.4	3.0	mV
Input Offset Current			0.02	0.2	μA
Input Bias Current			0.4	2.0	μA
Supply Current	$V_S = \pm 20V$		1.2	3	mA
Voltage Gain	$R_L = 100k$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$	20	70		V/mV
Voltage Gain	$R_L = 2k$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$	15	40		V/mV
Output Voltage Swing	$V_S = \pm 15$, $R_L = 100\Omega$	±10	±12		V
Input Resistance			100		kΩ
Average Temperature Coefficient of Offset Voltage	$R_S < 100\Omega$		4		μV/°C
Average Temperature Coefficient of Bias Current			8		nA/°C
CMRR	$R_S < 100\Omega$, $V_S = \pm V$, $V_{IN} = \pm 10V$	70	90		dB
PSRR	$R_S < 100\Omega$, $V_S = \pm 15V$, $\Delta V = 5V$ to 20V	70	90		dB
Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 10 kHz to 100 kHz, $V_S = \pm 15V$ dc		1.8		μVrms

Note 1. These specifications apply for Pin 7 grounded, for $\pm 5V < V_S < \pm 20V$, with capacitor $C_1 = 90$ pF from Pin 1 to Pin 10 and $C_2 = 90$ pF from Pin 5 to ground, over the specified operating temperature range, unless otherwise specified.

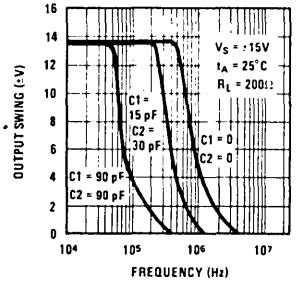
Note 2. Typical values are for $t_{AMBIENT} = 25°C$ unless otherwise specified.

Typical Performance

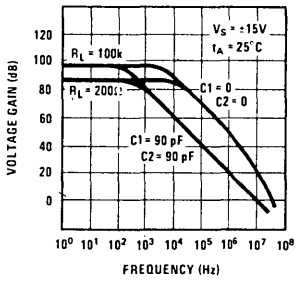
Maximum Power Dissipation



Large Signal Frequency Response



Open Loop Frequency Response



National Semiconductor

LH0004/LH0004C High Voltage Operational Amplifier

General Description

The LH0004/LH0004C is a general purpose operational amplifier designed to operate from supply voltages up to ±40V. The device dissipates extremely low quiescent power, typically 8 mW at 25°C and V_S = ±40V. Additional features include:

- Capable of operation over the range of ±5V to ±40V
- Large output voltage typically ±35V for the LH0004 and ±33V for the LH0004C into a 2 KΩ load with ±40V supplies
- Low input offset current typically 20 nA for the LH0004 and 45 nA for the LH0004C
- Low input offset voltage typically 0.3 mV
- Frequency compensation with 2 small capacitors
- Low power consumption 8 mW at ±40V

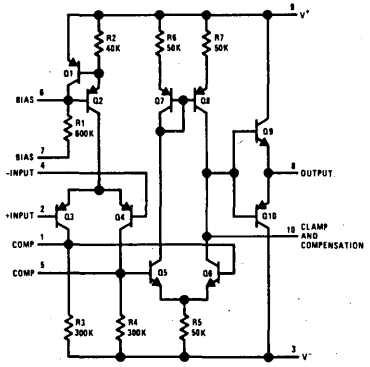
The LH0004's high gain and wide range of operating voltages make it ideal for applications requiring large output swing and low power dissipation.

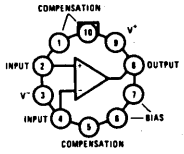
The LH0004 is specified for operation over the −55°C to +125°C military temperature range. The LH0004C is specified for operation over the 0°C to +85°C temperature range.

Applications

- Precision high voltage power supply
- Resolver excitation
- Wideband high voltage amplifier
- Transducer power supply

Schematic and Connection Diagrams



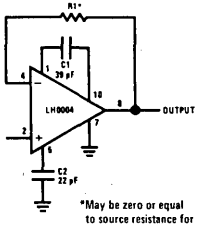


Note: Pin 7 must be grounded or connected to a voltage at least 5V more negative than the positive supply (Pin 9). Pin 7 may be connected to the negative supply; however, the standby current will be increased. A resistor may be inserted in series with Pin 7 to Pin 9. The value of the resistor should be a maximum of 100 KΩ per volt of potential between Pin 3 and Pin 9.

Order Number LH0004H or LH0004CH
See Package H10B

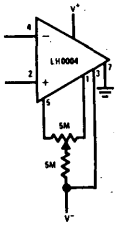
Typical Applications

Voltage Follower

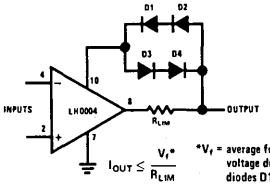


*May be zero or equal to source resistance for minimum offset.

Input Offset Voltage Adjust

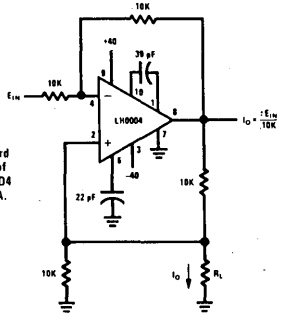


External Current Limiting Method



*V_f = average forward voltage drop of diodes D1 to D4 at 20 to 50 μA.

High Compliance Current Source



*Previously called NH0004/NH0004C

Absolute Maximum Ratings

Supply Voltage, Continuous	±45V
Power Dissipation (See curve)	400 mW
Differential Input Voltage	±7V
Input Voltage	Equal to supply
Short Circuit Duration	3 sec
Operating Temperature Range LH0004	−55°C to +125°C
LH0004C	0°C to 85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

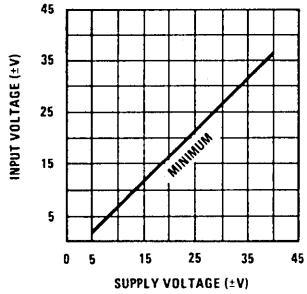
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LH0004			LH0004C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\,\Omega$, $T_A = 25°C$		0.3	1.0		0.3	1.5	mV
	$R_S \leq 100\,\Omega$			2.0			3.0	mV
Input Bias Current	$T_A = 25°C$		20	100		30	120	nA
				300			300	nA
Input Offset Current	$T_A = 25°C$		3	20		10	45	nA
				100			150	nA
Positive Supply Current	$V_S = \pm40V$, $T_A = 25°C$		110	150		110	150	μA
	$V_S = \pm40V$			175			175	μA
Negative Supply Current	$V_S = \pm40V$, $T_A = 25°C$		80	100		80	100	μA
	$V_S = \pm40V$			135			135	μA
Voltage Gain	$V_S = \pm40V$, $R_L = 100k$, $T_A = 25°C$, $V_{OUT} = \pm30V$	30	60		30	60		V/mV
	$V_S = \pm40V$, $R_L = 100k$, $V_{OUT} = \pm30V$	10			10			V/mV
Output Voltage	$V_S = \pm40V$, $R_L = 10k$	±30	±35		±30	±33		V
CMRR	$V_S = \pm40V$, $R_S \leq 5k$, $V_{IN} = \pm33V$	70	90		70	90		dB
PSRR	$V_S = \pm40V$, $R_S \leq 5k$, $\Delta V = 20V$ to $40V$	70	90		70	90		dB
Average Temperature Coefficient Offset Voltage	$R_S \leq 100\,\Omega$		4.0			4.0		μV/°C
Average Temperature Coefficient of Offset Current			0.4			0.4		nA/°C
Equivalent Input Noise Voltage	$R_S = 100\,\Omega$, $V_S = \pm40\,V$, $f = 500$ Hz to 5 kHz, $T_A = 25°C$		3.0			3.0		μVrms

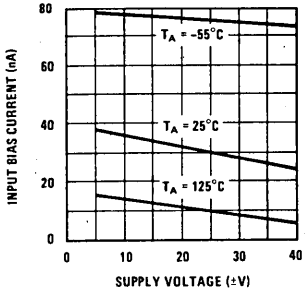
Note 1: These specifications apply for $\pm5V \leq V_S \leq \pm40V$, Pin 7 grounded, with capacitors C1 = 39 pF between Pin 1 and Pin 10, C2 = 22 pF between Pin 5 and ground, −55°C to +125°C for the LH0004, and 0°C to +85°C for the LH0004C unless otherwise specified.

Typical Performance

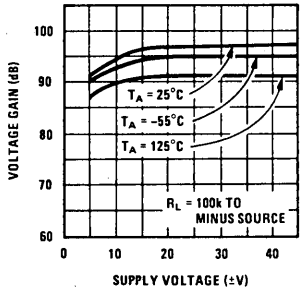
Input Voltage Range



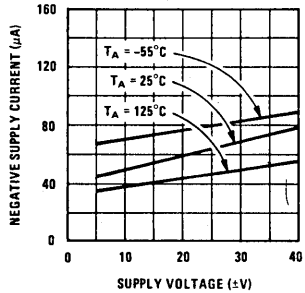
Input Bias Current



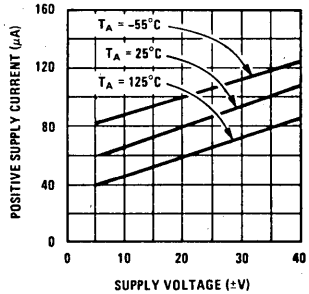
Voltage Gain



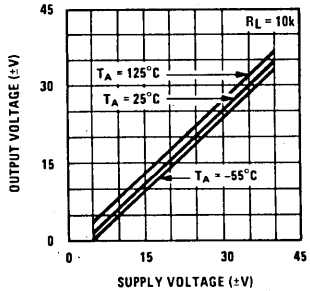
Negative Supply Current



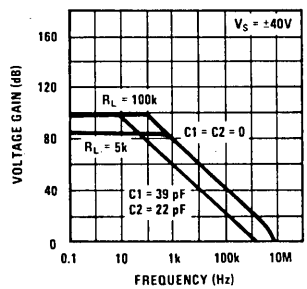
Positive Supply Current



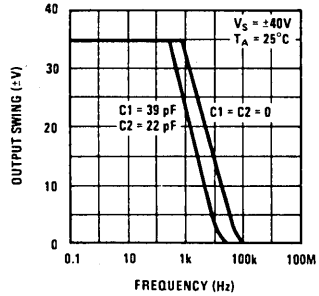
Output Voltage



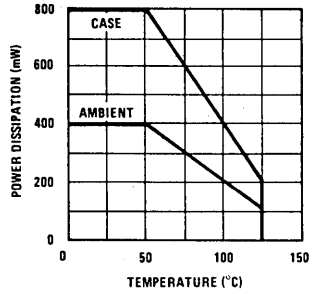
Open Loop Frequency Response



Large Signal Frequency Response



Package Power Dissipation



National Semiconductor

LH0005/LH0005A Operational Amplifier

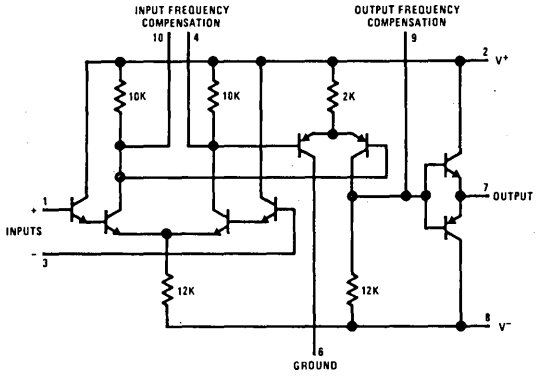
General Description

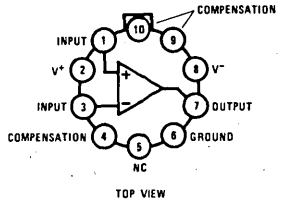
The LH0005/LH0005A is a hybrid integrated circuit operational amplifier employing thick film resistors and discrete silicon semiconductors in its design. The select matching of the input pairs of transistors results in low input bias currents and a very low input offset current, both of which exhibit excellent temperature tracking. In addition, the device features:

- Very high output current capability: ±50 mA into a 100 ohm load
- Low standby power dissipation: typically 60 mW at ±12V
- High input resistance: typically 2M at 25°C
- Full operating range: −55°C to +125°C
- Good high frequency response: unity gain at 30 MHz

With no external roll-off network, the amplifier is stable with a feedback ratio of 10 or greater. By adding a 200 pF capacitor between pins 9 and 10, and a 200 ohm resistor in series with a 75 pF capacitor from pin 4 to ground, the amplifier is stable to unity gain. The unity gain loop phase margin with the above compensation is typically 70 degrees. With a gain of 10 and no compensation the loop phase margin is typically 50 degrees.

Schematic and Connection Diagrams



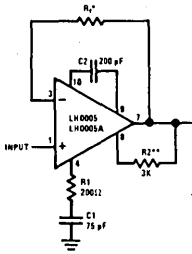


TOP VIEW

Order Number LH0005H or LH0005AH
See Package H10D

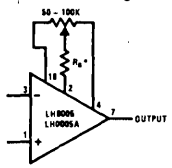
Typical Applications

Voltage Follower



*May be zero or equal to the input resistance for minimum offset.
**To minimize crossover distortion at higher frequencies. May be omitted for low frequency application or selected to suit design requirements

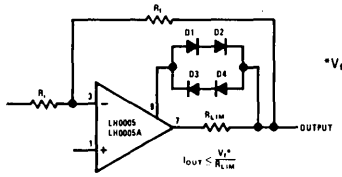
Offset Balancing Circuit



*Typical value, R_B = 100K. R_B may be increased for greater sensitivity with reduction in range.

*Previously called NH0005/NH0005A

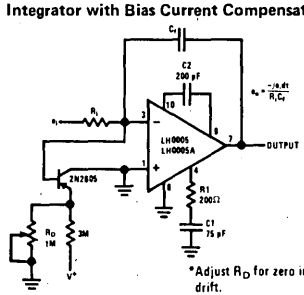
External Current Limiting



*V_f = Average forward voltage drop of diodes D_1 to D_4 at approx. 1 mA.

For continuous short circuit protection (V_S = ±12V, −55°C ≤ T_A ≤ +100°C) $R_{LIM} \geq 50\Omega$

Integrator with Bias Current Compensation



*Adjust R_D for zero integration drift.

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (see Curve)	400 mW
Differential Input Voltage	±15V
Input Voltage	Equal to supply voltages
Peak Load Current	±100 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

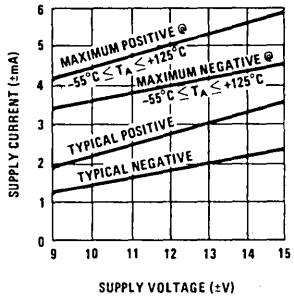
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LH0005			LH0005A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage								
25°C	$R_S \leq 100\,\Omega$		5	10		1	3	mV
−55°C, 125°C	$R_S \leq 100\,\Omega$			10			4	mV
Input Offset Current								
25°C to 125°C			10	20		2	5	nA
−55°C			25	75		10	25	nA
Input Bias Current								
25°C to 125°C			15	50		8	25	nA
−55°C			100	250		60	125	nA
Large Signal Voltage Gain								
−55°C to 25°C	R_L = 10K, R2 = 3K, V_{OUT} = ±5V	2	4		4	5.5		V/mV
125°C		1.5	3		3	5		V/mV
Output Voltage Swing								
−55°C to 125°C	R_L = 10 kΩ	−10		+6	−10		+6	V
25°C to 125°C	R_L = 100Ω	−5		+5	−5		+5	V
−55°C	R_L = 100Ω	−4		+4	−4		+4	V
Input Resistance								
25°C		1	2		1	2		MΩ
Common Mode Rejection Ratio								
25°C	V_{IN} = ±4V, $RS \leq 100\,\Omega$	55	60		60	66		dB
Power Supply Rejection Ratio								
25°C		55	60		60	66		dB
Supply Current (+)								
−55°C to 125°C			3	5		3	5	mA
Supply Current (−)								
−55°C to 125°C			2	4		2	4	mA
Average Temperature Coefficient of Input Offset Voltage								
−55°C to 125°C	$R_S \leq 100\,\Omega$		20			10		uV/°C
Output Resistance								
25°C			70			70		Ω

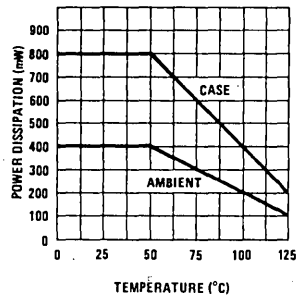
Note 1: These specifications apply for pin 6 grounded, V_S = ±12V, with Resistor R_1 = 200Ω in series with Capacitor C_1 = 75 pF from pin 4 to ground, and C_2 = 200 pF between pins 9 and 10 unless otherwise specified.

Guaranteed Performance Characteristics

Supply Current

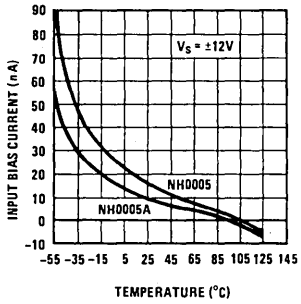


Maximum Power Dissipation

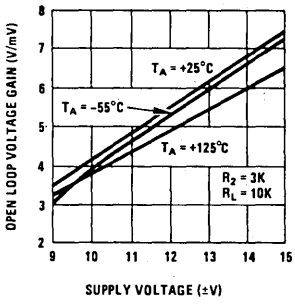


Typical Performance Characteristics

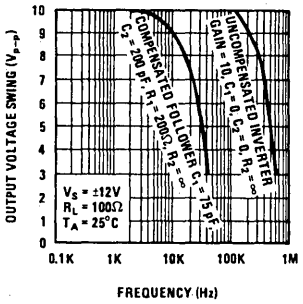
Input Bias Current



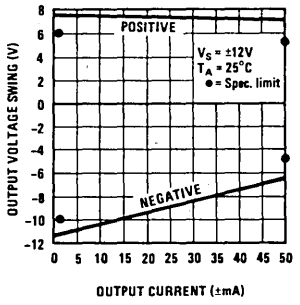
Voltage Gain



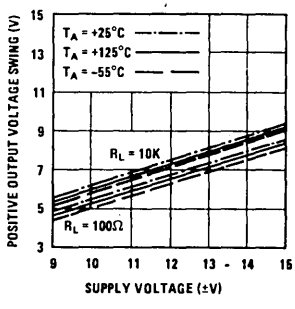
Loaded Output Voltage Swing



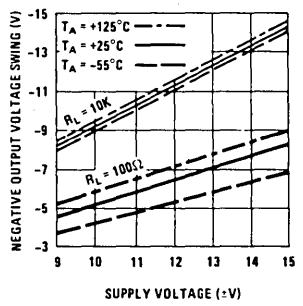
DC Output Voltage Swing



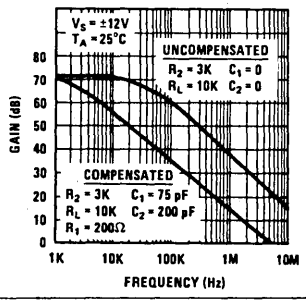
Positive Output Voltage Swing



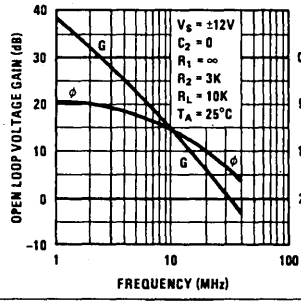
Negative Output Voltage Swing



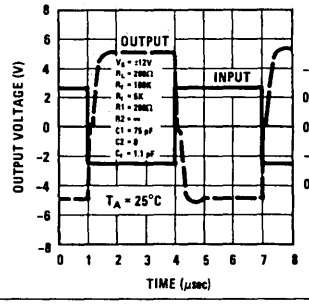
Frequency Response



Open Loop Gain vs Excess Phase



Inverting Pulse Response



National Semiconductor

LH0005C Operational Amplifier

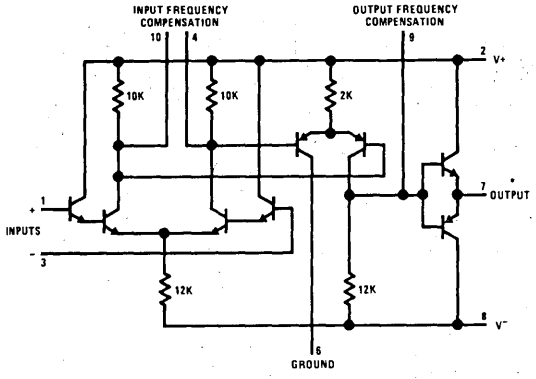
General Description

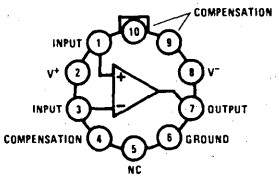
The LH0005C is a hybrid integrated circuit operational amplifier employing thick film resistors and discrete silicon semiconductors in its design. The select matching of the input pairs of transistors results in low input bias currents and a very low input offset current both of which exhibit excellent temperature tracking. In addition, the device features:

- Very high output current capability: ±40 mA into a 100 ohm load
- Low standby power dissipation: typically 60 mW at ±12V
- High input resistance: typically 2M at 25°C
- Operating range: 0° to 85°C
- Good high frequency response: unity gain at 30 MHz

With no external roll-off network, the amplifier is stable with a feedback ratio of 10 or greater. By adding a 200 pF capacitor between pins 9 and 10, and a 200 ohm resistor in series with a 75 pF capacitor from pin 4 to ground, the amplifier is stable to unity gain. The unity gain loop phase margin with the above compensation is typically 70 degrees. With a gain of 10 and no compensation the loop phase margin is typically 50 degrees.

Schematic and Connection Diagrams



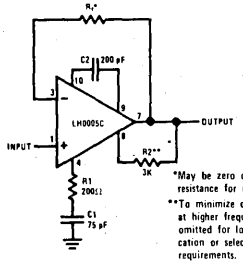


TOP VIEW

Order Number LH0005CH
See Package H10D

Typical Applications

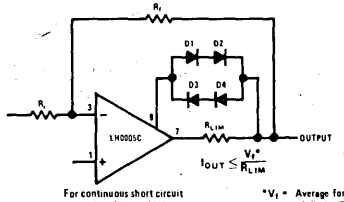
Voltage Follower



*May be zero or equal to the input resistance for minimum offset.

**To minimize crossover distortion at higher frequencies. May be omitted for low frequency application or selected to suit design requirements.

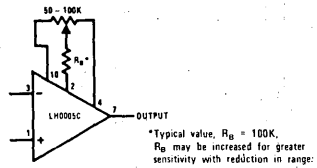
External Current Limiting



For continuous short circuit protection (V_S = ±12V, 0°C ≤ T_A ≤ 70°C $R_{LIM} \geq 50\Omega$

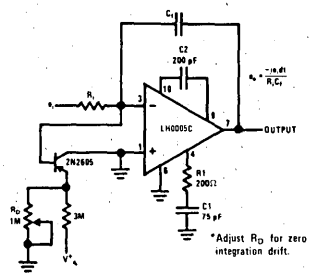
*V_f = Average forward voltage drop of diodes D_1 to D_4 at approx. 1 mA

Offset Balancing Circuit



*Typical value, R_B = 100K. R_B may be increased for greater sensitivity with reduction in range.

Integrator With Bias Current Compensation



*Adjust R_D for zero integration drift.

*Previously called NH0005C

Absolute Maximum Ratings

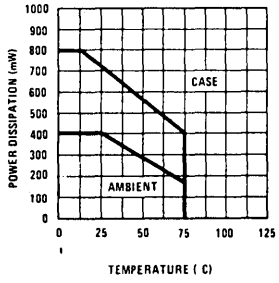
Supply Voltage	±20V
Power Dissipation (see Curve)	400 mW
Differential Input Voltage	±15V
Input Voltage	Equal to supply voltages
Peak Load Current	±100 mA
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to 85°C
Lead Temperature (soldering, 10 sec)	300°C

Electrical Characteristics

PARAMETER	CONDITIONS	LH0005C MIN	LH0005C TYP (Note 2)	LH0005C MAX	UNITS
Input Offset Voltage	$R_S \leq 100\,\Omega$		3	10	mV
Input Offset Current			5	25	nA
Input Bias Current			20	100	nA
Large Signal Voltage Gain	R_L = 10K, R2 = 3K, V_{OUT} = ±5V	2	5		V/mV
Output Voltage Swing	R_L = 10 kΩ R_L = 100Ω	−10 −4	 ±6	+6 +4	V V
Input Resistance	T_A = 25°C	0.5	2		MΩ
Common Mode Rejection Ratio	V_{IN} = ±4V, $R_S \leq 100\,\Omega$, T_A = 25°C	50	60		dB
Power Supply Rejection Ratio	T_A = 25°C	50	60		dB
Supply Current (+)			3	5	mA
Supply Current (−)			2	4	mA

Note 1: These specifications apply for pin 6 grounded, V_S = ±12V, with Resistor R1 = 200Ω in series with Capacitor C1 = 75 pF from pin 4 to ground, and C2 = 200 pF between pins 9 and 10, over the temperature range of 0°C to +85°C unless otherwise specified.

Note 2: Typical values are for 25°C only.



Maximum Power Dissipation

National Semiconductor

LH0020/LH0020C High Gain Operational Amplifier

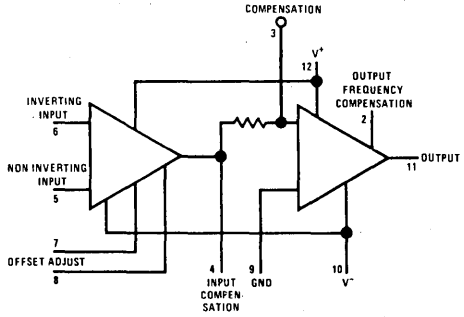
General Description

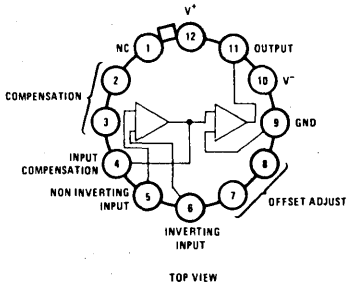
The LH0020/LH0020C is a general purpose operational amplifier designed to source and sink 50 mA output currents. In addition to its high output capability, the LH0020/LH0020C exhibits excellent open loop gain, typically in excess of 100 dB. The parameters of the LH0020 are guaranteed over the temperature range of −55°C to +125°C and $\pm 5V \leqslant V_S \leqslant \pm 22V$, while those of the LH0020C are guaranteed over the temperature range of 0°C to 85°C and $\leq \pm 5V \leq V_S \leq \pm 18V$. Additional features include:

- Low offset voltage typically 1.0 mV at 25°C over the entire common mode voltage range.
- Low offset current typically 10 nA at 25°C for the LH0020 and 30 nA for the LH0020C.
- Offset voltage is adjustable to zero with a single potentiometer.
- ±14V, 50 mA output capability.

Output current capability, excellent input characteristics, and large open loop gain make the LH0020/LH0020C suitable for application in a wide variety of applications from precision dc power supplies to precision medium power comparator.

Schematic and Connection Diagrams

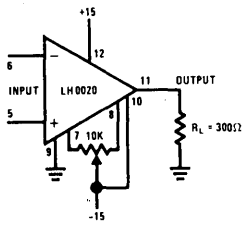




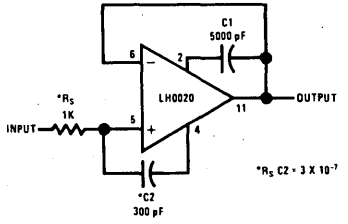
Order Number LH0020G or LH0020CG
See Package H12B

Typical Applications

Offset Adjustment



Unity Gain Frequency Compensation



*Previously called NH0020/NH0020C

Absolute Maximum Ratings

Supply Voltage		±22V
Power Dissipation		1.5W
Differential Input Voltage		±30V
Input Voltage (Note 1)		±15V
Output Short Circuit Duration		Continuous
Operating Temperature Range	LH0020	-55°C to +125°C
	LH0020C	0°C to 85°C
Storage Temperature		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

Electrical Characteristics

PARAMETER	CONDITIONS	LH0020				LH0020C				UNITS
		TEMP °C	MIN	TYP	MAX	TEMP °C	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\Omega$	25		1.0	2.5	25		1.0	6.0	mV
		-55 to +125		2.0	4.0	0 to 85		3.0	7.5	mV
Input Offset Current		25		10	50	25		30	200	nA
		-55 to +125			100	0 to 85			300	nA
Input Bias Current		25		60	250	25		200	500	nA
		-55 to +125			500	0 to 85			800	nA
Supply Current	$V_S = \pm 15V$	25		3.5	5.0	25		3.6	6.0	mA
Input Resistance		25	0.6	1.0		25	0.3	1.0		MΩ
Large Signal Voltage Gain	$V_S = \pm 15V, R_L = 300\Omega, V_O = \pm 10V$	25	100	300		25	50	150		V/mV
	$V_S = \pm 15V, R_L = 300\Omega, V_O = \pm 10V$	-55 to +125	50			0 to 85	30			V/mV
Output Voltage Swing	$V_S = \pm 15V, R_L = 300\Omega$	25	14.2	14.5		25	14.0	14.2		V
		-55 to +125	14.0			0 to 85	13.5			V
Output Short Circuit Current	$V_S = \pm 15V$ $R_L = 0\Omega$	25		100	130	25	25	120	140	mA
Input Voltage Range	$V_S = \pm 15V$	-55 to +125	±12			0 to 85	±12			V
										V
Common Mode Rejection Ratio	$R_S \leq 100\Omega$	-55 to +125	90	96		0 to 85	90	96		dB
Power Supply Rejection Ratio	$R_S \leq 100\Omega$	-55 to +125	90	96		0 to 85	90	96		dB

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: These specifications apply for $\pm 5V \leq V_S \leq \pm 22V$ for the LH0020, $\pm 5V \leq V_S \leq \pm 18V$ for the LH0020C, pin 9 grounded, and a 5000 pF capacitor between pins 2 and 3, unless otherwise specified.

National Semiconductor

LH0021/LH0021C 1.0 Amp Power Operational Amplifier
LH0041/LH0041C 0.2 Amp Power Operational Amplifier

General Description

The LH0021/LH0021C and LH0041/LH0041C are general purpose operational amplifiers capable of delivering large output currents not usually associated with conventional IC Op Amps. The LH0021 will provide output currents in excess of one ampere at voltage levels of ±12V; the LH0041 delivers currents of 200 mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload. The devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

Features

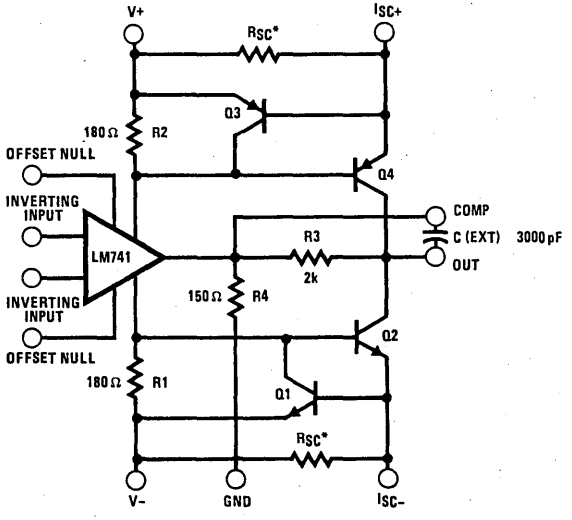
- Output current 1.0 Amp (LH0021)
  0.2 Amp (LH0041)
- Output voltage swing ±12V into 10Ω (LH0021)
  ±14V into 100Ω (LH0041)
- Wide full power bandwidth 15 kHz
- Low standby power 100 mW at ±15V
- Low input offset voltage and current 1 mV and 20 nA
- High slew rate 3.0V/μs
- High open loop gain 100 dB

The excellent input characteristics and high output capability of the LH0021 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

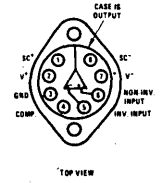
The LH0041 is particularly suited for applications such as torque driver for inertial guidance systems, diddle yoke driver for alpha-numeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

The LH0021 is supplied in a 8 pin TO-3 package rated at 20 watts with suitable heatsink. The LH0041 is supplied in both 12 pin TO-8 (2.5 watts with clip on heatsink) and a power 8 pin ceramic DIP (2 watts with suitable heatsink). The LH0021 and LH0041 are guaranteed over the temperature range of −55°C to +125°C while the LH0021C and LH0041C are guaranteed from −25°C to +85°C

Schematic and Connection Diagrams

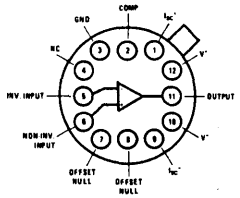


*RSC external on "G" and "K" packages. RSC internal on "J" package. Offset Null connections available only on "G" package.

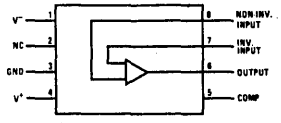


TOP VIEW

Order Number
LH0021K or LH0021CK
See Package K08A



Order Number
LH0041G or LH0041CG
See Package H12B



TOP VIEW

Order Number
LH0041CJ
See Package HY08A

Absolute Maximum Ratings

Supply Voltage		±18V
Power Dissipation		See curves
Differential Input Voltage		±30V
Input Voltage (Note 1)		±15V
Peak Output Current (Note 2)	LH0021/LH0021C	2.0 Amps
	LH0041/LH0041C	0.5 Amps
Output Short Circuit Duration (Note 3)		Continuous
Operating Temperature Range	LH0021/LH0041	−55°C to +125°C
	LH0021C/LH0041C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

DC Electrical Characteristics for LH0021/LH0021C (Note 4)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0021			LH0021C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S < 100\Omega$, $T_C = 25°C$		1.0	3.0		3.0	6.0	mV
	$R_S \leq 100\Omega$			5.0			7.5	mV
Voltage Drift with Temperature	$R_S < 100\Omega$		3	25		5	30	µV/°C
Offset Voltage Drift with Time			5			5		µV/week
Offset Voltage Change with Output Power			5	15		5	20	µV/watt
Input Offset Current	$T_C = 25°C$		30	100		50	200	nA
				300			500	nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_C = 25°C$		100	300		200	500	nA
				1.0			1.0	µA
Input Resistance	$T_C = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$							
	$R_L = 1\ k\Omega$, $T_C = 25°C$,	100	200		100	200		V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$							
	$R_L = 100\Omega$,	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$	±13.5	14		±13	±14		V
	$V_S = \pm 15V$, $R_L = 10\Omega$, $T_C = 25°C$	±11.0	±12		±10	±12		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_C = 25°C$, $R_{SC} = 0.5\Omega$	0.8	1.2	1.6	0.8	1.2	1.6	Amps
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

AC Electrical Characteristics for LH0021/LH0021C ($T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000\,pF$)

Slew Rate	$A_V = +1$, $R_L = 100\Omega$	0.8	3.0		1.0	3.0		V/µs
Power Bandwidth	$R_L = 100\Omega$		20			20		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	µs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		µs
Overload Recovery Time			3			3		µs
Harmonic Distortion	f = 1 kHz, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_S = 50\Omega$, B.W. = 10 Hz to 10 kHz		5			5		µV rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA rms

DC Electrical Characteristics for LH0041/LH0041C (Note 4)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0041			LH0041C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$		1.0	3.0		3.0	6.0	mV
	$R_S \leq 100\Omega$			5.0			7.5	mV
Voltage Drift with Temperature	$R_S \leq 100\Omega$		3			5		µV/°C
Offset Voltage Drift with Time			5			5		µV/week
Offset Voltage Change with Output Power			15			15		µV/watt
Offset Voltage Adjustment Range	(Note 5)		20			20		mV
Input Offset Current	$T_A = 25°C$		30	100		50	200	nA
				300			500	nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_A = 25°C$		100	300		200	500	nA
				1.0			1.0	µA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$							
	$R_L = 1\ k\Omega$, $T_A = 25°C$	100	200		100	200		V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$							
	$R_L = 100\Omega$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$	±13.0	14.0		±13.0	±14.0		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_A = 25°C$ (Note 6)		200	300		200	300	mA
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0.	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

AC Electrical Characteristics for LH0041/LH0041C ($T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000\,pF$)

Slew Rate	$A_V = +1$, $R_L = 100\Omega$	1.5	3.0		1.0	3.0		V/µs
Power Bandwidth	$R_L = 100\Omega$		20			20		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	µs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		µs
Overload Recovery Time			3			3		µs
Harmonic Distortion	f = 1 kHz, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_S = 50\Omega$, B.W. = 10 Hz to 10 kHz		5			5		µV/rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA/rms

Note 1: Rating applies for supply voltages above ±15V. For supplies less than ±15V, rating is equal to supply voltage.

Note 2: Rating applies for LH0041G and LH0021K with $R_{SC} = 0\Omega$.

Note 3: Rating applies as long as package power rating is not exceeded.

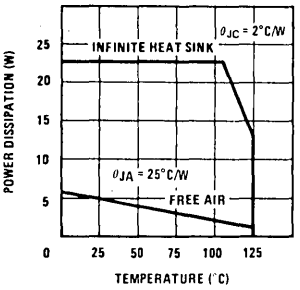
Note 4: Specifications apply for $\pm 5V \leq V_S \pm 18V$, and $-55°C \leq T_C = \leq 125°C$ for LH0021K and LH0041G, and $-25°C \leq T_C \leq +85°C$ for LH0021CK, LH0041CG and LH0041CJ unless otherwise specified. Typical values are for 25°C only.

Note 5: TO-8 "G" packages only.

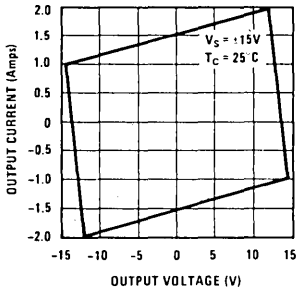
Note 6: Rating applies for "J" DIP package and for TO-8 "G" package with $R_{SC} = 3.3$ ohms.

Typical Performance Characteristics

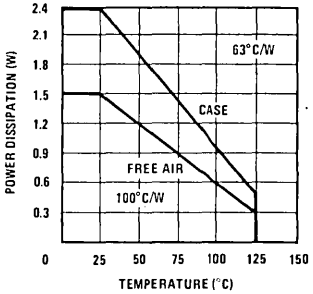
Power Derating-LH0021



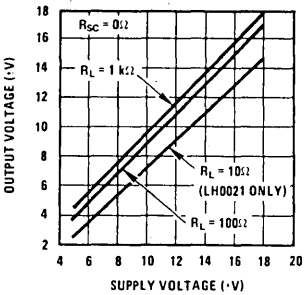
Safe Operating Area – LH0021



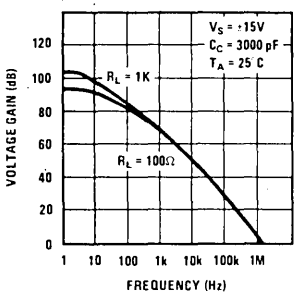
Package Power Dissipation LH0041/LH0041C



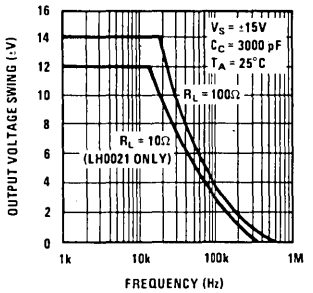
Output Voltage Swing



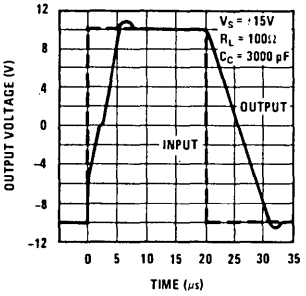
Open Loop Frequency Response



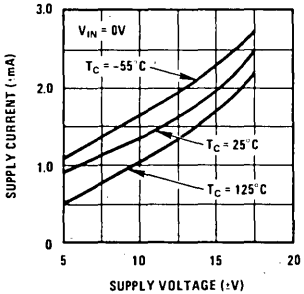
Large Signal Frequency Response



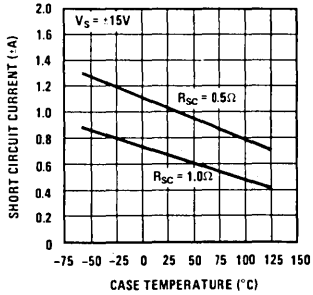
Voltage Follower Pulse Response



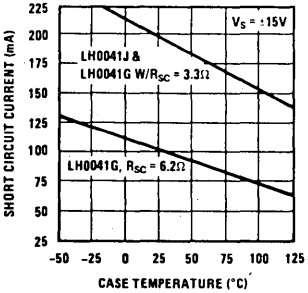
No Load Supply Current



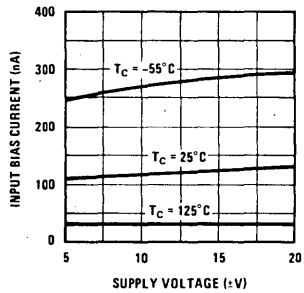
Short Circuit Current vs Temperature LH0021/LH0021C



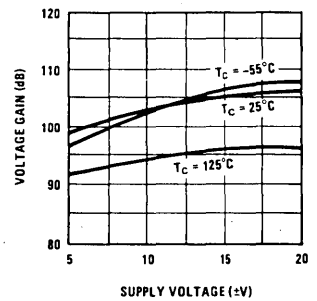
Short Circuit Current vs Temperature LH0041/LH0041C



Input Bias Current

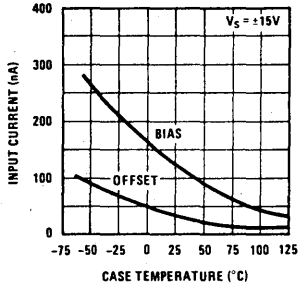


Voltage Gain

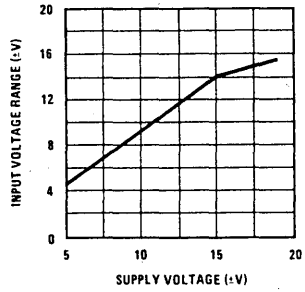


Typical Performance Characteristics (Cont'd)

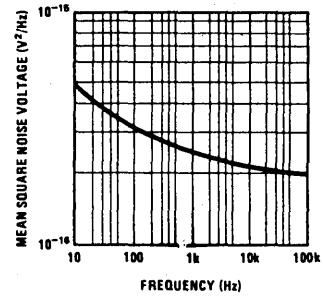
Input Current



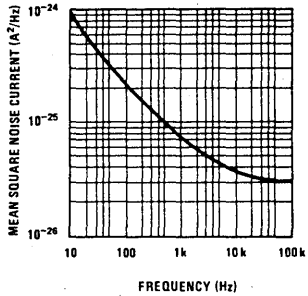
Input Voltage Range



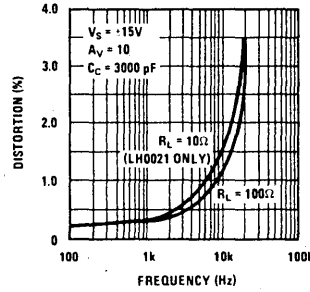
Input Noise Voltage



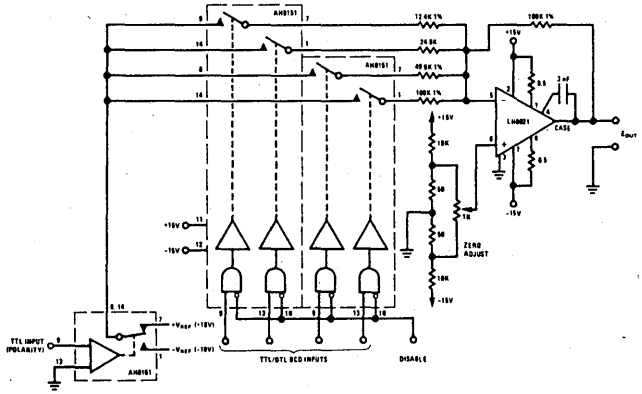
Input Noise Current



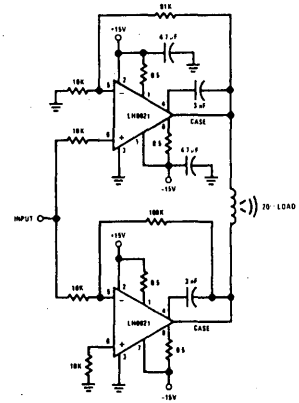
Distortion vs Frequency



Typical Applications

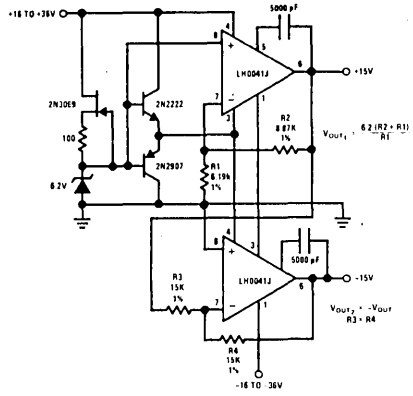


Programmable One Amp Power Supply

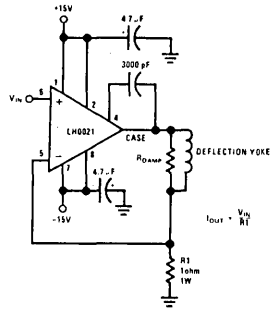


10 WATT (rms) Audio Amplifier

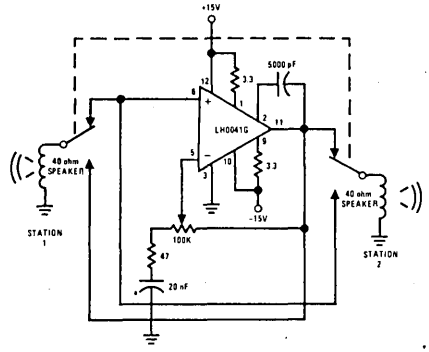
Typical Applications (Cont'd)



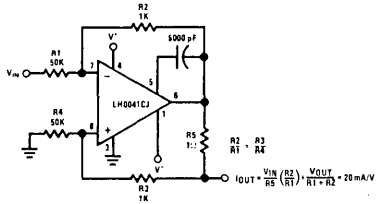
Dual Tracking One Amp Power Supply



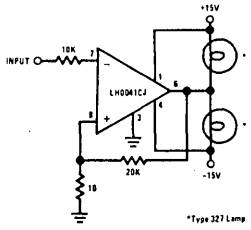
CRT Deflection Yoke Driver



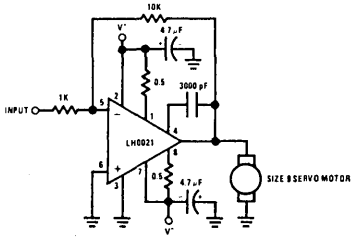
Two Way Intercom



Programmable High Current Source/Sink

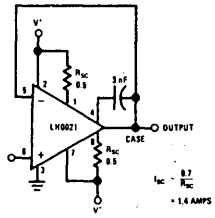


Power Comparator

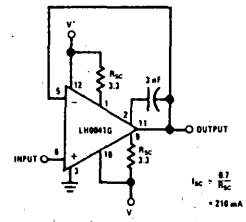


DC Servo Amplifier

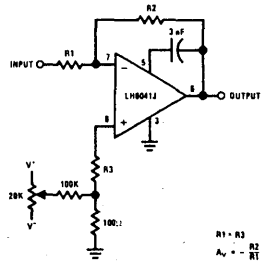
Auxiliary Circuits



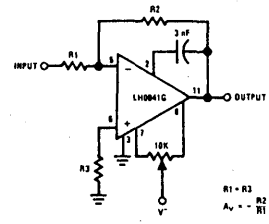
LH0021 Unity Gain Circuit with Short Circuit Limiting



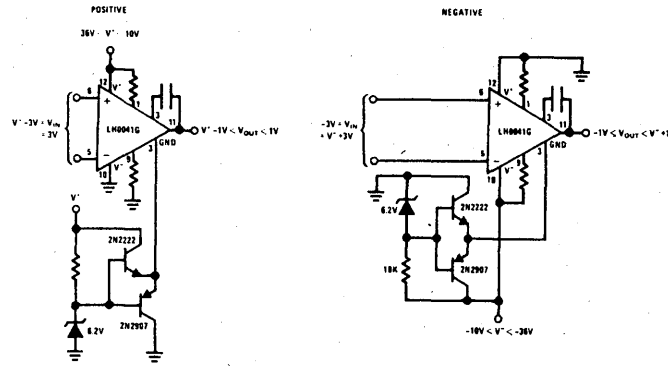
LH0041G Unity Gain with Short Circuit Limiting



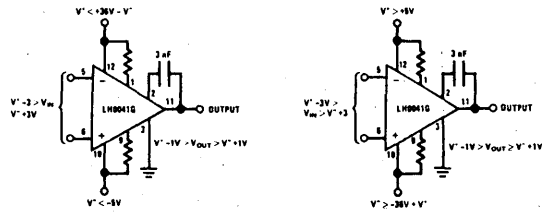
LH0041/LH0021 Offset Voltage Null Circuit (LH0041CJ Pin Connections Shown)*



LH0041G Offset Voltage Null Circuit *



Operation from Single Supplies



Operation from Non-Symmetrical Supplies

*For additional offset null circuit techniques see National Linear Applications Handbook.

National Semiconductor

LH0022/LH0022C High Performance FET Op Amp
LH0042/LH0042C Low Cost FET Op Amp
LH0052/LH0052C Precision FET Op Amp

General Description

The LH0022/LH0042/LH0052 are a family of FET input operational amplifiers with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 500 microvolts maximum offset and 5 $\mu V/^{\circ}C$ offset drift. Input offset current is less than 500 femtoamps at room temperature and 500 pA maximum at 125°C. The LH0022 and LH0042 are not internally nulled but offer comparable matching characteristics. All devices in the family are internally compensated and are free of latch-up and unusual oscillation problems. The devices may be offset nulled with a single 10k trimpot with neglible effect in CMRR.

The LH0022, LH0042 and LH0052 are specified for operation over the -55°C to +125°C military temperature range. The LH0022C, LH0042C and LH0052C are specified for operation over the -25°C to +85°C temperature range.

Features

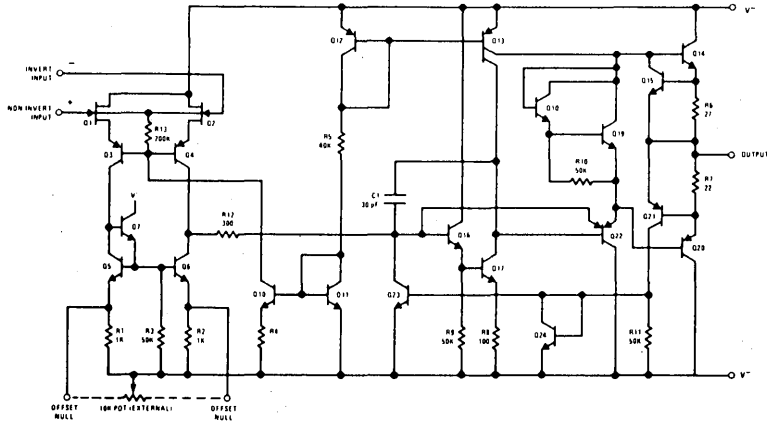
- Low input offset current—500 femtoamps max. (LH0052)
- Low input offset drift—5$\mu V/^{\circ}C$ max (LH0052)
- Low input offset voltage — 100 microvolts-typ.
- High open loop gain — 100 dB typ.
- Excellent slew rate — 3.0 V/μs typ.
- Internal 6 dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

The LH0022/LH0042/LH0052 family of IC op amps are intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers. The LH0022 and LH0042 provide low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

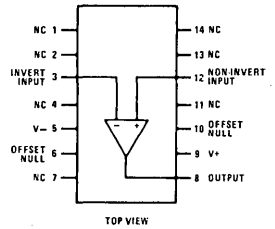
Special electrical parameter selection and custom built circuits are available on special request.

For additional application information and information on other National operational amplifiers, see *Available Linear Applications Literature.*

Schematic and Connection Diagrams



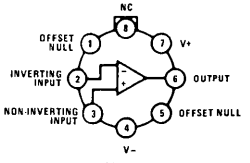
Dual-In-Line Package



TOP VIEW

Order Number LH0022D, LH0022CD, LH0042D, LH0042CD, LH0052D or LH0052CD
See Package D14E

Metal Can Package



TOP VIEW

Order Number LH0022H, LH0022CH, LH0042H, LH0042CH, LH0052H or LH0052CH
See Package H08A

*Previously Called NH0022/NH0022C

Absolute Maximum Ratings

Supply Voltage	±22V
Power Dissipation (see graph)	500 mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V^-	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0022, LH0042, LH0052	−55°C to +125°C
LH0022C, LH0042C, LH0052C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

DC Electrical Characteristics for LH0022/LH0022C (Note 3)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0022			LH0022C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\ k\Omega$; $T_A = 25°C$, $V_S = \pm 15V$		2.0	4.0		3.5	6.0	mV
	$R_S \leq 100\ k\Omega$, $V_S = \pm 15V$			5.0			7.0	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5	10		5	15	µV/°C
Offset Voltage Drift with Time			3			4		µV/week
Input Offset Current	(Note 4)		0.2	2.0		1.0	5.0	pA
				2.0			0.5	nA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	(Note 4)		5	10		10	25	pA
				10			2.5	nA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm 15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$	80	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	80	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$, $V_S = \pm 15V$	100	200		75	160		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $V_S = \pm 15V$	50			50			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$, $V_S = \pm 15V$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm 15V$		2.0	2.5		2.4	2.8	mA
Power Consumption	$V_S = \pm 15V$			75			85	mW

DC Electrical Characteristics for LH0042/LH0042C (Note 3)

Parameter	Conditions	Limits						Units
		LH0042			LH0042C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$R_S \leq 100k\Omega$		5.0	20		6.0	20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100k\Omega$		5.0			10		µV/°C
Offset Voltage Drift with Time			7.0			10		µV/week
Input Offset Current	(Note 4)		1.0	5.0		2.0	10	pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	(Note 4)		10	25		15	50	pA
Temperature Coeffieient of Input Bias Current		Doubles every 10°C			Doubles every 19°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range		±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$, $V_{IN} = \pm 10V$	70	86		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	70	86		70	80		dB
Large Signal Voltage Gain	$R_S \leq 2k\Omega$, $V_{OUT} = \pm 10V$	50	150		25	100		V/mV
Output Voltage Swing	$R_L = 1k\Omega$, $T_A = 25°C$ $R_L = 2k\Omega$	±10 ±10	±12.5		±10 ±10	±12		V V
Output Current Swing	$V_{OUT} = \pm 10V$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current			2.5	3.5		2.8	4.0	mA
Power Consumption				105			120	mW

DC Electrical Characteristics For LH0052/LH0052C (Note 3)

Parameter	Conditions	Limits						Units
		LH0052			LH0052C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$R_S < 100k\Omega$, $V_S = +15V$ $T_A = 25°C$ $R_S < 100k\Omega$, $V_S = \pm 15V$		0.1	0.5 1.0		0.2	1.0 1.5	mV mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100k\Omega$, $V_S = \pm 15V$		2.0	5.0		5.0	10	µV/°C
Offset Voltage Drift with Time			2.0			4.0		µV/week
Input Offset Current	(Note 4)		0.01	5.0 500		0.02	1.0 100	pA pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time		<0.1			<0.1			pA/week
Input Bias Current	(Note 4)		0.5	2.5 2.5		1.0	5.0 0.5	pA nA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm 15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$, $V_{IN} = \pm 10V$	74	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	74	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2K\Omega$, $V_{OUT} = \pm 10V$ $V_S = \pm 15V$, $T_A = 25°C$	100	200		75	160		V/mV
	$R_L = 2k\Omega$, $V_{OUT} = \pm 10V$ $V_S = \pm 15V$	50			50			V/mV
Output Voltage Swing	$R_L = 1k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$	±10	±12.5		±10	±12		V
	$R_L = 2k\Omega$, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $t_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm 15V$		3.0	3.5		3.0	3.8	mA
Power Consumption	$V_S = \pm 15V$			105			114	mW

AC Electrical Characteristics For all amplifiers ($T_A = 25°C$, $V_S = \pm 15V$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0022/42/52			LH0022C/42C/52C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	Voltage Follower	1.5	3.0		1.0	3.0		V/μs
Large Signal Bandwidth	Voltage Follower		40			40		kHz
Small Signal Bandwidth			1.0			1.0		MHz
Rise Time			0.3	1.5		0.3	1.5	μs
Overshoot			10	30		15	40	%
Settling Time (0.1 %)	ΔV_{IN} = 10V		4.5			4.5		μs
Overload Recovery			4.0			4.0		μs
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 Hz		150			150		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 100 Hz		55			55		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 1 kHz		35			35		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 kHz		30			30		nV/√Hz
Input Noise Voltage	BW = 10 Hz to 10 kHz, R_S = 10 kΩ		12			12		μVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

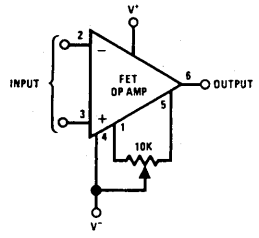
Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.

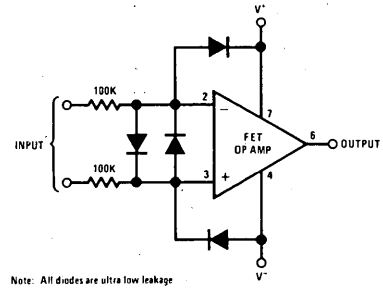
Note 3: Unless otherwise specified, these specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq \pm 125°C$ for the LH0022 and LH0052 and $-25°C \leq T_A \leq +85°C$ for the LH0022C and LH0052C Typical values are given for $T_A = 25°C$.

Note 4: Input currents are a strong function of temperature. Due to high speed testing they are specified a junction temperature $T_j = 25°C$, self heating will cause an increase in current in manual tests.

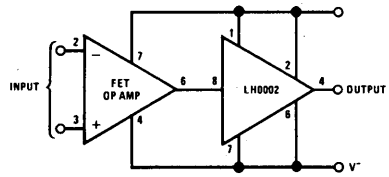
Auxiliary Circuits (Shown for TO-5 pin out)



Offset Null

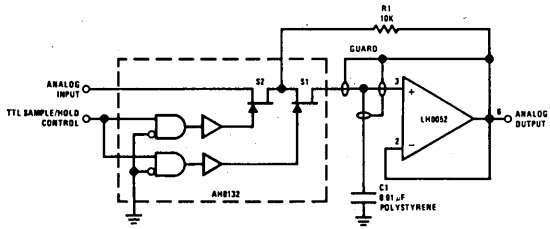


Protecting Inputs From ±150V Transients

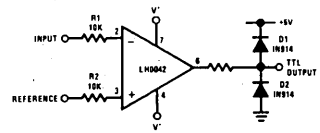


Boosting Output Drive to ±100 mA

Typical Applications

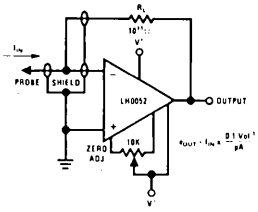


Low Drift Sample and Hold

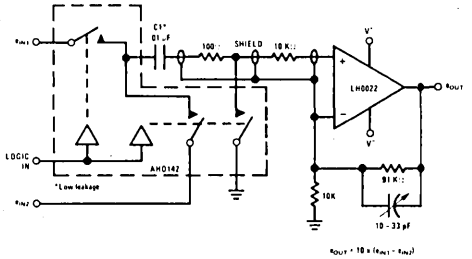


Precision Voltage Comparator

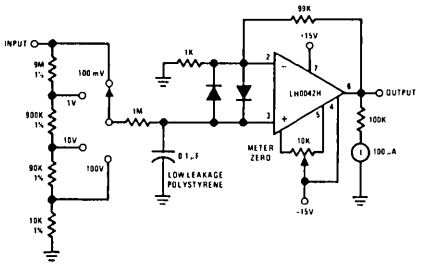
Typical Applications (Cont'd)



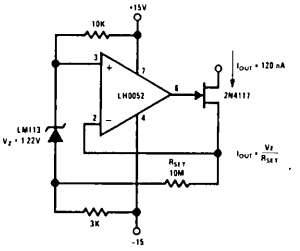
Picoamp Amplifier for pH Meters and Radiation Detectors



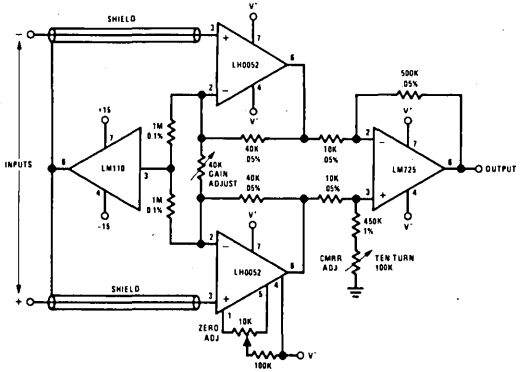
Precision Subtractor for Automatic Test Gear



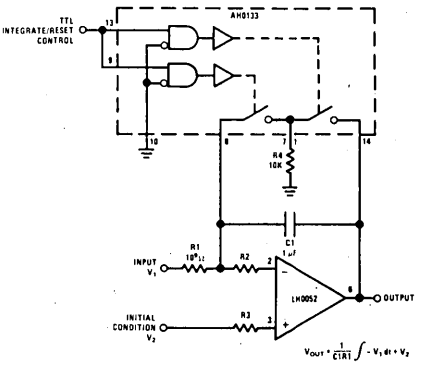
Sensitive Low Cost "VTVM"



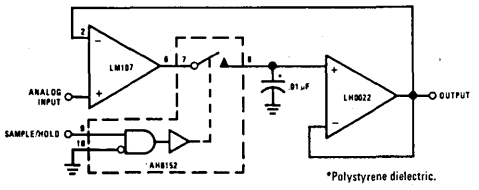
Ultra Low Level Current Source



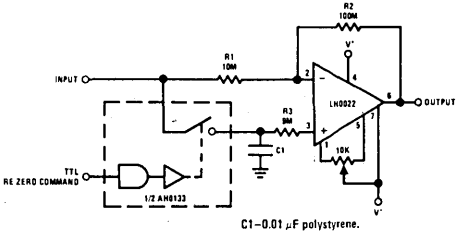
True Instrumentation Amplifier



Precision Integrator



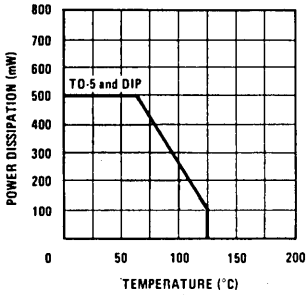
Precision Sample and Hold



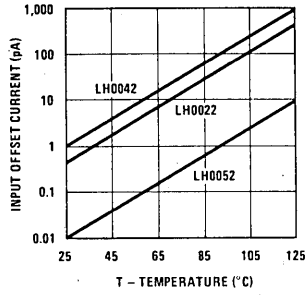
Re-Zeroing Amplifier

Typical Performance Characteristics

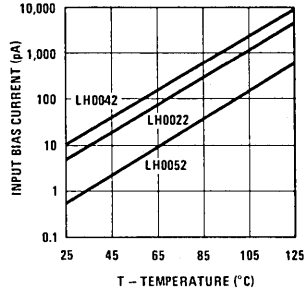
Maximum Power Dissipation



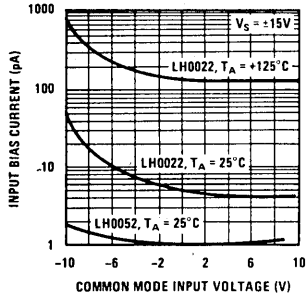
Input Offset Current vs Temperature



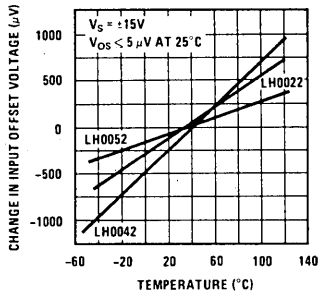
Input Bias Current vs Temperature



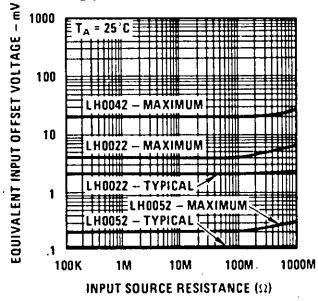
Input Bias Current vs Input Voltage



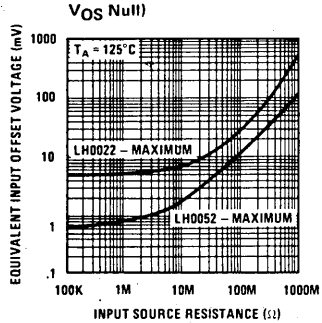
Input Offset Voltage vs Temperature



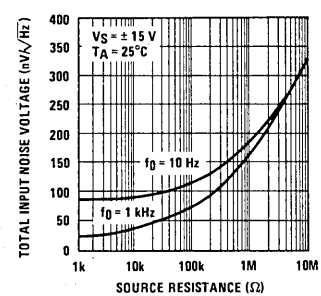
Offset Error (Without V_{OS} Null)



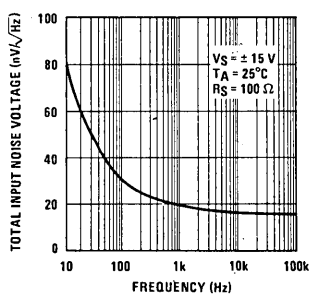
Offset Error (Without V_{OS} Null)



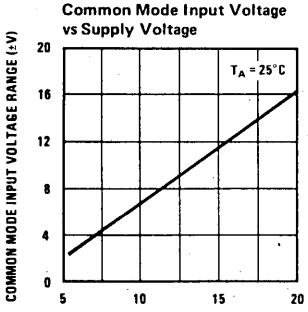
Total Input Noise Voltage* vs Source Resistance



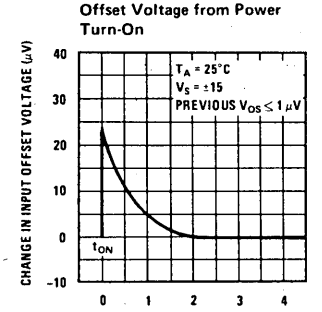
Total Input Noise Voltage* vs Frequency



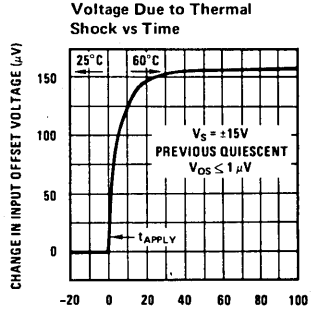
Common Mode Input Voltage vs Supply Voltage



Stabilization Time of Input Offset Voltage from Power Turn-On



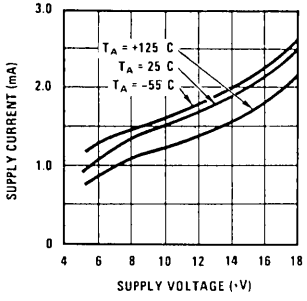
Change in Input Offset Voltage Due to Thermal Shock vs Time



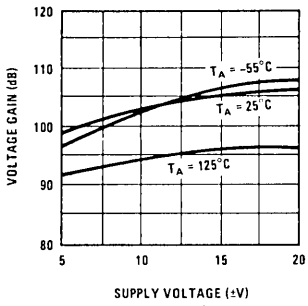
*Noise Voltage Includes Contribution from Source Resistance

Typical Performance Characteristics (Cont'd)

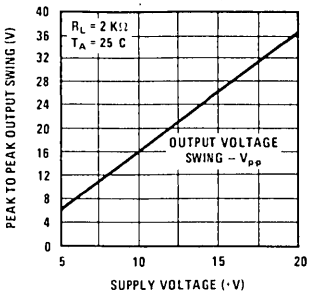
Supply Voltage vs Supply Current



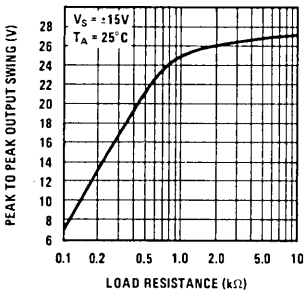
Voltage Gain



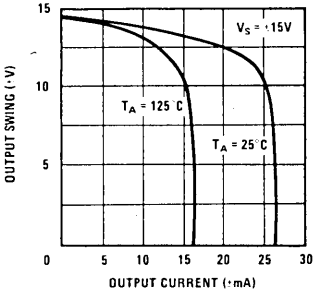
Output Swing vs Supply Voltage



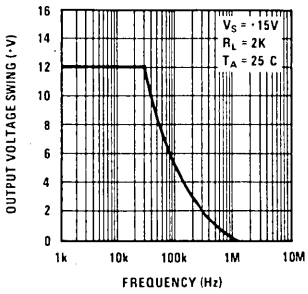
Output Voltage Swing vs Load Resistance



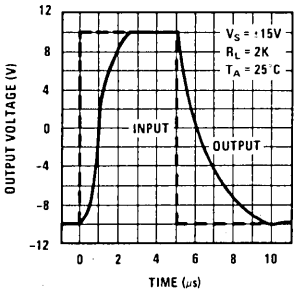
Current Limiting



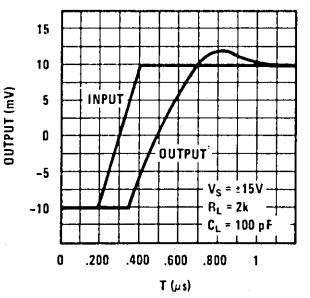
Output Voltage Swing vs Frequency



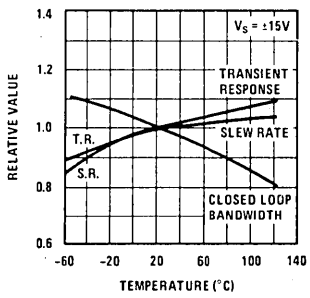
Voltage Follower Large Signal Response



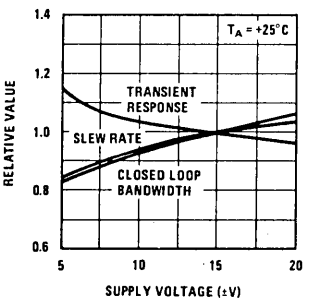
Transient Response



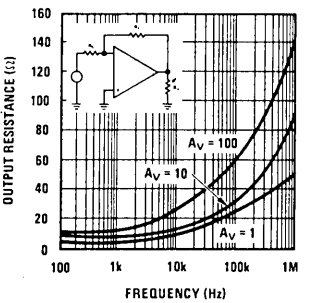
Frequency Characteristics vs Ambient Temperature



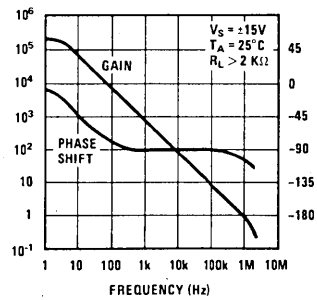
Frequency Characteristics vs Supply Voltage



Output Resistance vs Frequency



Open Loop Transfer Characteristics vs Frequency



National Semiconductor

LH0024/LH0024C High Slew Rate Operational Amplifier

General Description

The LH0024/LH0024C is a very wide bandwidth, high slew rate operational amplifier intended to fulfill a wide variety of high speed applications such as buffers to A to D and D to A converters and high speed comparators. The device exhibits useful gain in excess of 50 MHz making it possible to use in video applications requiring higher gain accuracy than is usually associated with such amplifiers.

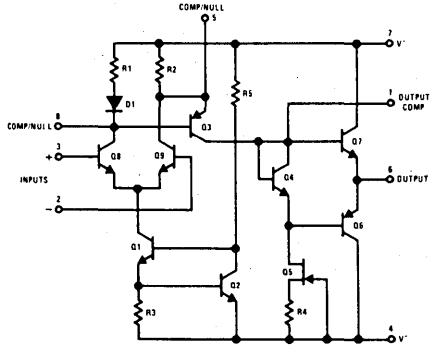
Features

- Very high slew rate — 500 V/μs at Av = +1
- Wide small signal bandwidth — 70 MHz
- Wide large signal bandwidth — 15 MHz
- High output swing — ±12V into 1K
- Offset null with single pot
- Low input offset — 2 mV
- Pin compatible with standard IC op amps

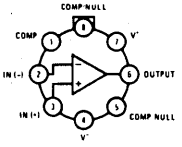
The LH0024/LH0024C's combination of wide bandwidth and high slew rate make it an ideal choice for a variety of high speed applications including active filters, oscillators, and comparators as well as many high speed general purpose applications.

The LH0024 is guaranteed over the temperature range -55°C to +125°C, whereas the LH0024C is guaranteed -25°C to +85°C.

Schematic and Connection Diagrams



Metal Can Package

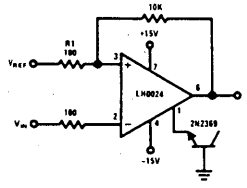


Note: For heat sink use Thermalloy 2230-5 series.

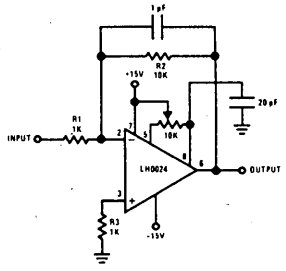
Order Number LH0024H or LH0024CH
See Package H08B

Typical Applications

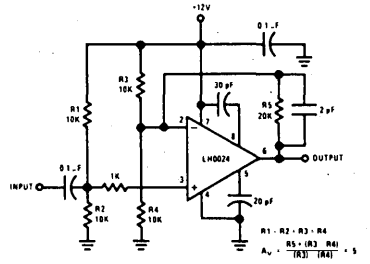
TTL Compatible Comparator



Offset Null



Video Amplifier



Absolute Maximum Ratings

Supply Voltage		±18V
Input Voltage		Equal to Supply
Differential Input Voltage		±5V
Power Dissipation		600 mW
Operating Temperature Range	LH0024	-55°C to +125°C
	LH0024C	-25°C to +85°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

DC Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LH0024			LH0024C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		2.0	4.0		5.0	8.0	mV
	$R_S = 50\Omega$			6.0			10.0	mV
Average Temperature Coefficient of Input Offset Voltage	$V_S = \pm15V$, $R_S = 50\Omega$ -55°C to 125°C		-20			-25		µV/°C
Input Offset Current	$T_A = 25°C$		2.0	5.0		4.0	15.0	µA
				10.0			20.0	µA
Input Bias Current	$T_A = 25°C$		15	30		18	40	µA
				40			50	µA
Supply Current			12.5	15		12.5	15	mA
Large Signal Voltage Gain	$V_S = \pm15V$, $R_L = 1k$, $T_A = 25°C$	4	5		3	4		V/mV
	$V_S = \pm15V$, $R_L = 1k$	3			2.5			V/mV
Input Voltage Range	$V_S = \pm15V$	±12	±13		±12	±13		V
Output Voltage Swing	$V_S = \pm15V$, $R_L = 1k$, $T_A = 25°C$	±12	±13		±10	±13		V
	$V_S = \pm15V$, $R_L = 1k$	±10			±10			V
Slew Rate	$V_S = \pm15V$, $R_L = 1k$, $C_1 = C_2 = 30$ pF $A_V = +1$, $T_A = 25°C$	400	500		250	400		V/µs
Common Mode Rejection Ratio	$V_S = \pm15V$, $\Delta V_{IN} = \pm10V$ $R_S = 50\Omega$		60			60		dB
Power Supply Rejection Ratio	$\pm5V \leq V_S \leq \pm18V$ $R_S = 50\Omega$		60			60		dB

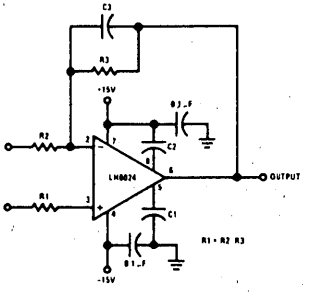
Note 1: These specifications apply for $V_S = \pm15V$ and -55°C to +125°C for the LH0024 and -25°C to +85°C for the LH0024C.

Frequency Compensation

TABLE I

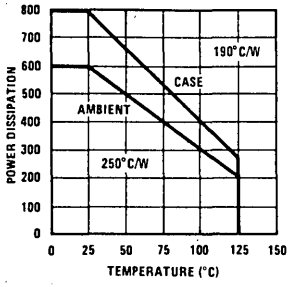
CLOSED LOOP GAIN	C_1	C_2	C_3
100	0	0	0
20	0	0	0
10	0	20 pF	1 pF
1	30 pF	30 pF	3 pF

Frequency Compensation Circuit

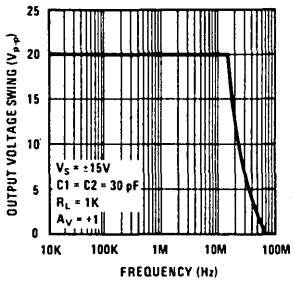


Typical Performance Characteristics

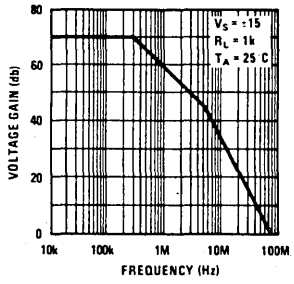
Maximum Power Dissipation



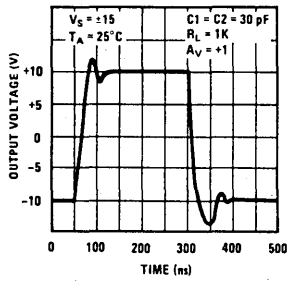
Large Signal Frequency Response



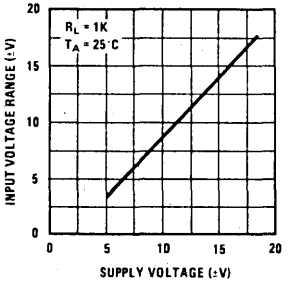
Open Loop Frequency Response



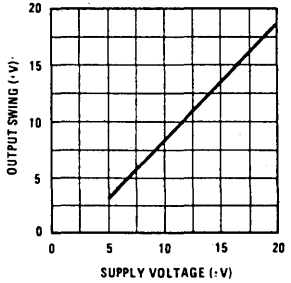
Voltage Follower Pulse Response



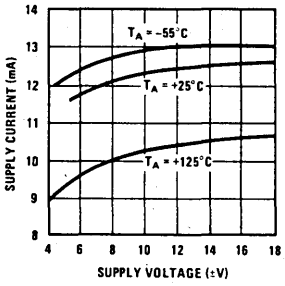
Input Voltage vs Supply Voltage



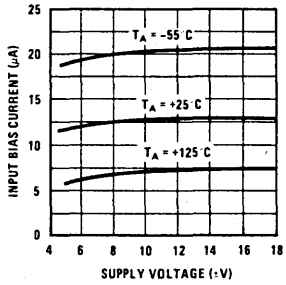
Output Voltage Swing



Supply Current vs Supply Voltage



Input Bias Current vs Voltage



Applications Information

1. Layout Considerations

The LH0024/LH0024C, like most high speed circuitry, is sensitive to layout and stray capacitance. Power supplies should be by-passed as near the device as is practicable with at least .01 μF disc type capacitors. Compensating capacitors should also be placed as close to device as possible.

2. Compensation Recommendations

Compensation schemes recommended in Table 1 work well under typical conditions. However, poor layout and long lead lengths can degrade the performance of the LH0024 or cause the device to oscillate. Slight adjustments in the values for C1, C2, and C3 may be necessary for a given layout. In particular, when operating at a gain of −1, C3 may require adjustment in order to perfectly cancel the input capacitance of the device.

When operating the LH0024/LH0024C at a gain of +1, the value of R1 should be at least 1K ohm.

The case of the LH0024 is electrically isolated from the circuit; hence, it may be advantageous to drive the case in order to minimize stray capacitances.

3. Heat Sinking

The LH0024/LH0024C is specified for operation without the use of an explicit heat sink. However, internal power dissipation does cause a significant temperature rise. Improved offset voltage drift can be obtained by limiting the temperature rise with a clip-on heat sink such as the Thermalloy 2228B or equivalent.

National Semiconductor

LH0032/LH0032C Ultra Fast FET Operational Amplifier

General Description

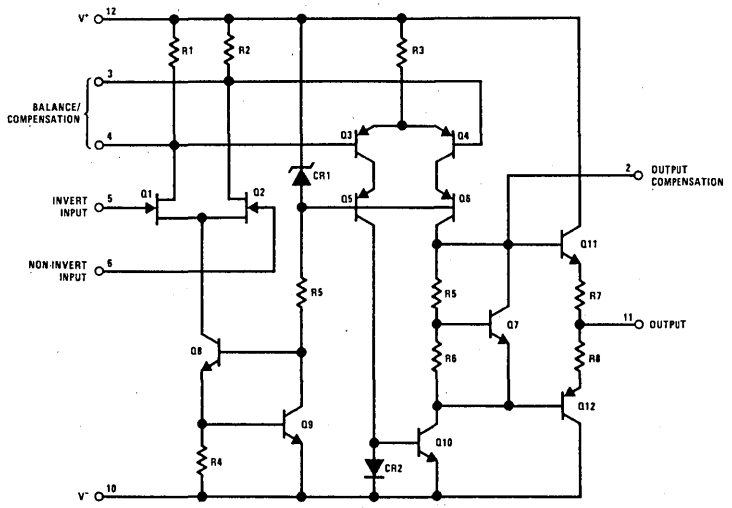
The LH0032/LH0032C is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

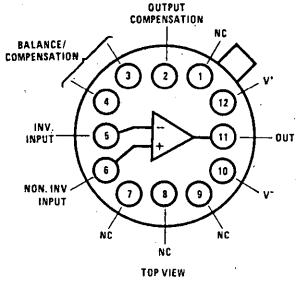
Features

- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- 5 mV max. input offset voltage
- FET input
- Offset null with single pot
- No compensation for gains above 50
- Peak output current to 100 mA

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A's, buffers in data acquisition systems, and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 is guaranteed over the temperature range −55°C to +125°C and the LH0032C is guaranteed from −25°C to +85°C.

Schematic and Connection Diagrams





Order Number LH0032G or LH0032CG
See NS Package H12B

Absolute Maximum Ratings

Supply Voltage, V_S	±18V
Input Voltage, V_{IN}	$\pm V_S$
Differential Input Voltage	±30V or $\pm 2V_S$
Power Dissipation, P_D	
$T_A = 25°C$	1.5W, derate 100°C/W to 125°C (Note 1)
$T_C = 25°C$	2.2W, derate 70°C/W to 125°C (Note 1)
Operating Temperature Range, T_A	
LH0032G	−55°C to +125°C
LH0032CG	−25°C to +85°C
Operating Junction Temperature, T_J	175°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

DC Electrical Characteristics

$V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted

Parameter		Test Conditions		LH0032G			LH0032CG			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input Offset Voltage	$V_{IN} = 0$	$T_A = T_J = 25°C$ (Note 2)		2	5 10		2	15 20	mV
$\Delta V_{OS}/\Delta T$	Average Offset Voltage Drift				25			25		µV/°C
I_{OS}	Input Offset Current		$T_J = 25°C$ (Note 2) $T_A = 25°C$ (Note 3) $T_J = T_A = T_{MAX}$			25 250 25			50 500 5	pA pA nA
I_B	Input Bias Current		$T_J = 25°C$ (Note 2) $T_A = 25°C$ (Note 3) $T_J = T_A = T_{MAX}$			100 1 50			500 5 15	pA nA nA
V_{INCM}	Input Voltage Range			±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = 10V$		50	60		50	60		dB
A_{VOL}	Open-Loop Voltage Gain	$V_O = \pm 10V$, $f = 1kHz$	$T_J = 25°C$	60	70		60	70		dB
		$R_L = 1k\Omega$		57			57			
V_O	Output Voltage Swing	$R_L = 1k\Omega$		±10	±13.5		±10	±13		V
I_S	Power Supply Current	$T_J = 25°C$, $I_O = 0$			18	20		20	22	mA
PSRR	Power Supply Rejection Ratio	$\Delta V_S = 10V$		50	60		50	60		dB

AC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 1k\Omega$, $T_J = 25°C$

Parameter		Conditions		Min.	Typ.	Max.	Units
S_R	Slew Rate	$A_V = +1$	$\Delta V_{IN} = 20V$	350	500		V/µs
t_S	Settling Time to 1% of Final Value	$A_V = -1$,			100		ns
t_S	Settling Time to 0.1% of Final Value				300		
t_R	Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$			8	20	
t_D	Small Signal Delay time				10	25	

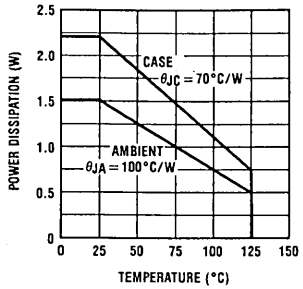
Note 1: In order to limit maximum junction temperature to +175°C, it may be necessary to operate with $V_S < \pm 15V$ when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation. See Applications Notes AN277, "Applications of Wide-Band Buffer Amplifiers" and AN253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

Note 2: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

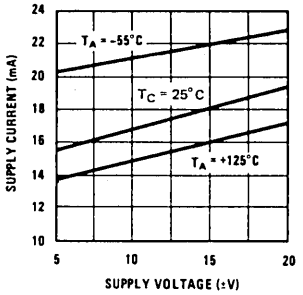
Note 3: Measured in still air 7 minutes after application of power.

Typical Performance Characteristics

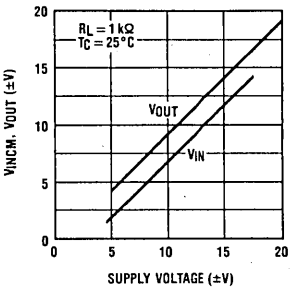
Maximum Power Dissipation



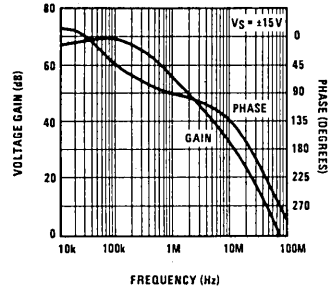
Supply Current vs. Supply Voltage



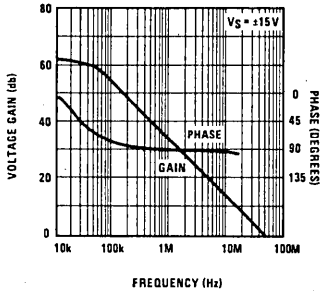
Input Voltage Range and Output Voltage vs. Supply Voltage



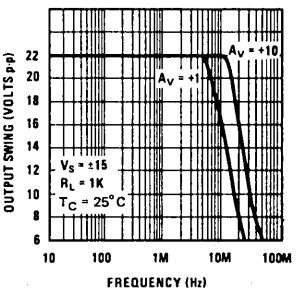
Bode Plot (Uncompensated)



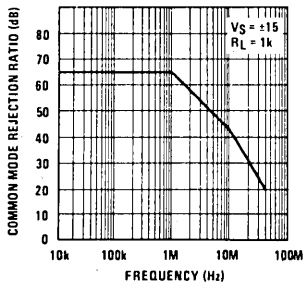
Bode Plot (Unity Gain Compensation)



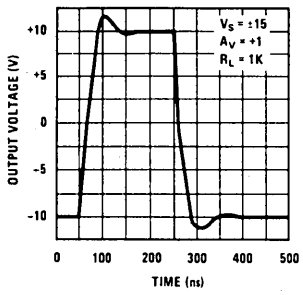
Large Signal Frequency Response



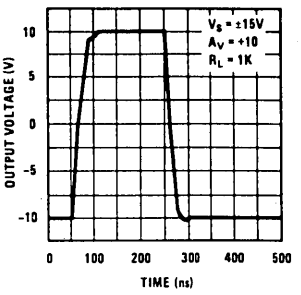
Common Mode Rejection Ratio vs. Frequency



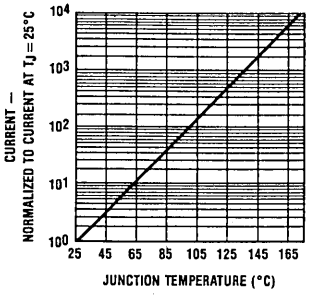
Large Signal Pulse Response



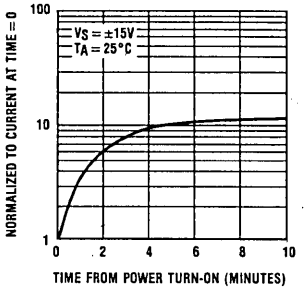
Large Signal Pulse Response



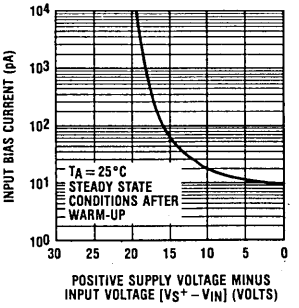
Normalized Input Bias and Offset Current vs. Junction Temperature



Normalized Input Bias Current During Warm-Up

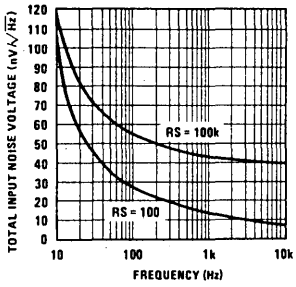


Input Bias Current vs. Input Voltage

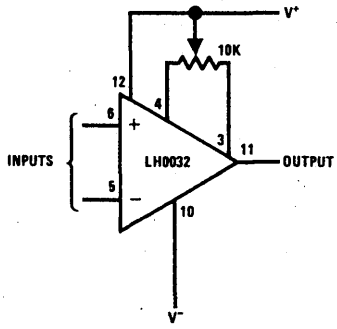


Auxiliary Circuits

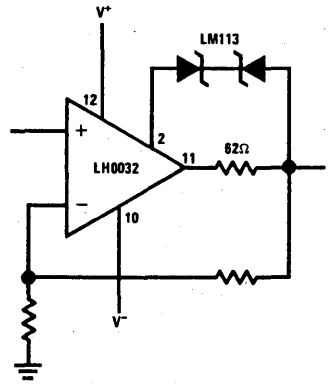
Total Input Noise Voltage vs. Frequency*



Offset Null



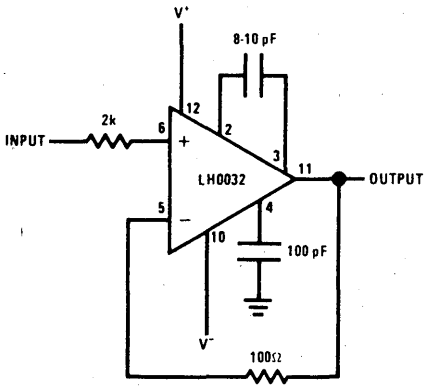
Output Short Circuit Protection



* Noise voltage includes contribution from source resistance.

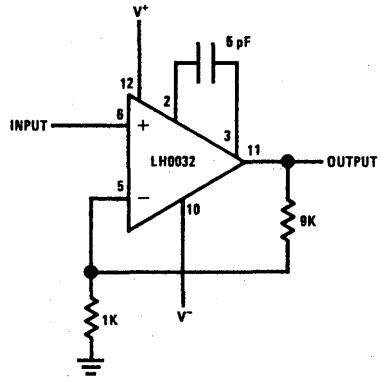
Typical Applications

Unity Gain Amplifier



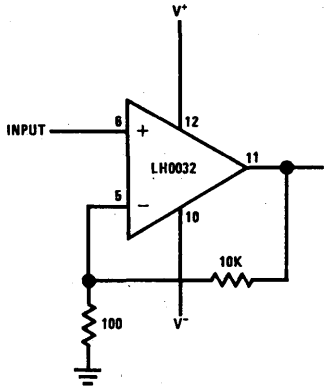
TYP. $BW_{3dB} = 45$ MHz

10X Buffer Amplifier



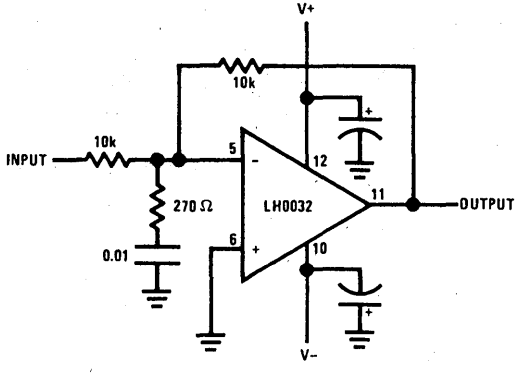
TYP. $BW_{3dB} = 10$ MHz

100X Buffer Amplifier



TYP. $BW_{3dB} = 5$ MHz

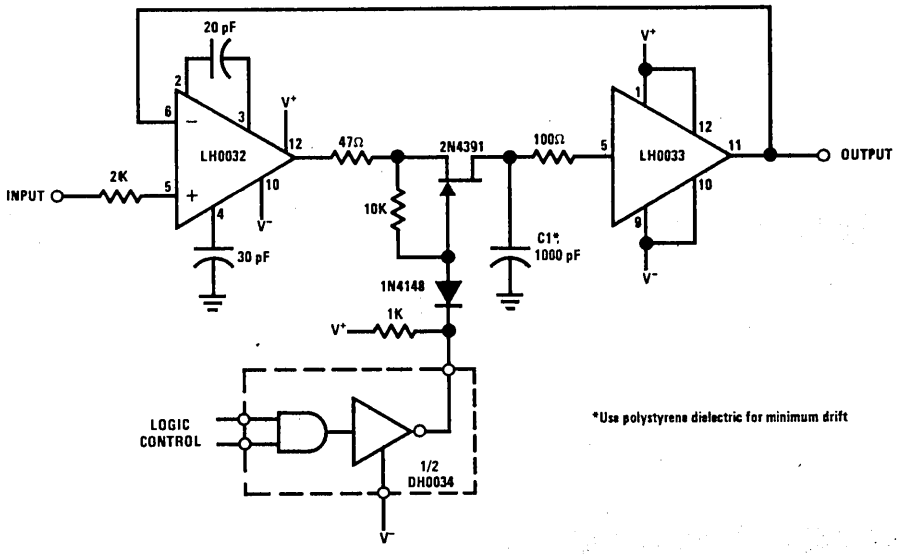
Non-Compensated Unity Gain Inverter



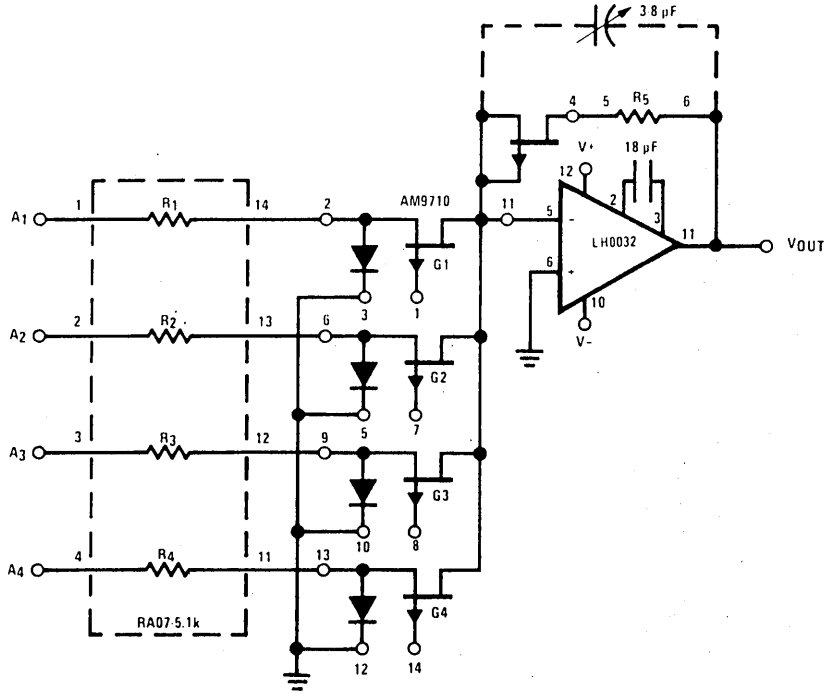
TYP. $BW_{3dB} = 70$ MHz

Typical Applications (cont'd)

High Speed Sample and Hold



High Speed Current Mode MUX



Applications Information

Power Supply Decoupling

The LH0032/LH0032C, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be by-passed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

Input Current

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40-60°C above free-air ambient temperature when supplies are ±15V. The device temperature will stabilize within 5-10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels. This effect will be noted as the input voltage of the LH0032 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

Input Capacitance

The input capacitance to the LH0032/LH0032C is typically 5pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

Heat Sinking

While the LH0032/LH0032C is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

For additional applications information see Application Note AN-253.

National Semiconductor

LH0044 Series Precision Low Noise Operational Amplifiers

General Description

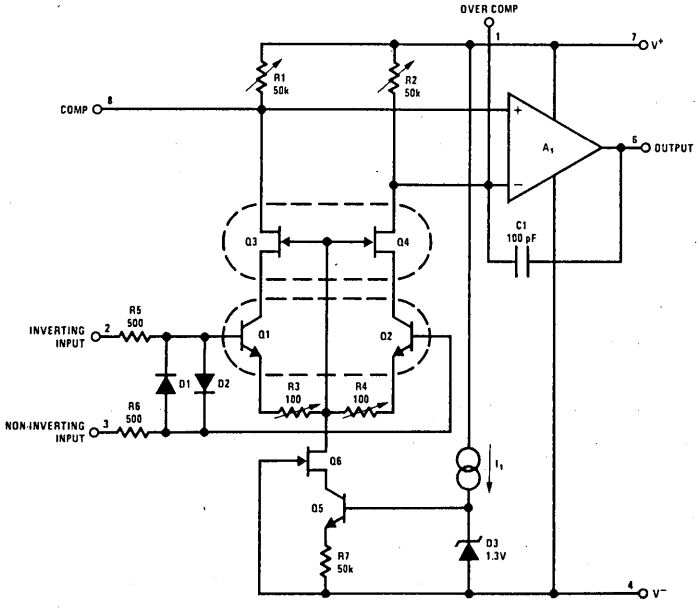
The LH0044 Series is a low noise, ultra-stable, high gain, precision operational amplifier family intended to replace either chopper-stabilized monolithic or modular amplifiers. The devices are particularly suited for differential mode, inverting, and non-inverting mode applications requiring very low initial offset, low offset drift, very high gain, high CMRR, and high PSRR. In addition, the LH0044 Series' low initial offset and offset drift eliminate costly and time consuming null adjustments at the systems level. The superior performance afforded by the LH0044 Series is made possible by advanced processing and testing techniques, as well as active laser trim of critical metal film resistors to minimize offset voltage and drift. Unique construction eliminates thermal feedback effects.

The LH0044 Series is an excellent choice for a wide range of precision applications including strain gauge bridges, thermocouple amplifiers, and ultrastable reference amplifiers. The LH0044 and LH0044A are guaranteed over the temperature range of −55°C to +125°C, and the LH0044AC, LH0044B, and LH0044C are guaranteed from −25°C to +85°C. The device is available in standard TO-5 op amp pin out and is compatible with LM108A, LM725, and LM741 type amplifiers.

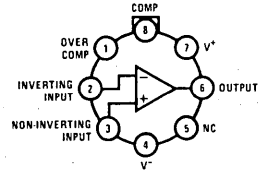
Features

- Low input offset voltage — 25μV max
- Excellent long-term stability — ±1μV/month max
- Low offset drift — 0.5μV/°C max
- Very low noise — 0.7μVp-p max 0.1 Hz to 10 Hz
- High CMRR and PSRR — 120 dB min
- High open loop gain — 120 dB min
- Wide common-mode range — ±13V min
- Wide supply voltage range — ±2V to ±20V

Equivalent Circuit and Connection Diagram



Metal Can Package



TOP VIEW

Case is electrically isolated

Note: Compensation is not normally required. However, for maximum stability, a 0.01μF capacitor should be placed between pins 7 and 8 when device is used below closed loop gains of 10.

Order Number LH0044H, LH0044AH, LH0044CH, LH0044ACH, LH0044BH
See Package H08B

Absolute Maximum Ratings

Supply Voltage	±20V	Operating Temperature Range	
Power Dissipation	600 mW	LH0044, LH0044A	−55°C to +125°C
Differential Input Voltage (Note 4)	±1V	LH0044AC, LH0044B, LH0044C	−25°C to +85°C
Input Voltage (Note 5)	±15V	Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Continuous	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0044A/LH0044AC			LH0044/LH0044B/LH0044C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S = 50\Omega$, $V_{CM} = 0V$		8	25		12	50	µV
	LH0044C Only						100	µV
Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$			55			180	µV
	LH0044A and LH0044B Only			75			80	µV
Average Input Offset Voltage Drift	$T_{MIN} \leq T_A \leq T_{MAX}$		0.1	0.5		0.2	1.3	µV/°C
	LH0044B Only						0.5	µV/°C
Long-Term Stability	(Note 2)		0.2	1		0.3	2	µV/month
Input Noise Voltage (Note 3)	BW = 0.1 Hz to 10 Hz, $R_S = 50\Omega$		0.35	0.7		0.35	0.8	µVp-p
	R_S = 10 kΩ Imbalance		0.50	0.9		0.50	1.0	µVp-p
Thermal Feedback Coefficient			0.005			0.005		µV/mW
Open Loop Voltage Gain	R_L = 10 kΩ	120	145		114	140		dB
Common-Mode Rejection Ratio	$-10V \leq V_{CM} \leq +10V$	120	145		114	140		dB
Power Supply Rejection Ratio	$\pm 3V \leq V_S \leq \pm 18V$	120	145		114	140		dB
Input Voltage Range		±13	±13.8		±12	±13.5		V
Output Voltage Swing	R_L = 10 kΩ	±13	±13.7		±12	±13.5		V
Input Offset Current	$25°C \leq T_A \leq T_{MAX}$		1.0	2.5		1.5	5.0	nA
	$T_{MIN} \leq T_A < 25°C$			5.0			10.0	nA
Average Input Offset Current Drift			5	40		15	80	pA/°C
Input Bias Current	$25°C \leq T_A \leq T_{MAX}$		8.5	15		10	30	nA
	$T_{MIN} \leq T_A < 25°C$			50			100	nA
Average Input Bias Current Drift			50	300		100	600	pA/°C
Differential Input Impedance		5	10		2.5	8		MΩ
Common-Mode Input Impedance			2×10^{11}			2×10^{11}		Ω
Supply Current	$I_L = 0$		0.9	3.0		1.0	4.0	mA
Power Dissipation			27	90		30	120	mW

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm 15V$

PARAMETER	CONDITIONS	TYP	UNITS
Input Noise Voltage	$R_S = 1\ k\Omega$, $f_O = 10$ Hz	11	$nV/\sqrt{Hz}$
	$R_S = 1\ k\Omega$, $f_O = 1$ kHz	9	$nV/\sqrt{Hz}$
Slew Rate	$A_V = +1$, $R_L = 10\ k\Omega$, $V_{IN} = \pm 10V$	0.06	V/µs
Large Signal Bandwidth	$A_V = +1$, $R_L = 10\ k\Omega$, $V_{IN} = \pm 10V$	1	kHz
Overload Recovery Time	$A_V = +100$, $V_{IN} = -100$ mV, $\Delta V_{IN} = 200$ mV	5	µs
Small Signal Bandwidth	$A_V = +1$, $R_L = 10\ k\Omega$	400	kHz
Small Signal Rise Time	$A_V = +1$, $R_L = 10\ k\Omega$, $V_{IN} = 10$ mV	2.5	µs
Overshoot	$A_V = +1$, $R_L = 10\ k\Omega$, $V_{IN} = 10$ mV, $C_L = 100$ pF	10	%

Note 1: All specifications apply for all device grades, at $V_S = \pm 15V$, and from T_{MIN} to T_{MAX} unless otherwise specified. T_{MIN} is −55°C and T_{MAX} is +125°C for the LH0044A and LH0044. T_{MIN} is −25°C and T_{MAX} is +85°C for the LH0044AC, LH0044B and LH0044C. Typicals are given for $T_A = 25°C$.

Note 2: This parameter is not 100% tested; however, 90% of the devices are guaranteed to meet this specification after one month of operation and after initial turn-on stabilization.

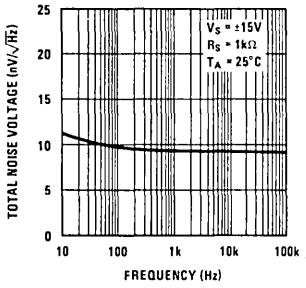
Note 3: Noise is 100% tested on the LH0044A, LH0044AC and LH0044B only. 90% of the LH0044 and LH0044C devices are guaranteed to meet this specification.

Note 4: The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow for differential input voltages in excess of 1V. Input current should be limited to less than 1 mA.

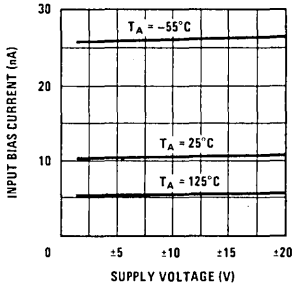
Note 5: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Typical Performance Characteristics

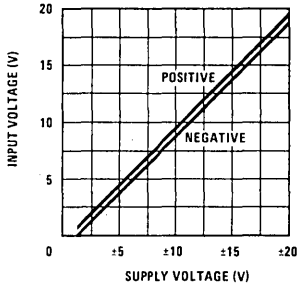
Total Input Noise Voltage vs Frequency



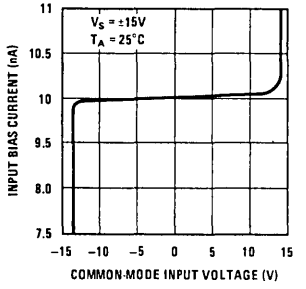
Input Bias Current



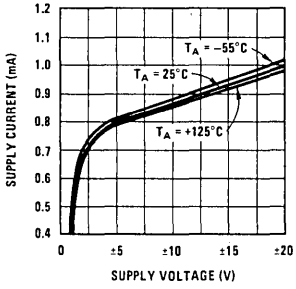
Input Voltage Range



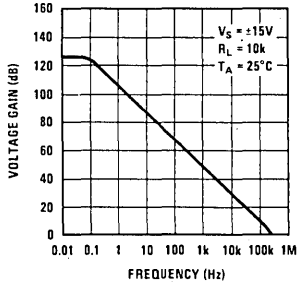
Input Bias Current vs Common-Mode Input Voltage



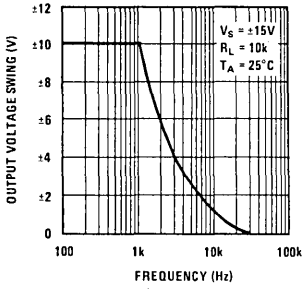
Supply Current vs Supply Voltage



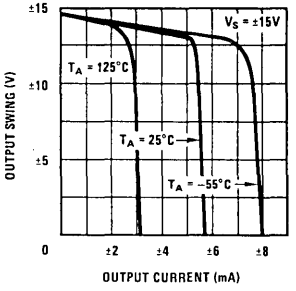
Open Loop Frequency Response



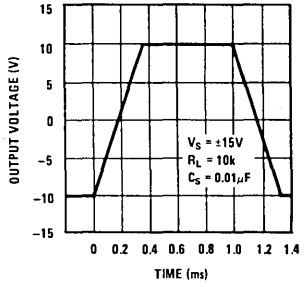
Large Signal Voltage Response



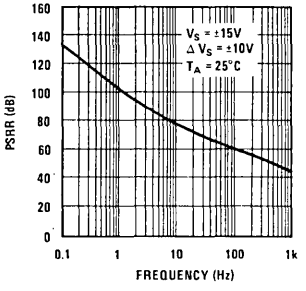
Output Swing



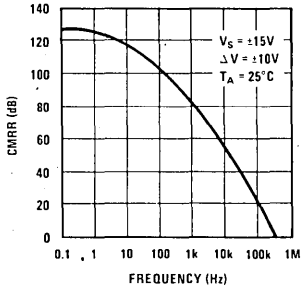
Large Signal Pulse Response



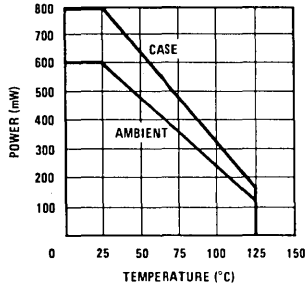
Power Supply Rejection Ratio vs Frequency



CMRR vs Frequency



Maximum Power Dissipation



Applications Information

LOW DRIFT CONSIDERATIONS

Achieving ultra-low drift in practical applications requires strict attention to board layout, thermocouple effects, and input guarding. For specific recommendations refer to AN-63 and AN-79.

A point worth stressing with regard to low drift specifications is testing of the LH0044. Simply stated—it is virtually impossible to test the device using a thermoprobe or other form of local heating. A one degree centigrade temperature gradient can account for tens of microvolts of virtual offset (or drift). The test circuit of *Figure 1* is recommended for use in a stabilized oven or continuously stirred oil bath with the entire circuit inside the oven or bath. Isothermal layout of the resistors is advised in order to minimize thermocouple induced EMF's.

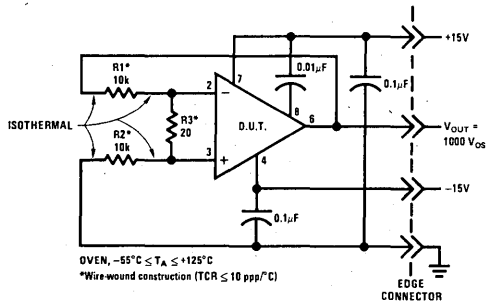


FIGURE 1. LH0044 Temperature Test Circuit

OVER COMPENSATION

The LH0044 may be overcompensated in order to minimize noise bandwidth by paralleling the internal 100 pF capacitor with an external capacitor connected between pins 1 and 6. Unity gain frequency may be predicted by:

$$f = \frac{4 \times 10^{-5}}{100\ pF + C_{ext}\ pF}\ (Hz)$$

COMPENSATION

For closed loop gains in excess of 10, no external components are required for frequency stability. However, for gains of 10 or less, a 0.01μF disc capacitor is recommended between pin 7 (V^+) and pin 8 (Comp). An improvement in ac PSRR will also be realized by use of the 0.01μF capacitor.

OFFSET NULL

In general, further nulling of LH0044 is neither necessary nor recommended. For most applications the specified initial offset is sufficient.

However, for those applications requiring additional null, an obvious temptation might be to place a pot between pins 1 and 8 with the wiper returned to V^+. This technique will usually result in reduced gain and increased offset drift due to mismatch in the TCR of the pot and R1 and R2. The technique is, therefore, not generally recommended.

The recommended technique for offset nulling the LH0044 is shown in *Figure 2.* Null is accomplished in A_2 and all errors are divided by the closed loop gain of the LH0044. Additional offset and drift incurred due to use of A_2 is less than 1μV/V for V^+ and V^- changes and 0.01μV/°C drift for the values shown in *Figure 2.*

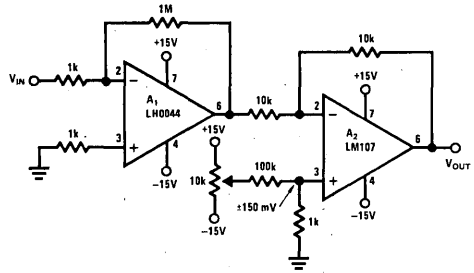
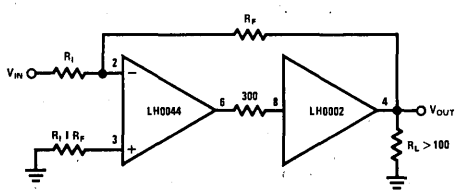
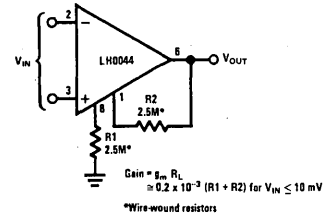


FIGURE 2. LH0044 Null Technique

Typical Applications

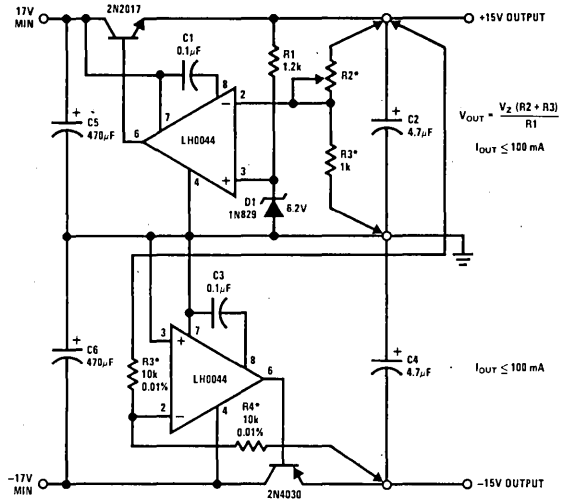


Buffered Output for Heavy Loads



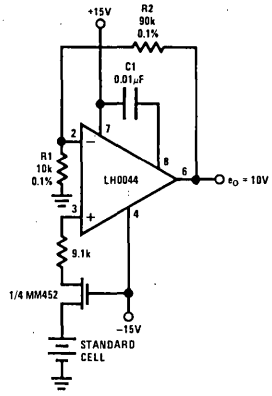
X1000 Instrumentation Amp

Typical Applications (Continued)

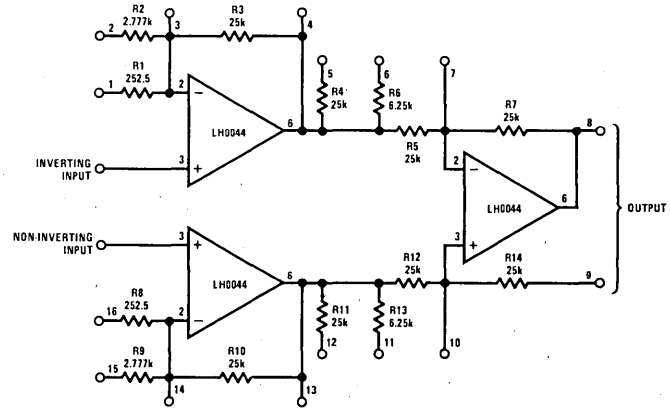


*Wire-wound for minimum drift.
Line and load regulation ≤ 0.005%

Precision Dual Tracking Regulator



10V Reference Supply

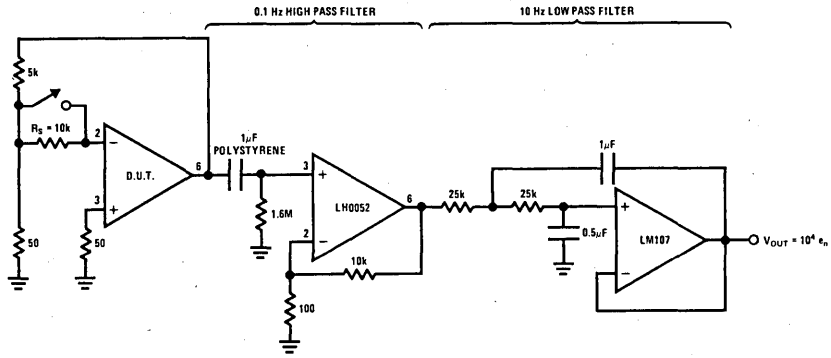


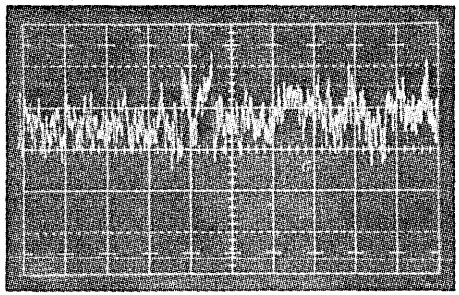
All resistors are part of National's RA201 resistor array.

OVERALL GAIN	INPUT STAGE GAIN	OUTPUT STAGE GAIN	JUMPER PINS ON RA201
X1	X1	X1	
X2	X1	X2	5 to 7, 12 to 10
X5	X1	X5	6 to 7, 11 to 10
X10	X10	X1	2 to 15
X20	X10	X2	2 to 15, 5 to 7, 12 to 10
X50	X10	X5	2 to 15, 6 to 7, 11 to 10
X100	X100	X1	1 to 16
X200	X100	X2	1 to 16, 5 to 7, 12 to 10
X500	X100	X5	1 to 16, 6 to 7, 11 to 10
X995	X199	X5	1 to 14, 6 to 7, 11 to 10

Precision Instrumentation Amplifier

Noise Test Circuit





VERT: 200 nV/DIV
HORIZ: 5 SEC/DIV

LH0045/LH0045C Two Wire Transmitter

General Description

The LH0045/LH0045C Two Wire Transmitters are linear integrated circuits designed to convert the voltage from a sensor to a current, and send it through to a receiver, utilizing the same simple twisted pair as the supply voltage.

The LH0045 and LH0045C contain an internal reference designed to power the sensor bridge, a sensitive input amplifier, and an output current source. The output current scale can be adjusted to match the industry standards of 4.0 mA to 20 mA or 10 mA to 50 mA.

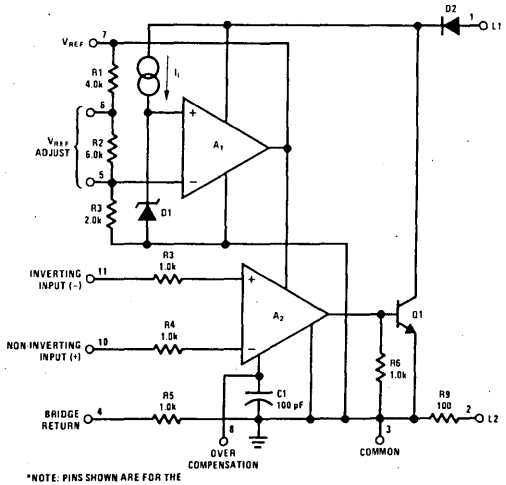
Designed for use with various sensors, the LH0045/LH0045C will interface with thermocouples, strain gauges, or thermistors. The use of the power supply leads as the signal output eliminates two or three extra wires in remote signal applications. Also, current output minimizes susceptibility to voltage noise spikes and eliminates line drop problems.

Features

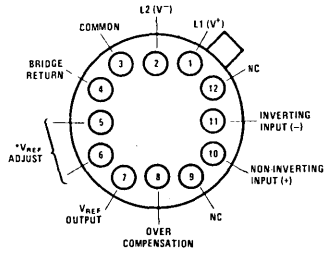
- High sensitivity — $> 10\ \mu A/\mu V$
- Low input offset voltage — 1.0 mV
- Low input bias current — 2.0 nA
- Single supply operation — 10V to 50V
- Programmable bridge reference (LH0045G) — 5.0V to 30V
- Non-interactive span and null adjust
- Over compensation capability
- Supply reversal protection

The LH0045/LH0045C is intended to fulfill a wide variety of process control, instrumentation, and data acquisition applications. The LH0045 is guaranteed over the temperature range of −55°C to +125°C; whereas the LH0045C is guaranteed from −25°C to +85°C.

Equivalent Schematic and Connection Diagrams



*NOTE: PINS SHOWN ARE FOR THE 12 PIN TO 8 ("G") PACKAGE.



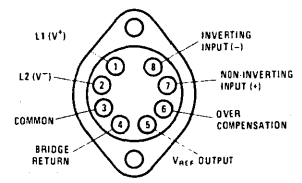
TOP VIEW

*NOTE: PIN 5 IS SHORTED TO PIN 6 TO OBTAIN A NOMINAL +5.1V, V_{REF}. LEFT OPEN V_{REF} = +10V.

THE CASE IS ISOLATED FROM THE CIRCUIT FOR BOTH TO 3 AND TO 8

Order Number LH0045G or LH0045CG
See Package H12B

TO-3



TOP VIEW

Order Number LH0045K or LH0045CK
See Package K08A

Absolute Maximum Ratings

Supply Voltage (L1 to common)	+50V
Input Current	±20 mA
Input Voltage (Either Input to Common)	0V to V_{REF}
Differential Input Voltage	±20 V
Output Current (Either L1 or L2)	50 mA
Reference Output Current	5.0 mA
Power Dissipation	
LH0045G	1.5W
LH0045K	3.0W
Operating Temperature Range	
LH0045	−55°C to +125°C
LH0045C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

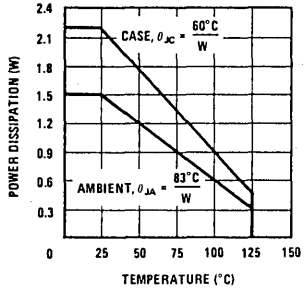
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0045			LH0045C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{OS})	I_S = 4.0 mA, T_A = 25°C		0.7	2.0		2.0	7.5	mV
	I_S = 4.0 mA			3.0			10	mV
Offset Voltage Temperature Coefficient ($\Delta V_{OS}/\Delta T$)	I_S = 4.0 mA		3.0			6.0		µV/°C
Input Bias Current (I_B)	T_A = 25°C		0.8	2.0		1.5	7.0	nA
				3.0			10	nA
Input Offset Current (I_{OS})	T_A = 25°C		0.05	0.2		0.2	1.0	nA
				0.4			1.5	nA
Open Loop Transconductance (g_{MOL})	ΔI_S = 4.0 mA to 20 mA	10^6	10^7		10^6	10^7		µ℧
	ΔI_S = 10 mA to 50 mA	$2x10^6$	$2x10^7$		$2x10^6$	$2x10^7$		µ℧
Supply Voltage Range (V_S)		9.0		50	9.0		50	V
	LH0045G pins 5 and 6 open	15		50	15		50	V
Input Voltage Range (V_{IN})		1.0		3.3	1.0		3.3	V
	LH0045G pins 5 and 6 open	1.0		7.6	1.0		7.6	V
Open Loop Output Impedance (R_{OUT})	V_S = 10V to 45V, I_S = 4.0 mA, T_A = 25°C		1.0			1.0		MΩ
Common Mode Rejection Ratio (CMRR)	ΔV_{IN} = 1.0V to 3.3V, I_S = 12 mA	0.1	0.05		0.1	0.05		mV/V
Power Supply Rejection Ratio (PSRR)	ΔV_S = 10V to 45V, I_S = 12 mA	0.1	0.01		0.1	0.01		mV/V
Open Loop Supply Current (I_{SOL})	V_S = 50V		2.0	3.0		2.0	3.0	mA
Reference Voltage Load Regulation ($\Delta V_{REF}/\Delta I_{REF}$)	ΔI_{REF} = 0 mA to 2.0 mA, T_A = 25°C		0.05	0.2		0.05	0.2	%
Reference Voltage Line Regulation ($\Delta V_{REF}/\Delta V_S$)	ΔV_S = 10V to 45V, T_A = 25°C		0.3	0.5		0.3	0.7	mV/V
Reference Voltage Temperature Coefficient ($\Delta V_{REF}/\Delta T$)	I_{REF} = 2.0 mA		0.004			0.004		%/°C
Reference Voltage (V_{REF})	I_{REF} = 2.0 mA, T_A = 25°C	4.3	5.1	5.9	4.3	5.1	5.9	V
	I_{REF} = 2.0 mA, T_A = 25°C, LH0045G pins 5 and 6 open	8.6	10.3	12	8.6	10.3	12	V
Resistor R9	I_S = 12 mA, T_A = 25°C	95	100	105	95	100	105	Ω
Average Temperature Coefficient of R9 (TCR_9)	I_S = 12 mA		50	300		50	300	PPM/°C
Resistor R5	I_S = 1.0 mA, T_A = 25°C	950	1000	1050	950	1000	1050	Ω
Average Temperature Coefficient of R5 (TCR_5)	I_S = 1.0 mA		50	300		50	300	PPM/°C
Input Resistance (R_{IN})	T_A = 25°C		50			50		MΩ

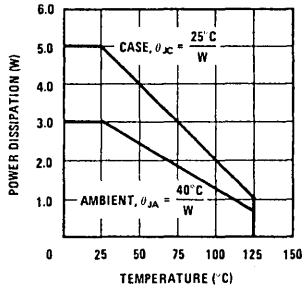
Note 1: Unless otherwise specified, these specifications apply for +10V ≤ V_S ≤ +50V, pin 5 shorted to pin 6 on the LH0045G, over the temperature range −55°C to +125°C for the LH0045 and −25°C to +85°C for the LH0045C.

Typical Performance Characteristics

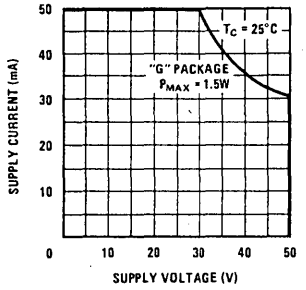
LH0045G Maximum Power Dissipation



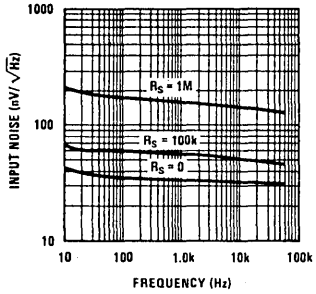
LH0045K Maximum Power Dissipation



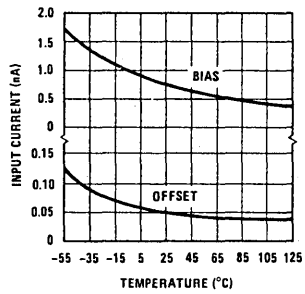
Safe Operating Area



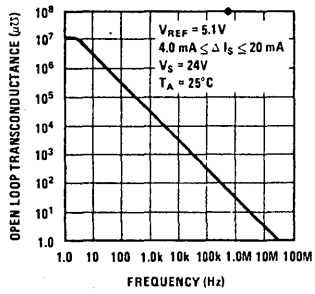
Input Noise Voltage



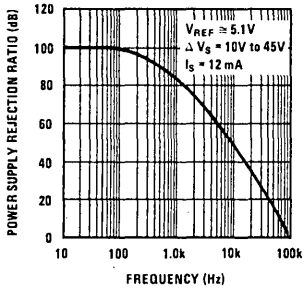
Input Currents



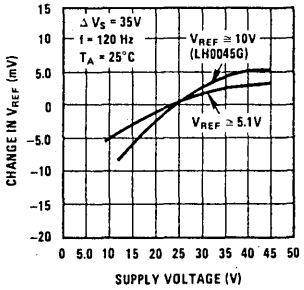
Open Loop Transconductance vs Frequency



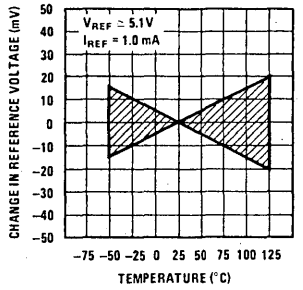
Power Supply Rejection Ratio vs Frequency



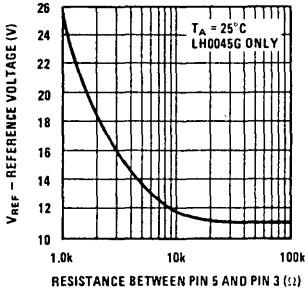
V_{REF} Line Regulation



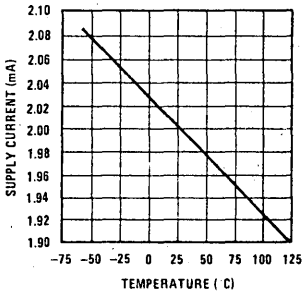
Variation of V_{REF} With Temperature Normalized to 25°C



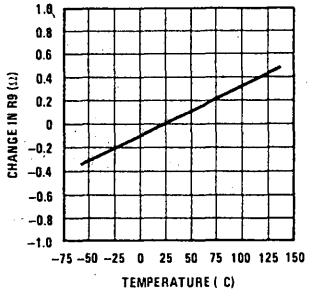
V_{REF} vs Resistance Between Pin 5 and Pin 3



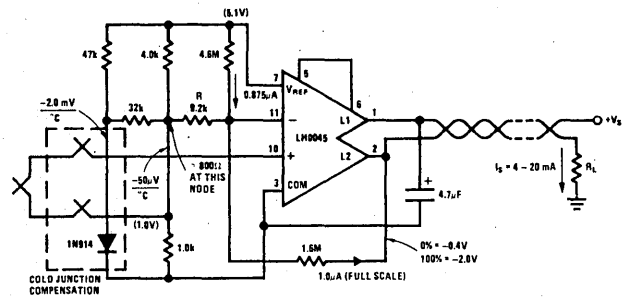
Open Loop Supply Current vs Temperature



Change in R9 With Temperature Normalized to 25°C

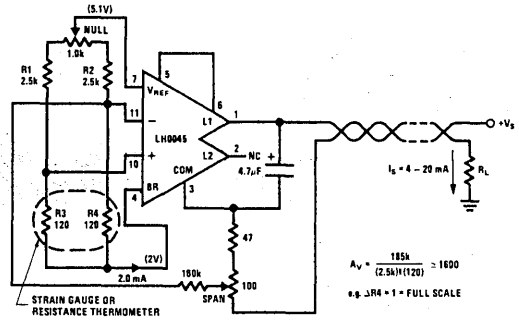


Typical Applications

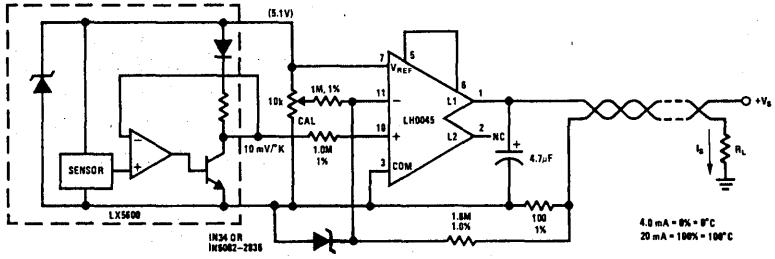


FOR 1μA FULL SCALE, $R_{IN} = V_{IN}/1\mu A$ = SOURCE IMPEDANCE @ PIN 11
e.g., V_{IN} (FULL SCALE) = 10 mV, R_{IN} = 10k
BRIDGE IMPEDANCE = 9.8k, ∴ R = 10k − 0.8k = 9.2k

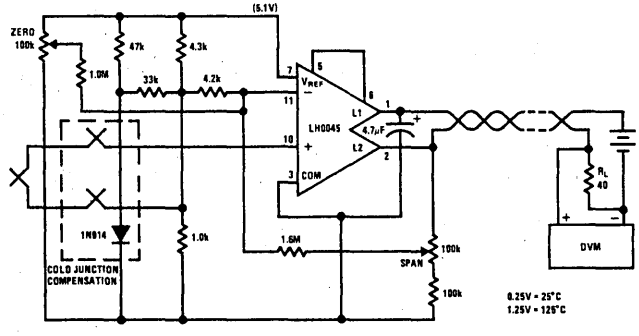
Thermocouple Input Transmitter



Resistance Bridge Input Transmitter



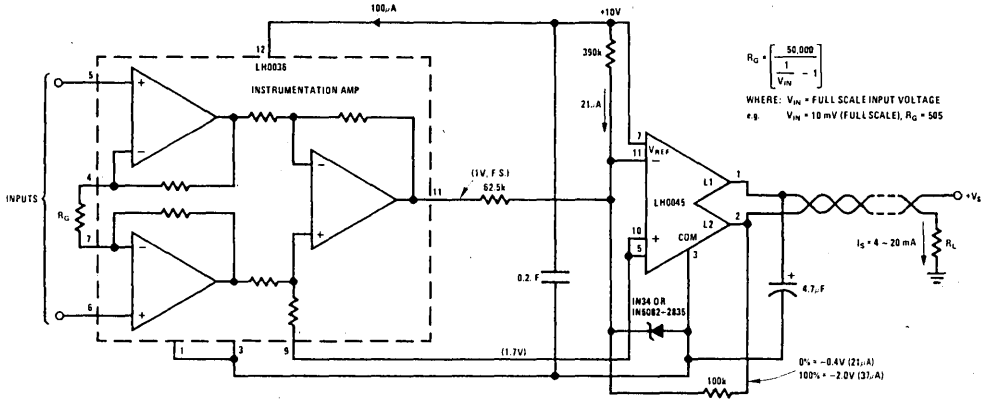
Electronic Temperature Sensor



Remote Sensing Digital Thermometer

*Pin numbers refer to 'G' package. All voltages indicated by ( ) are measured with respect to common, pin 3.

Typical Applications (Cont'd)



*Pin numbers refer to 'G' package. All voltages indicated by ( ) are measured with respect to common, pin 3.

Instrumentation Amplifier Transmitter

Applications Information

CIRCUIT DESCRIPTION AND OPERATION

A simplified schematic of the LH0045/LH0045C is shown in Figure 1. Differential amplifier, A_2 converts very low level signals to an output current via transistor Q1. Reference voltage diode D1 is used to supply voltage for operation of A_2 and to bias an external bridge. Current source I_1 minimizes fluctuation in the bridge reference voltage due to changes in V_S.

In normal operation, the LH0045/LH0045C is used in conjunction with an external bridge comprised of R_{B1} through R_{B4}. The bridge resistors in conjunction with bridge return resistor, R5, bias A_2 in its linear region and sense the input signal; e.g. R_{B4} might be a strain sensitive resistor in a strain gauge bridge. R_T is adjusted to purposely unbalance the bridge for 4.0 mA output (null) for zero signal input. This is accomplished by forcing 2.5μA more through R_{B3} than R_{B4}.

The 2.5μA imbalance causes a voltage rise of (2.5μA) x (100Ω) or 250μV at the top of R_{B3}. Terminal L2 may be viewed as the output of an op amp whose closed loop gain is approximately R_F/R_{B3} = 1600.

The 250μV rise at the top of R_{B3} causes a voltage drop of (1600) x (250μV) or −0.4V across R9. An output current, I_S, equal to 0.4V/R9 or 4.0 mA is thus established in Q1. If R_{B4} is now decreased by 1.0Ω (due to application of a strain force), a −1.0 mV change in input voltage will result. This causes L2 to drop to −2.0V. The output current would then be 2.0V/100Ω or 20 mA (Full Scale). If R_{B3} is a resistor of the same material as R_{B4} but not subjected to the strain, temperature drift effects will be equal in the two legs and will cancel.

In actual practice the loading effects of R_{B2} on the gain (span) and R_F on output current must be taken into account.

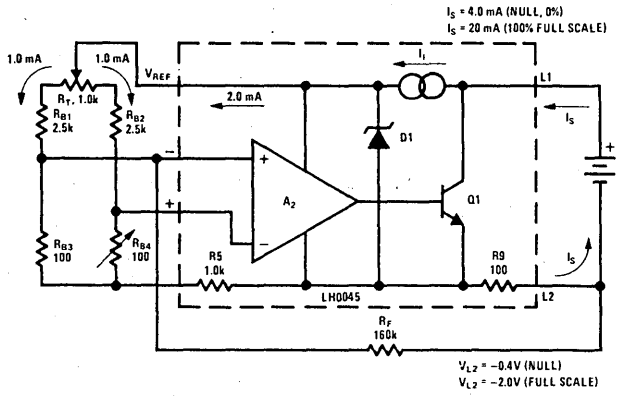


FIGURE 1. LH0045 Simplified Schematic

Applications Information (Cont'd)

THERMAL CONSIDERATIONS

The power output transistor of the LH0045 is thermally isolated from the signal amplifier, A_2. Nevertheless, a change in the power dissipation will cause a change in the temperature of the package and thus may cause amplifier drift. These temperature excursions may be minimized by careful heat sinking to hold the case temperature equal to the ambient. With the TO-8 (G) package this is best accomplished by a clip-on heat sink such as the Thermalloy #2240A or the Wakefield #215-CB. The 8 lead TO-3 is particularly convenient for heat sinking, in that it may be bolted directly to many commercial aluminum heat sink extrusions, or to the chassis. In both packages the case is electrically isolated from the circuit.

In addition, the power change can be minimized by operating the device from relatively high supply voltages in series with a relatively high load resistance. When the signal forces the supply current higher, the voltage across the device will be reduced and the internal power dissipation kept nearly equal to the low current, high voltage condition.

For example, take the case of a 4.0 mA to 20 mA transmitter with a 24V supply and a 100Ω load resistance. The power at 4.0 mA is (23.6V) x (4.0 mA) = 94.4 mW while at full scale the power is (22V) x (20 mA) = 440 mW. The net change in power is 345 mW. This change in power will cause a change in temperature and thus a change in offset voltage of A_2.

If the optimum load resistance of 800Ω (from Figure 2) is used, the power at null is [24V − (4.0 mA) x (800Ω)] (4.0 mA) = 83 mW. The power at full scale is [24V − (20 mA) x (800Ω)] (20 mA) = 160 mW. The net change is 77 mW. This change is significantly less than without the resistor.

If the supply voltage is increased to 48V and the load resistance chosen to be the optimum value from Figure 2 (1.95k), then the power at null is [48V − (4.0 mA) x (1.95k)] (4.0 mA) = 160.8 mW and the power at full scale is [48 − (20) x (1.95k)] (20 mA) = 180 mW for a net change of 19.2 mW.

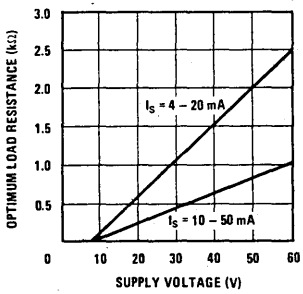


FIGURE 2. Optimum Load Resistance vs Supply Voltage

Note that the optimized load resistance is actually the sum of the line resistance, receiver resistances and added external load resistance. However, in many applications the line resistance and receiver resistances are negligible compared to the added external load resistance and thus may be omitted in calculations.

AUXILIARY PINS

The LH0045 has several auxiliary pins designed to provide the user with enhanced flexibility and performance. The following is a discussion of possible uses for these pins.

Programmable V_{REF} – Pins 5 and 6 (LH0045G Only)

The LH0045G provides pins 5 and 6 to allow the user to program the value of the reference voltage. The factory trimmed 10V value is obtained by leaving 5 and 6 open. A short between 5 and 6 will program the reference to a nominal 5.1V (equivalent to the fixed value used in the LH0045K).

A resistor or pot may be placed between pin 5 and common (pin 3) to obtain reference voltages between 10V and 30V or between pin 5 and pin 7 for reference voltages below 10V. Increased reference voltage might be useful to extend the positive common mode range or to accommodate transducers requiring higher supply voltage. A plot of resistance between pin 5 and pin 3 versus V_{REF} is given in the typical electrical characteristics section. V_{REF} may be adjusted about its nominal value by arranging a pot from V_{REF} to common and feeding a resistor from the wiper into pin 5 so that it may either inject or extract current. Lastly, pin 5 may be used as a nominal 1.7V reference point, if care is taken not to unduly load it with either dc current or capacitance. Obviously, higher supply voltages must be used to obtain the higher reference values. The minimum supply voltage to reference voltage differential is about 4.0V.

Bridge Return

An applications resistor is provided in the LH0045 with a nominal value of 1.0 kΩ. The primary application for the resistor is to maintain the minimum common mode input voltage (1.0V) required by the signal amplifier, A_2. A typical input application might utilize a strain gauge or thermistor bridge where the resistance of the sensor is 100Ω. Since only 1.0 mA may be drawn from V_{REF}, the 1.0 kΩ bridge return resistor is used to bias A_2 in its linear region as shown in Figure 3.

Applications Information (Cont'd)

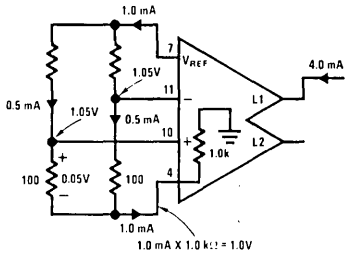


FIGURE 3. Use of Bridge Return

Over Compensation — Pin 8 (LH0045G), Pin 6 (LH0045K)

Over compensation of the signal amplifier, A_2 may be desirable in dc applications where the noise-bandwidth must be minimized. A capacitor should be placed between pin 8 (pin 6 on the LH0045K) and pin 3, common.

Typically,

$$f_{3db} = \frac{1}{2\pi R (C_1 + C_{EXT})}$$

where:

R = 400 MΩ

C1 = Internal Compensation Capacitor = 100 pF

C_{EXT} = External (over-compensation) Capacitor

Input Guard — Pins 9 and 12 (LH0045G)

Pins 9 and 12 have no internal connection whatever and thus need not be used. In some critical low current applications there may be an advantage to running a guard conductor between the inputs and the adjacent pins to intercept stray leakage currents. Pins 9 and 12 may be connected to this guard to simplify the PC board layout and allow the guard to continue under the device. (See AN-63 for further discussion of guarding techniques.)

NULL AND SPAN ADJUSTMENTS

Most applications of the LH0045 will require potentiometers to trim the initial tolerances of the sensor, the external resistors and the LH0045 itself. The preferred adjustment procedure is to stimulate the sensor, alternating between two known values, such as zero and full scale. The span and null are adjusted by monitoring the output current on a chart recorder, meter, or oscilloscope. A full scale stimulus is applied to the sensor and the span potentiometer adjusted for the desired full scale. Then, to adjust the null, apply a zero percent signal to the sensor and adjust the null potentiometer for the desired zero percent current indication.

If it is impractical to cycle the sensor during the calibration procedure, the signal may be simulated electrically with two cautions: 1) the calibration signal must be floating and 2) the calibration thus achieved does not account for sensor inaccuracies and/or errors in the signal generator.

SENSOR SELECTION

Generally it is easiest to use an insulated sensor. If it is necessary to use a grounded sensor, the power supply must be isolated from chassis ground to avoid extraneous circulating currents.

DESIGN EXAMPLE

There are numerous circuit configurations that may be utilized with the LH0045. The following is intended as a general design example which may be extended to specific cases.

Circuit Requirements

Output Characteristics

a. 0% = 4.0 mA (NULL)

b. 100% = 20 mA (SPAN = 16 mA)

c. Supply Voltage = 24V

Input (Sensor) Characteristics

a. V_{IN} = 100 mV (Full Scale)

b. V_{IN} = 0 mV (Zero Scale)

c. Source Impedance $\leq$ 1.0Ω

General Characteristics

a. $0°C \leq T_A \leq +75°C$

b. Overall Accuracy $\leq$ 0.5%

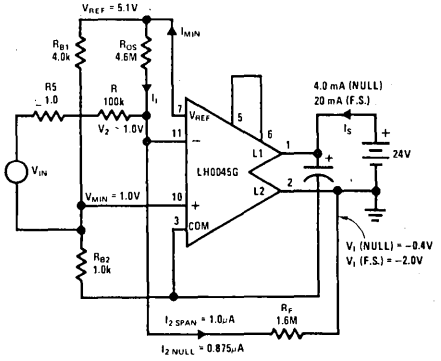


FIGURE 4. Design Example Circuit

Selection of R_F

Input bias current to the LH0045C is guaranteed less than 10 nA. Furthermore, the change in I_B over the temperature range of interest is typically under 1.0 nA. If $I_{2\ SPAN}$ is selected to be 1.0μA (1000 ΔI_B) errors due to $\Delta I_B/\Delta T$ will be less than 0.1%. For SPAN = 16 mA.

$$V_{SPAN} = \Delta V_1 = -(16\,mA)(R9) = -1.6V$$

Applications Information (Cont'd)

where R9 = Internal Current Set Resistor = 100Ω
For $I_{2\ SPAN}$ = 1.0μA,

$$R_F = \frac{V_{SPAN}}{I_{2\ SPAN}} = \frac{-1.6V}{1.0\mu A} = 1.6M$$

$$R_F = 1.6\ M\Omega$$

NOTE: For applications with DC gain (ratio of feedback and input resistance) less than 8, it is recommended that a Schottky barrier diode be connected between pin 11 (cathode) and pin 3 (anode). This prevents the possibility of latch up resulting from the inverting input being forced beyond the amplifier supply voltage during power up.

Selection of R_{B1} and R_{B2}

The minimum input common mode voltage, V_{MIN} required at the pin 10 input of A_2 is 1.0V. Furthermore, the maximum open loop supply current (I_{SOL}) drawn by the LH0045 is 3.0 mA. That leaves I_{MIN} = 4.0 mA − 3.0 mA = 1.0 mA left to bias the bridge at null. Hence:

$$R_{B2} \geqq \frac{V_{MIN}}{I_{MIN}} = \frac{1.0V}{1.0\ mA} = 1.0\ k\Omega$$

And,

$$\frac{V_{REF}\ R_{B2}}{R_{B1} + R_{B2}} = 1.0V$$

$$R_{B1} = R_{B2}\ \frac{V_{REF} - 1.0V}{1.0V}$$

$$= 1.0k\ (5.1 - 1.0)$$

$$R_{B1} \cong 4.0\ k\Omega$$

Alternatively, an LM113, 1.22V reference diode, or an op amp such as the LM108 may be used to bias the signal amplifier, A_2 as shown in Figure 5. These techniques have the advantage of lowering the impedance seen at pin 10.

Selection of R_{OS}

R_{OS} is selected to provide the null current of 4.0 mA, $V_{1\ NULL}$ = 4.0 mA x 100Ω = 0.4V. From previous calculations we know that V_{MIN} = 1.0V. The voltage pin 11, V_2 is:

$$V_2 = V_{MIN} + V_{OS} \cong V_{MIN}$$

for V_{IN} = 0V

Hence, the current required to generate the null voltage, $I_{2\ NULL}$ is:

$$I_{2\ NULL} = \frac{V_{MIN} - V_{1\ NULL}}{R_F}$$

$$= \frac{1.0V - (-0.4V)}{1.6\ M\Omega} = 0.875\mu A$$

This current must be provided by R_{OS} from V_{REF}; hence:

$$R_{OS} = \frac{V_{REF} - V_{MIN}}{I_{2\ NULL}}$$

The nominal value for V_{REF} is 5.1V, therefore the nominal value for R_{OS} is:

$$\frac{5.1V - 1.0V}{0.875\mu A} \quad \text{or}$$

$$R_{OS} = 4.6\ M\Omega$$

It should be noted however, that the variation of V_{REF} may be as high as 5.9V or as low as 4.3V. Furthermore, the tolerances of R9 (100Ω), R_{B1}, R_{B2}, and the input V_{OS} of A_2 would predict values for R_{OS} as low as 3.98M and as high as 5.43M. The implication is that in the specific case, R_{OS} should be implemented with a pot, of appropriate value, in order to accommodate the tolerances of V_{REF}, R9, V_{OS}, R_{B1}, R_{B2}, etc.

Selection of R

SPAN is required to be 16 mA. From feedback theory and the gain equation we know:

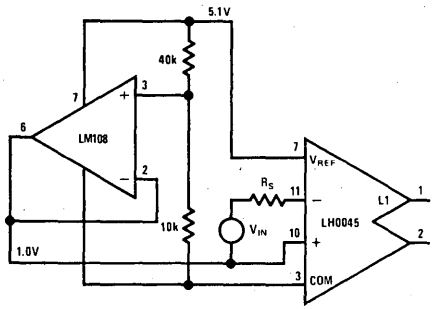
$$I_{SPAN} = V_{IN}\ \frac{R_F}{R}\ x\ \frac{1}{R9}$$

where:

R = total impedance in signal path between pin 10 and pin 11

R9 = Current setting resistor = 100Ω

V_{IN} = Full scale input voltage = 100 mV



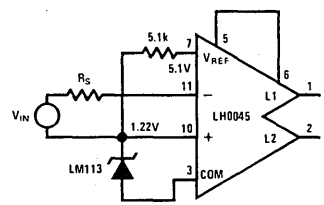


FIGURE 5. Alternate Biasing Techniques

Applications Information (Cont'd)

$$\therefore R = \frac{(V_{IN})\,(R_F)}{(I_{SPAN})\,(R9)}$$

$$R = \frac{(100\text{ mV})\,(1.6\text{ M}\Omega)}{(16\text{ mA})\,(100\Omega)}$$

$$R = 100\text{ k}\Omega$$

As before, uncertainties in device parameters might dictate that R_F be made a pot of appropriate value.

Summary of the Steps to Determine External Resistor Values

1. Select $I_{FULL\ SCALE} = I_{NULL} + I_{SPAN}$ for the desired application. (I_{NULL} is frequently 4.0 mA and $I_{FULL\ SCALE}$ is frequently 20 mA.)

2. Select $I_{2\ SPAN}$ so that it is large compared to ΔI_B. 1000 ΔI_B is a good value.

3. Determine $V_{SPAN} = \Delta V_2 = (I_{SPAN})(R9)$.

4. Determine $R_F = (V_{SPAN}/I_{2\ SPAN})$

5. Select

$$R_{B2} \geq \frac{V_{MIN}}{I_{MIN}}$$

$$R_{B2} \geq \frac{1\text{ VOLT}}{I_{NULL} - I_{SOL}}$$

Where:

V_{MIN} = minimum common mode input voltage

I_{MIN} = minimum available bridge current

I_{SOL} = maximum open loop supply current

6. Determine

$$R_{B1} = R_{B2}\,\frac{V_{REF} - V_{MIN}}{V_{MIN}}$$

7. Determine $V_{2\ NULL} = I_{NULL}\ R9$

8. Determine

$$I_{2\ NULL} = \frac{V_{MIN} - V_{2\ NULL}}{R_F}$$

9. Determine

$$R_{OS} = \frac{V_{REF} - V_{MIN}}{I_{2\,NULL}}$$

10. Determine

$$R = \frac{(V_{IN})\,(R_F)}{(I_{SPAN})\,(R9)}$$

Where:

V_{IN} = Sensor full scale output voltage

ERROR BUDGET ANALYSIS

Errors Due to Change in V_{REF} (ΔV_{REF})

There are several factors which could cause a change in V_{REF}. First, as the ambient temperature changes, a V_{REF} drift of ±0.2 mV/°C might be expected. Secondly, supply voltage variations could cause a 0.5 mV/V change in V_{REF}. Lastly, self-heating due to power dissipation variations can cause drift of the reference.

An overall expression for change in V_{REF} is:

$$\Delta V_{REF} = \underbrace{\left[(\theta)(\Delta P_{DISS}) + \Delta T_A\right]\frac{\Delta V_{REF}}{\Delta T}}_{\text{Thermal Effects}} + \underbrace{\frac{\Delta V_{REF}}{\Delta V_S}\,(\Delta V_S)}_{\text{Supply Voltage Effects}}$$

Where:

θ = Thermal resistance, either junction-to-ambient to junction to case

ΔP_{DISS} = Change in avg. power dissipation

ΔT_A = Change in ambient temperature

$\frac{\Delta V_{REF}}{\Delta T}$ = Reference voltage drift (in mV/°C)

$\frac{\Delta V_{REF}}{\Delta V_S}$ = Line regulation of V_{REF}

Several steps may be taken to minimize the bracketed terms in the equation above. For example, operating the LH0045G with a heat-sink reduces the thermal resistance from $\theta_{JA} = 83°C/W$ to $\theta_{JC} = 60°C/W$. For the LH0045K (TO-3) $\theta_{JA} = 40°C/W$ may be reduced to $\theta_{JC} = 25°C/W$ by using a heat sink. The ΔP_{DISS} term may be significantly reduced using the power minimization technique described under "Thermal Considerations." For the design example, ΔP_{DISS} is reduced from 384 mW to 77 mW ($R_L = 800\Omega$.) Evaluating the LH0045G with a heat-sink and $R_L = 800\Omega$ yields.

$$\Delta V_{REF} = \left(\frac{60°C}{W}\,(0.077W) + 75°C\right)\left(\frac{0.2\text{ mV}}{°C}\right) + \frac{0.5\text{ mV}}{V}\,(16V)$$

$$\Delta V_{REF} = 24\text{ mV}$$

The LH0045K (TO-3) under the same operating conditions would exhibit a $\Delta V_{REF} \cong 23$ mV.

Applications Information (Cont'd)

An expression for error in the output current due to ΔV_{REF} is:

$$\frac{\Delta I_S}{I_{SPAN}} (\%) = 100 \frac{(K)(R_{OS})(\Delta V_{REF}) - (1-K)(\Delta V_{REF})(R_F)}{(R9)(R_{OS})(I_{SPAN})}$$

Where:

ΔV_{REF} = Total change in V_{REF}

$K = \frac{R_{B2}}{R_{B1} + R_{B2}}$

R9 = Current set resistor

I_{SPAN} = Change in output current from 0% to 100%

For example, ΔV_{REF} = 24 mV, K = 0.2, R9 = 100Ω, I_{SPAN} = 16 mA. Hence, a 0.12% worst case error might be expected in output currents due to ΔV_{REF} effects.

Error Due to V_{OS} Drift

One of the primary causes of error in I_S is caused by V_{OS} drift. Drift may be induced either by self heating of the device or ambient temperature changes. The input offset voltage drift, $\Delta V_{OS}/\Delta T$, is nominally 3.3μV/°C per millivolt of initial offset. An expression for the total temperature dependent drift is:

$$\Delta V_{OS} = [(\theta)(\Delta P_{DISS}) + \Delta T_A] \frac{\Delta V_{OS}}{\Delta T}$$

Where:

θ = Thermal resistance either junction-to-ambient or junction-to-case

ΔP_{DISS} = Change in average power dissipation

ΔT_A = Change in ambient temperature

The bracketed term may be minimized by heat sinking and using the power minimization technique described under "Thermal Considerations." For the LH0045G design example, ΔV_{OS} = 0.352 mV under ambient conditions and 0.263 mV using a heat-sink and R_L = 800Ω. Comparable V_{OS} for the LH0045K would be 0.254 mV.

The error in output current due to ΔV_{OS} is:

$$\frac{\Delta I_S}{I_{SPAN}} (\text{in } \%) = 100 \times \frac{\Delta V_{OS}}{V_{IN\ (FULL\ SCALE)}}$$

$$= 100 \times \frac{R_F}{(R)(R9)(I_{SPAN})}$$

For the design example, ΔV_{OS} = 0.263 mV, V_{IN} (Full Scale) = 100 mV. Hence, 0.26 mV ÷ 100 mV or 0.26% worst case error could be expected in output current effects.

Errors Due to Changes in R9

The temperature coefficient of R9 (TCR) will produce errors in the output current. Changes in R9 may be caused by self-heating of the device or by ambient temperature changes.

$$\frac{\Delta I_S}{I_{SPAN}} (\text{in } \%) = 100 \frac{\Delta R9}{\Delta T} (\theta P_{DISS} + \Delta T_A)$$

Where:

θ = Thermal resistance either from junction-to-ambient or junction-to-case

ΔP_{DISS} = Change in average power dissipation

ΔT_A = Change in ambient temperature

$\frac{\Delta R9}{\Delta T}$ = TCR of R9

Using the LH0045G design example, $\Delta R9/\Delta T$ = 0.03%/°C, hence a 3.2% worst case error in output current might be expected for operation without a heat sink over the temperature range.

Heat sinking the device and using R_L = 800Ω, reduces $\Delta I_S/I_{SPAN}$ to 2.3%. Comparable error for the LH0045K would also be about 2.3%.

The error analysis indicates that the internal current set resistor, R9 is inadequate to satisfy high accuracy design criterion. In these instances, an external 100Ω resistor should be substituted for R9.

Obviously, the TCR of the resistor should be low. Metal film or wire-wound resistors are the best choice offering TCR's less than 10 ppm/°C versus 50 ppm/°C typical drift for R9.

External Causes of Error

The components external to the LH0045 are also critical in determining errors. Specifically, the composition of resistors R_{B1}, R_{OS}, R_F, R, etc. in the design example will influence both drift and long term stability.

In particular, resistors and potentiometers of wire wound construction are recommended. Also, metal-film resistors with low TCR (≤ 10 ppm/°C) may be used for fixed resistor applications.

Applications Information (Cont'd)

Error Analysis Summary

The overall errors attributable to the LH0045 may be minimized using heat sinking, and utilization of an external load resistor. Although R_L reduces the compliance of the circuit, its use is generally advisable in precision applications. External components should be selected for low TCR and long-term stability.

The design example errors, using an external 100Ω wire wound resistor for R9 equal:

$$\frac{\Delta I_S}{I_{SPAN}} = \underbrace{0.12\%}_{\Delta V_{REF}} + \underbrace{0.26\%}_{\Delta V_{OS}} + \underbrace{0.08\%}_{\Delta R9} = 0.46\%$$

SOCKETS AND HEAT SINKS

Mounting sockets, test sockets, and heat sinks are available for the G package and K package.

The following or their equivalents are recommended:

Sockets:

G – 12 lead TO-8:	Barnes Corp. #MGX-12 Textool #212-100-323
K – 8 lead TO-3:	Robinson Nugent #0002011 Wells #6010–20811

Heat Sinks

G – 12 lead TO-8:	Thermalloy #2240A Wakefield #215-CB
K – 8 lead TO-3:	IERC #LAIC 3B4V

Definition of Terms

Input Offset Voltage, V_{OS}: The voltage which must be applied between the input terminals through equal resistances to obtain 4.0 mA of supply (output) current.

Input Bias Current, I_B: The average of the two input currents.

Input Offset Current, I_{OS}: The difference in the current into the two input terminals when the supply (output) current is 4.0 mA.

Input Resistance, R_{IN}: The ratio of the change in input voltage to the change in input current at either input with the other input connected to 1.0 Vdc.

Open Loop Transconductance, g_{MOL}: The ratio of the supply (output) current SPAN to the input voltage required to produce that SPAN.

Open Loop Output Resistance, R_{OUT}: The ratio of a specified supply (output) voltage change to the resulting change in supply (output) current at the specified current level.

Common Mode Rejection Ratio, CMRR: The ratio of the change in input offset voltage to the peak-to-peak input voltage range.

Power Supply Rejection Ratio, PSRR: The ratio of the change in input offset voltage to the change in supply (output) voltage producing it.

Input Voltage Range, V_{IN}: The range of voltages on the input terminals for which the device operates within specifications.

Open Loop Supply Current, I_S: The supply current required with the signal amplifier A_2 biased off (inverting input positive, non-inverting input negative) and no load on the V_{REF} terminal.

This represents a measure of the minimum low end signal current.

Reference Voltage Line Regulation, $\Delta V_{REF}/\Delta V_S$: The ratio of the change in V_{REF} to the peak-to-peak change in supply (output) voltage producing it.

Reference Voltage Load Regulation, $\Delta V_{REF}/\Delta I_{REF}$: The change in V_{REF} for a stipulated change in I_{REF}.

National Semiconductor

LH0061/LH0061C 0.5 Amp Wide Band Operational Amplifier

General Description

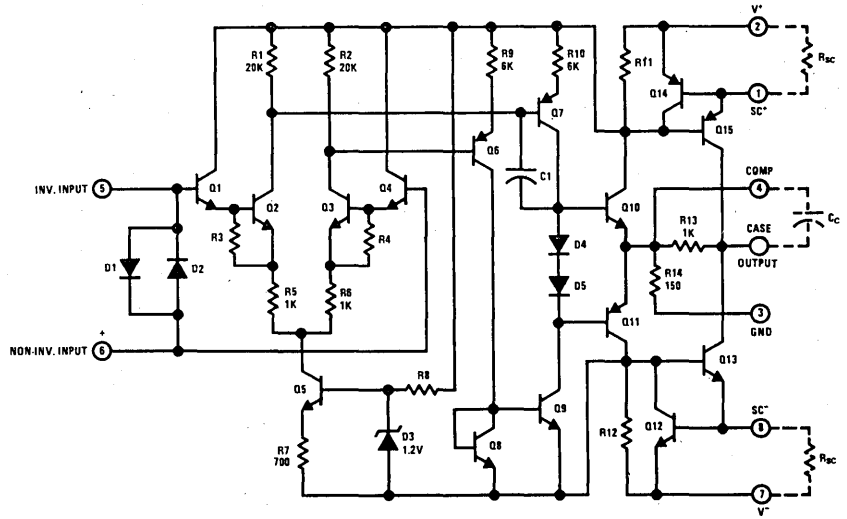
The LH0061/LH0061C is a wide band, high speed, operational amplifier capable of supplying currents in excess of 0.5 ampere at voltage levels of ±12V. Output short circuit protection is set by external resistors, and compensation is accomplished with a single external capacitor. With a suitable heat sink the device is rated at 20 Watts.

The wide bandwidth and high output power capabilities of the LH0061/LH0061C make it ideal for such applications as AC servos, deflection yoke drivers, capstan drivers, and audio amplifiers. The LH0061 is guaranteed over the temperature range −55°C to +125°C; whereas, the LH0061C is guaranteed from −25°C to +85°C.

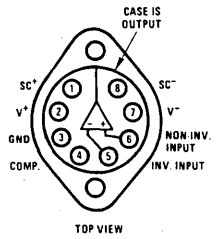
Features

- Output current 0.5 Amp
- Wide large signal bandwidth 1 MHz
- High slew rate 70V/μs
- Low standby power 240 mW
- Low input current 300 nA Max

Schematic and Connection Diagrams



TO-3 Package



Order Numbers:

LH0061K (−55°C to +125°C)
LH0061CK (−25°C to +85°C)
See Package K08A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation	See Curve
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Peak Output Current	2A
Output Short Circuit Duration (Note 4)	Continuous
Operating Temperature Range LH0061	−55°C to +125°C
LH0061C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

DC Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0061			LH0061C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S < 10\,k\Omega$, $T_C = 25°C$, $V_S = \pm15V$		1.0	4.0		3.0	10	mV
	$R_S < 10\,k\Omega$, $V_S = \pm15V$			6.0			15	mV
Voltage Drift with Temperature	$R_S < 10\,k\Omega$		5			5		µV/°C
Offset Voltage Change with Output Power			5			5		µV/watt
Input Offset Current	$T_C = 25°C$		30	100		50	200	nA
				300			500	nA
Offset Current Drift with Temperature			1			1		nA/°C
Input Bias Current	$T_C = 25°C$		100	300		200	500	nA
				1.0			1.0	µA
Input Resistance	$T_C = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S < 10\,k\Omega$, $\Delta V_{CM} = \pm10V$	70	90		60	80		dB
Input Voltage Range	$V_S = \pm15V$	±11			±11			V
Power Supply Rejection Ratio	$R_S < 10\,k\Omega$, $\Delta V_S = \pm10V$	70	80		50	70		dB
Voltage Gain	$V_S = \pm15V$, $V_O = \pm10V$							
	$R_L = 1\,k\Omega$, $T_C = 25°C$	50	100		25	50		V/mV
	$V_S = \pm15V$, $V_O = \pm10V$							
	$R_L = 20\Omega$	5			2.5			V/mV
Output Voltage Swing	$V_S = \pm15V$, $R_L = 20\Omega$	±10	±12		±10	±12		V
Output Short Circuit Current	$V_S = \pm15V$, $T_C = 25°C$, $R_{SC} = 1.0\Omega$		600			600		mA
Power Supply Current	$V_S = \pm15V$, $V_{OUT} = 0$		7	10		10	15	mA
Power Consumption	$V_S = \pm15V$, $V_{OUT} = 0$		210	300		300	450	mW

AC Electrical Characteristics ($T_C = 25°C$, $V_S = \pm15V$, $C_C = 3000\,pF$)

Slew Rate	$A_V = +1$, $R_L = 100\Omega$	25	70		25	70		V/µs
Power Bandwidth	$R_L = 100\Omega$		1			1		MHz
Small Signal Transient Response			30			30		ns
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		0.8			0.8		µs
Overload Recovery Time			1			1		µs
Harmonic Distortion	$f = 1\,kHz$, $P_O = 0.5W$		0.2			0.2		%

Note 1: Specifications apply for $\pm5V \leq V_S \leq \pm18V$, $C_C = 3000\,pF$, and $-55°C \leq T_C \leq +125°C$ for the LH0061K and $-25°C \leq T_C \leq +85°C$ for the LH0061CK. Typical values are for $T_C = 25°C$.

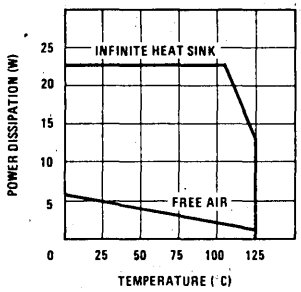
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Excessive current will flow if a differential voltage in excess of 1V is applied between the inputs without limiting resistors.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

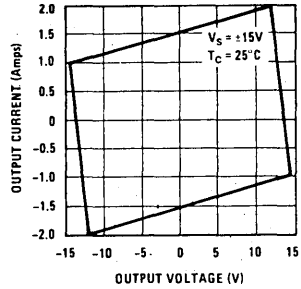
Note 4: Rating applies as long as package power rating is not exceeded.

Typical Performance Characteristics

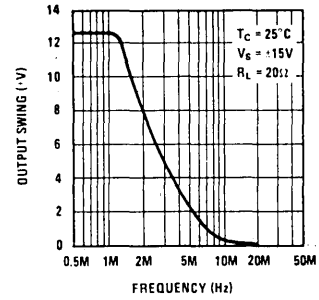
Power Derating



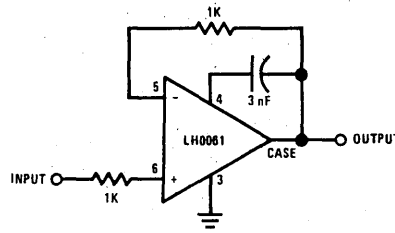
Safe Operating Area



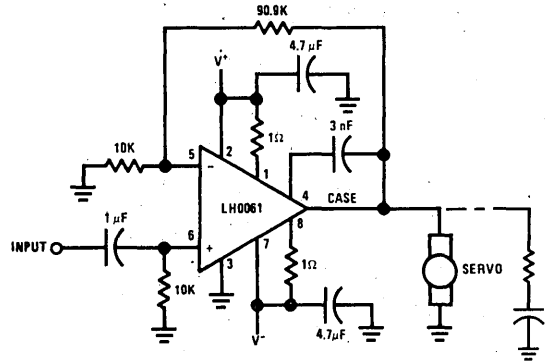
Large Signal Frequency Response



Typical Applications



Unity Gain Driver



AC Servo Amplifier

National Semiconductor

LH0062/LH0062C High Speed FET Operational Amplifier

General Description

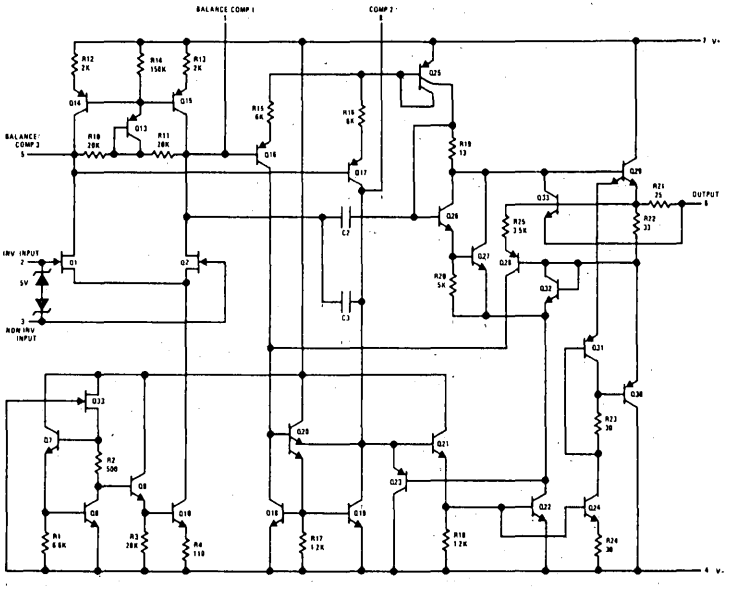
The LH0062/LH0062C is a precision, high speed FET input operational amplifier with more than an order of magnitude improvement in slew rate and bandwidth over conventional FET IC op amps. In addition it features very closely matched input characteristics, very high input impedance, and ultra low input currents with no compromise in noise, common mode rejection ratio or open loop gain. The device has internal unity gain frequency compensation, thus assuring stability in all normal applications. This considerably simplifies its application, since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 120 V/μs and almost double the bandwidth. (See LB-2, LB-14, and LB-17 for discussions of the application of feed-forward techniques). Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs. In addition it is free of latch-up and may be simply offset nulled with negligible effect on offset drift or CMRR.

The LH0062 is designed for applications requiring wide bandwidth, high slew rate and fast settling time while at the same time demanding the high input impedance and low input currents characteristic of FET inputs. Thus it is particularly suited for such applications as video amplifiers, sample/hold circuits, high speed integrators, and buffers for A/D conversion and multiplex system. The LH0062 is specified for the full military temperature range of −55° to +125°C while the LH0062C is specified to operate over a −25°C to +85°C temperature range.

Features

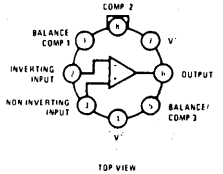
- High slew rate — 70 V/μs
- Wide bandwidth — 15 MHz
- Settling time (0.1%) — 1μs
- Low input offset voltage — 2 mV
- Low input offset current — 1 pA
- Wide supply range — ±5V to ±20V
- Internal 6 dB/octave frequency compensation
- Pin compatible with std IC op amps (TO-5 pkg)

Schematic and Connection Diagrams



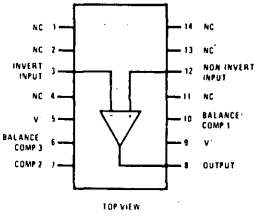
*Pin Numbers Shown for TO-5 Package

Metal Can Package



Order Number
LH0062H or LH0062CH
See Package H08A

Dual-In-Line Package



Order Number
LH0062D or LH0062CD
See Package D14E

Absolute Maximum Ratings

Supply Voltage	±20V	Operating Temperature	
Power Dissipation (see graph)	500 mW	LH0062,	−55°C to +125°C
Input Voltage (Note 1)	±5V	LH0062C,	−25°C to +85°C
Differential Input Voltage (Note 2)	±30V	Storage Temperature Range	−65°C to +150°C
Short Circuit Duration	Continuous	Lead Temperature (Soldering, 10 sec)	300°C

DC Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0062			LH0062C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100\ k\Omega$; $T_A = 25°C$		2	5		10	15	mV
	$R_S \leq 100\ k\Omega$			7			20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5	25		10	35	µV/°C
Offset Voltage Drift with Time			4			5		µV/week
Input Offset Current	$T_A = 25°C$		0.2	2		1	5	pA
				2			0.2	nA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	$T_A = 25°C$		5	10		10	65	pA
				10			2	nA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4			4		pF
Input Voltage Range	$V_S = \pm 15V$	±10	±12		±10	±12		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$	80	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	80	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$, $V_S = \pm 15V$	50	200		25	160		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $V_S = \pm 15V$	25			25			V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25°C$, $V_S = \pm 15V$	±12	±13		±12	±13		V
	$R_L = 2\ k\Omega$, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current	$T_A = 25°C$		25			25		mA
Supply Current	$V_S = \pm 15V$		5	8		7	12	mA
Power Consumption	$V_S = \pm 15V$			240			360	mW

AC Electrical Characteristics ($T_A = 25°C$, $V_S = \pm 15V$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0062			LH0062C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	Voltage Follower	50	70		50	70		V/µs
Large Signal Bandwidth	Voltage Follower		2			2		MHz
Small Signal Bandwidth			15			15		MHz
Rise Time			25			25		ns
Overshoot			10			15		%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$		1			1		µs
Overload Recovery			0.9			0.9		µs
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 10\ Hz$		150			150		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 100\ Hz$		55			55		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 1\ kHz$		35			35		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10\ k\Omega$, $f_o = 10\ kHz$		30			30		$nV/\sqrt{Hz}$
Input Noise Voltage	BW = 10 Hz to 10 kHz, $R_S = 10\ k\Omega$		12			12		µVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

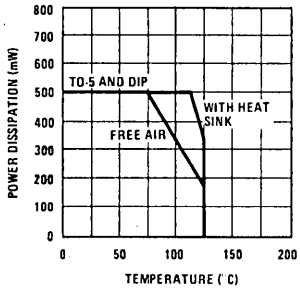
Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Inputs are protected from excessive voltages by back-to-back diodes. Input currents should be limited to 1 mA.

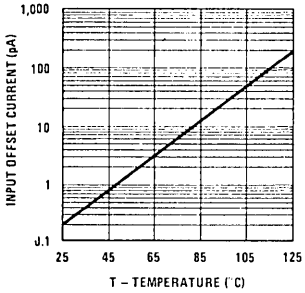
Note 3: Unless otherwise specified, these specifications apply for $+5V < V_S < +20V$ and $-55°C < T_A < +125°C$ for the LH0062 and $-25°C < T_A < +85°C$ for LH0062C. Typical values are given for $T_A = 25°C$. Power supplies should be bypassed with 0.1 µF ceramic capacitors.

Typical Performance Characteristics

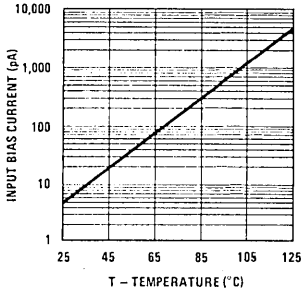
Maximum Power Dissipation



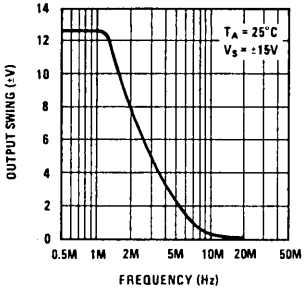
Input Offset Current vs Temperature



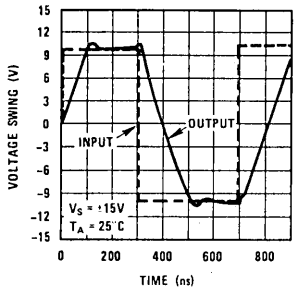
Input Bias Current vs Temperature



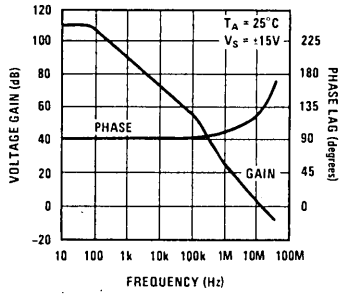
Large Signal Frequency Response



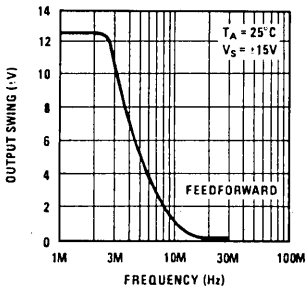
Voltage Follower Pulse Response



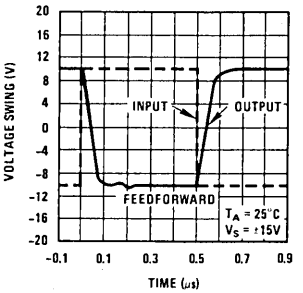
Open Loop Frequency Response



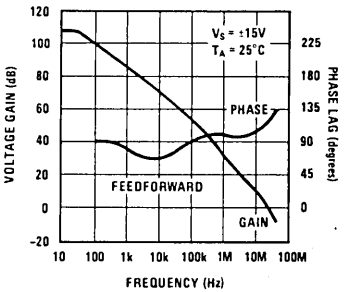
Large Signal Frequency Response



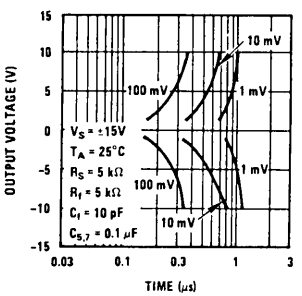
Inverter Pulse Response



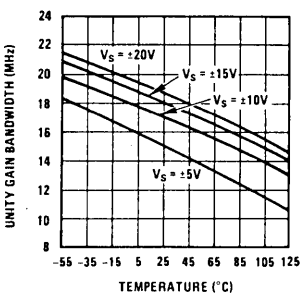
Open Loop Frequency Response



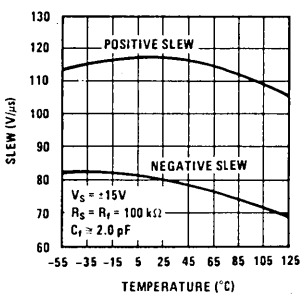
Inverter Settling Time



Unity Gain Bandwidth

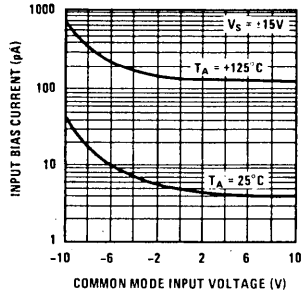


Voltage Follower Slew Rate

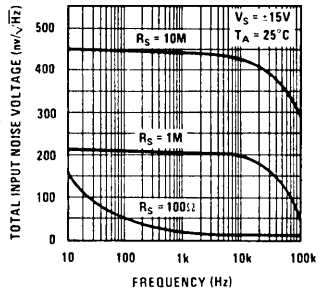


Typical Performance Characteristics (Cont'd)

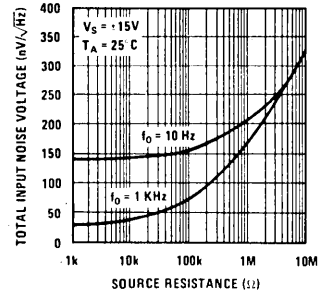
Input Bias Current vs Input Voltage



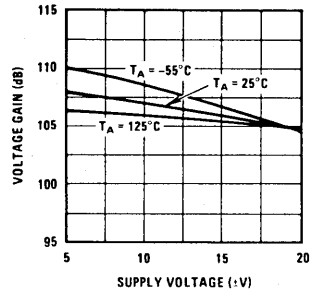
Total Input Noise Voltage* vs Frequency



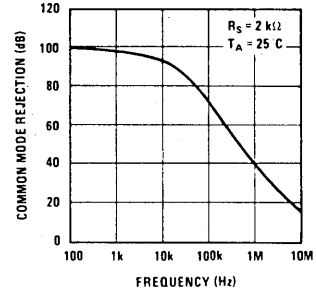
Total Input Noise Voltage* vs Source Resistance



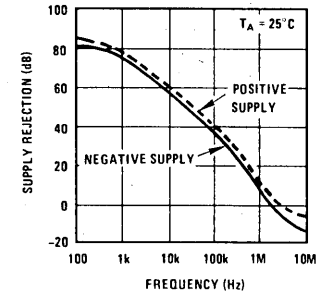
Voltage Gain



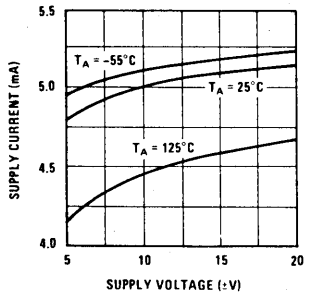
Common Mode Rejection



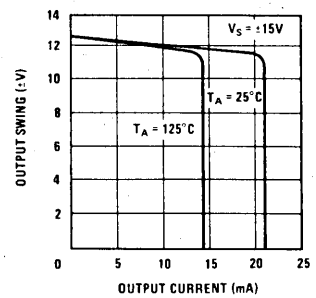
Power Supply Rejection



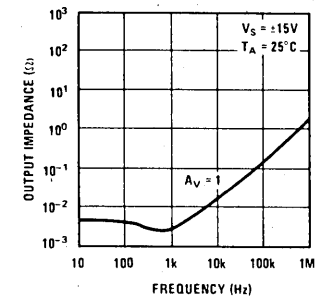
Supply Current



Current Limiting



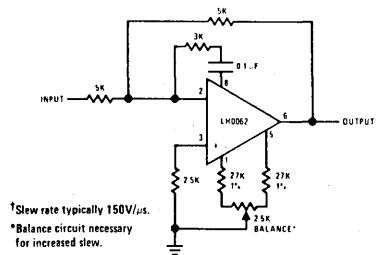
Closed Loop Output Impedance



*Noise Voltage Includes Contribution from Source Resistance

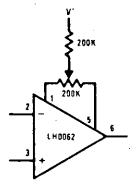
Auxiliary Circuits

Feedforward Compensation for Greater Inverting Slew Rate†

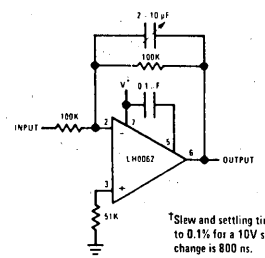


†Slew rate typically 150V/µs.
*Balance circuit necessary for increased slew.

Offset Balancing



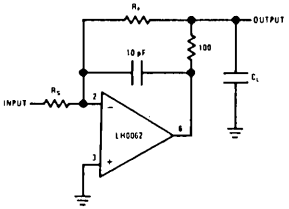
Compensation for Minimum Settling† Time



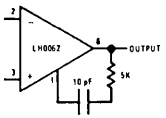
†Slew and settling time to 0.1% for a 10V step change is 800 ns.

Auxiliary Circuits (Cont'd)

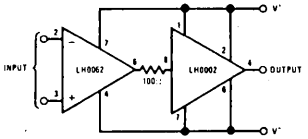
Isolating Large Capacitive Loads



Overcompensation

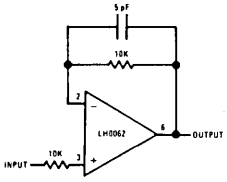


Boosting Output Drive to ±100 mA

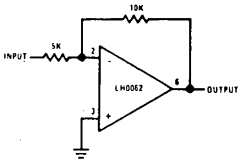


Typical Applications*

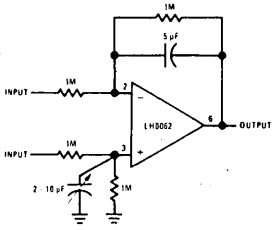
Fast Voltage Follower



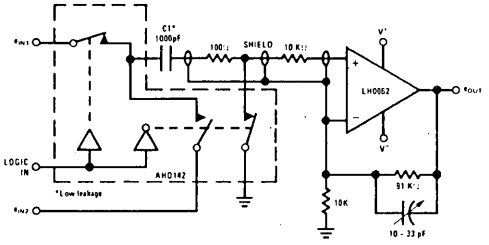
Fast Summing Amplifier



Differential Amplifier

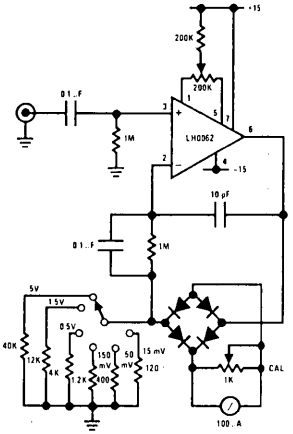


High Speed Subtractor

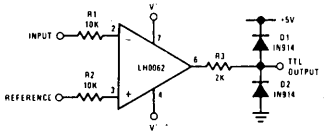


$e_{OUT} = 10 \times (e_{IN1} - e_{IN2})$

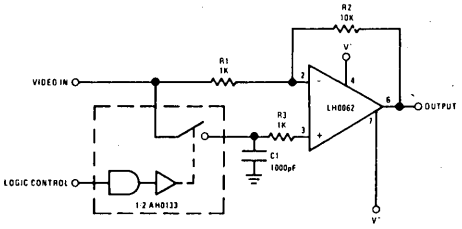
Wide Range AC Voltmeter



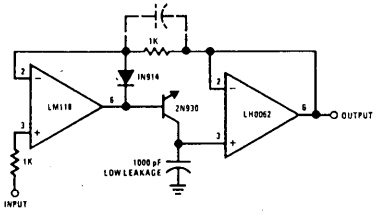
Fast Precision Voltage Comparator



Video DC Restoring Amplifier



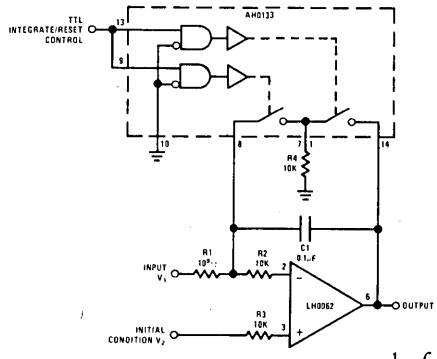
High Speed Positive Peak Detector



*Pin numbers shown for TO-5 package

Typical Applications* (Cont'd)

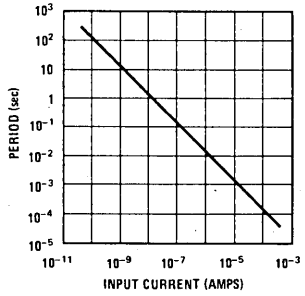
Precision Integrator

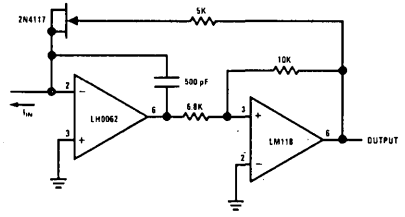


$$V_{OUT} = \frac{1}{C1R1}\int -V_1\,dt + V_2$$

*Pin numbers shown for TO-5 package

Precision Wide Range Current to Period Converter





National Semiconductor

LH0101/LH0101C, LH0101A/LH0101AC Power Operational Amplifier

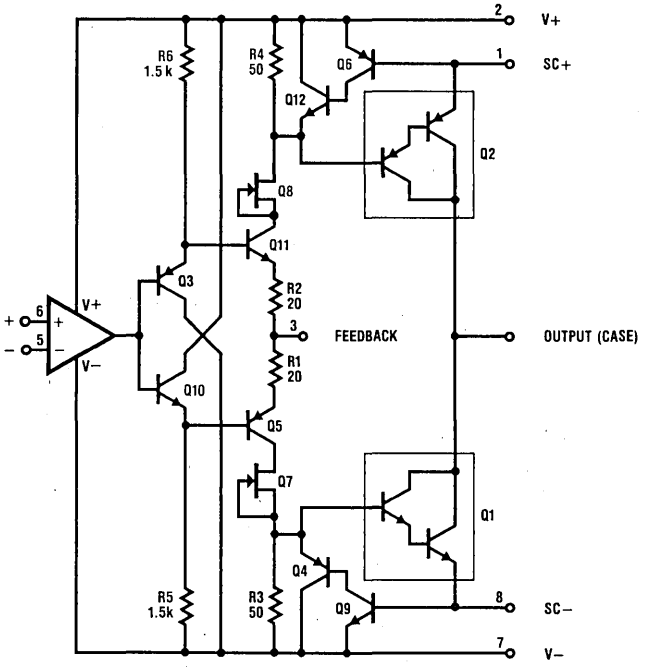
General Description

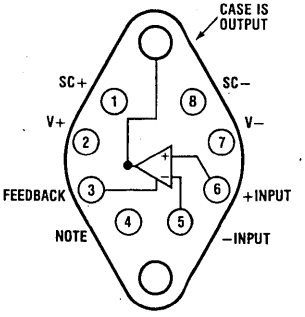
The LH0101 is a wideband power operational amplifier featuring FET inputs, internal compensation, virtually no crossover distortion, and rapid settling time. These features make the LH0101 an ideal choice for DC or AC servo amplifiers, deflection yoke drives, programmable power supplies, and disk head positioner amplifiers. The LH0101 is packaged in an 8 pin TO-3 hermetic package, rated at 20 watts with a suitable heat sink.

Features

- 5 Amp peak, 2 Amp continuous output current
- 300 kHz power bandwidth
- 850 mW standby power (±15V supplies)
- 300 pA input bias current
- 10 V/μS slew rate
- Virtually no crossover distortion
- 2μS settling time to 0.01%
- 5 MHz gain bandwidth

Schematic and Connection Diagrams





TOP VIEW

Order Numbers

LH0101CK
LH0101K
LH0101ACK
LH0101AK

See Package K08A

NOTE: ELECTRICALLY CONNECTED INTERNALLY, NO CONNECTION SHOULD BE MADE TO PIN.

Absolute Maximum Ratings

Supply Voltage, V_S	±22V
Power Dissipation at $T_A = 25°C$, P_D	5W
Derate linearly at 25°C/W to zero at 150°C,	
Power Dissipation at $T_C = 25°C$	62W
Derate linearly at 2°C/W to zero at 150°C	
Differential Input Voltage, V_{IN}	±40V but < $\pm V_S$
Input Voltage Range, V_{CM}	±20V but < $\pm V_S$
Peak Output Current (50ms pulse), $I_{O(PK)}$	5A
Output Short Circuit Duration (within rated power dissipation,	
$R_{SC} = 0.35\Omega$, $T_A = 25°C$)	Continuous
Operating Temperature Range, T_A	
LH0101, LH0101C	−25°C to +85°C
LH0101A, LH0101AC	−55°C to +125°C
Storage Temperature Range, T_{STG}	−65°C to +150°C
Maximum Junction Temperature, T_J	150°C
Lead Temperature (Soldering < 10 seconds)	300°C

DC Electrical Characteristics (see Note 1) $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

				LH0101AC LH0101A			LH0101C LH0101			
Symbol	Parameter	Conditions		Min.	Typ.	Max.	Min.	Typ.	Max.	Units
V_{OS}	Input Offset Voltage				1	3		5	10	mV
		$T_{MIN} \leq T_A \leq T_{MAX}$				7			15	
$\Delta V_{OS}/\Delta P_D$	Change in Input Offset Voltage with dissipated power	Note 2			150			300		µV/W
$\Delta V_{OS}/\Delta T$	Change in Input Offset Voltage with temperature	$V_{CM} = 0$			10			10		µV/°C
						300			1000	pA
I_B	Input Bias Current	$T_A \leq T_{MAX}$	LH0101C/AC			60			60	nA
			LH0101/A			300			1000	
						75			250	pA
I_{OS}	Input Offset Current	$T_A \leq T_{MAX}$	LH0101C/AC			15			15	nA
			LH0101/A			75			250	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$	$R_L = 10\Omega$	50	200		50	200		V/mV
V_O	Output Voltage Swing	$R_{SC} = 0$	$R_L = 100\Omega$	±11.7	±12.5		±11.7	±12.5		V
		$A_V = +1$	$R_L = 10\Omega$	±11	±11.6		±11	±11.6		
		Note 3	$R_L = 5\Omega$	±10.5	±11		±10.5	±11		
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = \pm 10V$		85	100		85	100		dB
PSRR	Power Supply Rejection Ratio	$\Delta V_S = \pm 5V$ to $\pm 15V$		85	100		85	100		
I_S	Quiescent Supply Current				28	35		28	35	mA

AC Electrical Characteristics See Note 1, $V_S = \pm 15V$, $T_A = 25°C$

Symbol	Parameter	Conditions		LH0101AC LH0101A Min.	LH0101AC LH0101A Typ.	LH0101AC LH0101A Max.	LH0101C LH0101 Min.	LH0101C LH0101 Typ.	LH0101C LH0101 Max.	Units
e_n	Equivalent input noise voltage	$f = 1kHz$			25			25		$nV/\sqrt{Hz}$
C_{in}	Input Capacitance	$f = 1MHz$			3.0			3.0		pF
	Power Bandwidth, −3dB	$R_L = 10\Omega$	$A_V = +1$		300			300		kHz
SR	Slew Rate			7.5 (note 4)	10			10		V/μs
t_r, t_f	Small Signal Rise or Fall Time				200			200		ns
	Small Signal Overshoot				10			10		%
GBW	Gain-Bandwidth Product	$R_L = \infty$		4.0 (note 4)	5.0			5.0		MHz
t_s	Large Signal Settling Time to 0.01%				2.0			2.0		μs
THD	Total Harmonic Distortion	$P_O = 0.5W$ $f = 1kHz$ $R_L = 10\Omega$			0.008			0.008		%

Note 1: Specification is at $T_A = 25°C$. Actual values at operating temperature may differ from the $T_A = 25°C$ value. When supply voltages are ±15V, quiescent operating junction temperature will rise approximately 20°C without heat sinking. Accordingly, V_{OS} may change 0.5mV and I_B and I_{OS} will change significantly during warm-ups. Refer to the I_B vs. temperature and power dissipation graphs for expected values. Power supply voltage is ±15V. Temperature tests are made only at extremes.

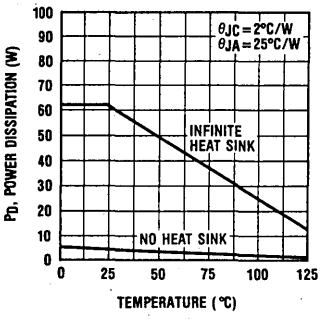
Note 2: Change in offset voltage with dissipated power is due entirely to average device temperature rise and not to differential thermal feedback effects. Test is performed without any heat sink.

Note 3: At light loads, the output swing may be limited by the second stage rather than the output stage. See the application section under "Output swing enhancement" for hints on how to obtain extended operation.

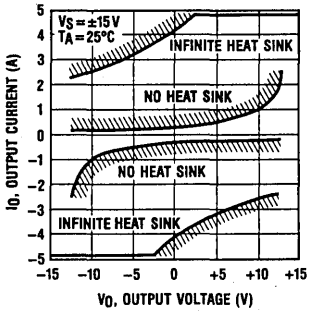
Note 4: These parameters are sample tested to 10% LTPD.

Typical Performance Characteristics

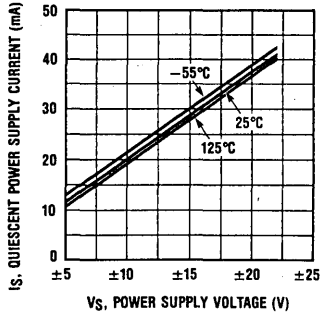
Maximum Power Dissipation



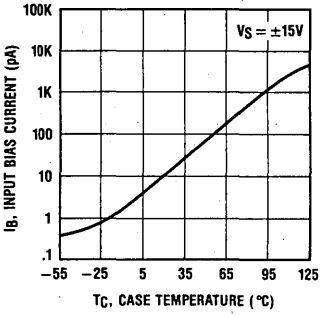
Safe Operating Area



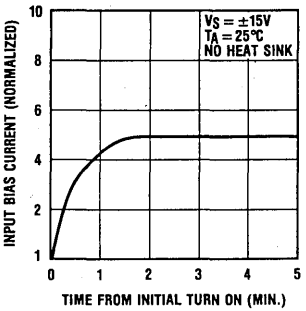
Quiescent Power Supply Current



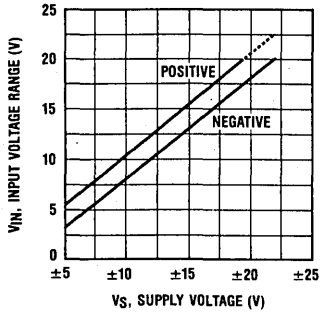
Input Bias Current



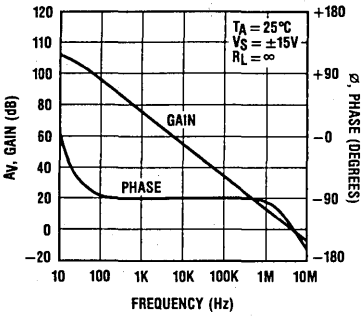
Input Bias Current after Warm-up



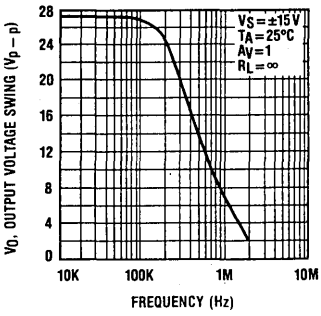
Input Common-Mode Voltage Range



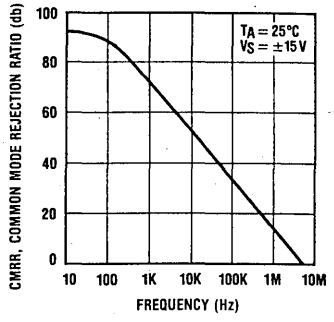
Small Signal Frequency Response (open loop)



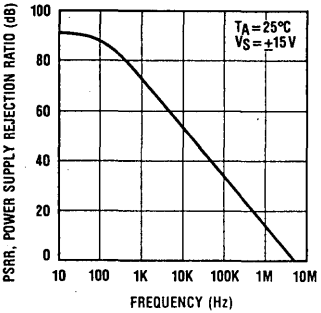
Output Voltage Swing vs. Frequency



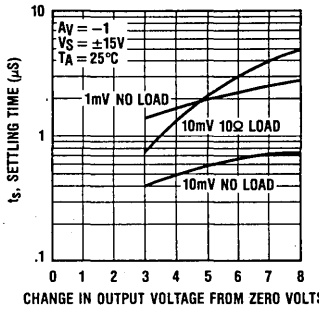
Common-Mode Rejection Ratio vs. Frequency



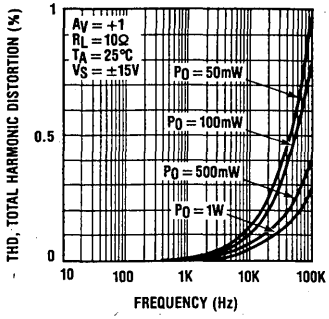
Power Supply Rejection Ratio vs. Frequency



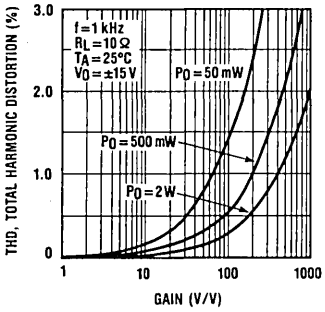
Settling Time



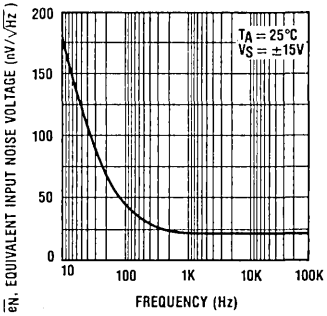
Total Harmonic Distortion vs. Frequency



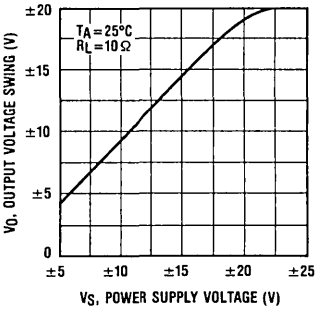
Total Harmonic Distortion vs. Gain



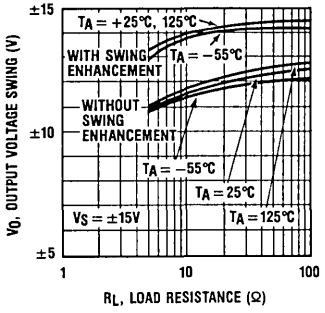
Equivalent Input Noise Voltage



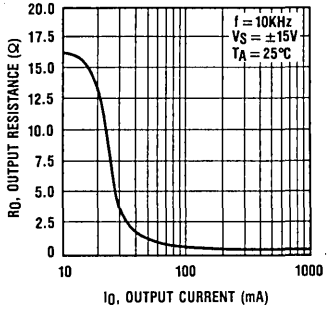
Output Voltage Swing with Swing Enhancement



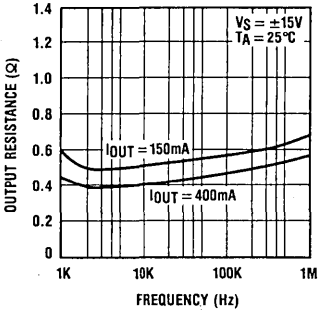
Output Voltage Swing vs. Load Resistance



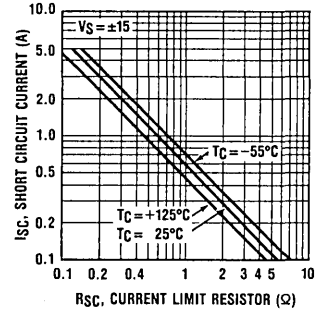
Open-Loop Output Resistance

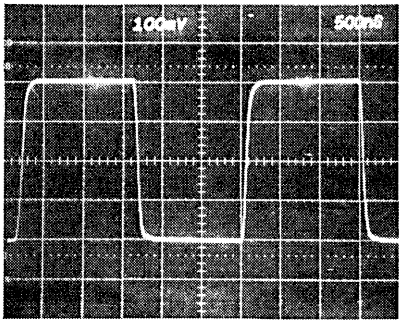


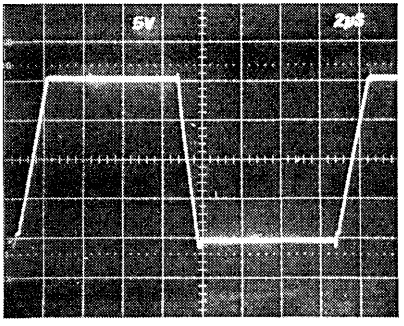
Open-Loop Output Resistance vs. Frequency



Short Circuit Current vs. R_{SC}







Application Hints

Input Voltages

The LH0101 operational amplifier contains JFET input devices which exhibit high reverse breakdown voltages from gate to source or drain. This eliminates the need for input clamp diodes, so that high differential input voltages may be applied without a large increase in input current. However, neither input voltage should be allowed to exceed the negative supply as the resultant high current flow may destroy the unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage may exceed the positive supply by approximately 100 mV, independent of supply voltage and over the full operating temperature range. The positive supply may therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

With the LH0101 there is a temptation to remove the bias current compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than 3V. The potential problem involves loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the inputs of the device is not limited to less than 100 mA or if there is much more than 1 μF bypass on the supply buss.

Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LH0101.

Layout Considerations

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs.

Electrostatic shielding of high impedance circuitry is advisable.

Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients.

Since the LH0101 can deliver large output currents, careful attention should be paid to power supply, power supply bypassing and load currents. Incorrect grounding of signal inputs and load can cause significant errors.

Every attempt should be made to achieve a single point ground system as shown in the figure below.

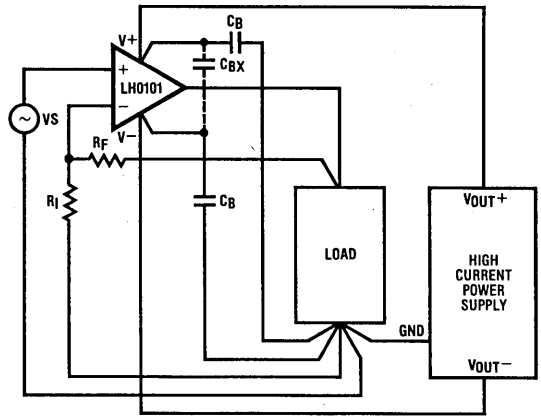


FIGURE 1. Single-Point Grounding

Bypass capacitor C_{BX} should be used if the lead lengths of bypass capacitors C_B are long. If a single point ground system is not possible, keep signal, load, and power supply from intermingling as much as possible. For further information on proper grounding techniques refer to "Grounding and Shielding Techniques in Instrumentation" by Morrison, and "Noise Reduction Techniques in Electronic Systems" by Ott (both published by John Wiley and Sons).

Leads or PC board traces to the supply pins, short-circuit current limit pins, and the output pin must be substantial enough to handle the high currents that the LH0101 is capable of producing.

Short Circuit Current Limiting

Should current limiting of the output not be necessary, SC+ should be shorted to V+ and SC− should be shorted to V−. Remember that the short circuit current limit is dependent upon the total resistance seen between the supply and current limit pins. This total resistance includes the desired resistor plus leads, PC Board traces, and solder joints.* Assuming a zero TCR current limit resistor, typical temperature coefficient of the short circuit will be approximately .3%.

*Short circuit current will be limited to approximately $\frac{0.6}{RSC}$.

Thermal Resistance

The thermal resistance between two points of a conductive system is expressed as:

$$\theta_{12} = \frac{T_1 - T_2}{P_D} °C/W$$

where subscript order indicates the direction of heat flow. A simplified heat transfer circuit for a cased semiconductor and heat sink system is shown in the figure below.

The circuit is valid only if the system is in thermal equilibrium (constant heat flow) and there are, indeed, single specific temperatures T_J, T_C, and T_S (no temperature distribution in junction, case, or heat sink). Nevertheless, this is a reasonable approximation of actual performance.

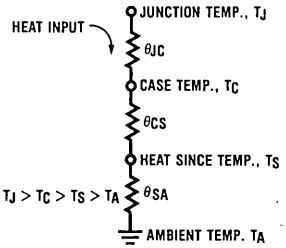


FIGURE 2. Semiconductor-Heat Sink Thermal Circuit

The junction-to-case thermal resistance θ_{JC} specified in the data sheet depends upon the material and size of the package, die size and thickness, and quality of the die bond to the case or lead frame. The case-to-heat sink thermal resistance θ_{CS} depends on the mounting of the device to the heat sink and upon the area and quality of the contact surface. Typical θ_{CS} for a TO-3 package is 0.5 to 0.7°C/W, and 0.3 to 0.5°C/W using silicone grease.

The heat sink to ambient thermal resistance θ_{SA} depends on the quality of the heat sink and the ambient conditions

Cooling is normally required to maintain the worst case operating junction temperature T_J of the device below the specified maximum value $T_{J(MAX)}$. T_J can be calculated from known operating conditions. Rewriting the above equation, we find:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} °C/W$$

$$T_J = T_A + P_D\theta_{JA}°C$$

Where: $P_D = (V_S - V_{OUT})I_{OUT} + |V+ - (V-)|I_Q$

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ and V_S = Supply Voltage

θ_{JC} for the LH0101 is about 2°C/W.

Stability and Compensation

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequncy of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time consistant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Some inductive loads may cause output stage oscillation. A .01μF ceramic capacitor in series with a 10Ω resistor from the output to ground will usually remedy this situation.

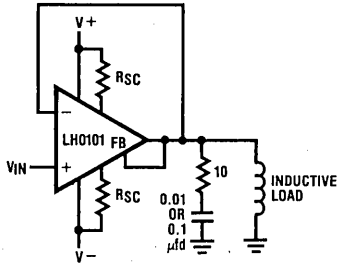


FIGURE 3. Driving Inductive Loads

Capacitive loads may be compensated for by traditional techniques. (See "Operational Amplifiers: Theory and Practice" by Roberge, published by Wiley):

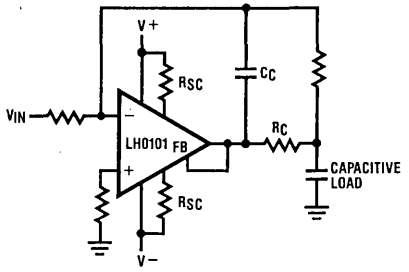


FIGURE 4. R_C and C_C Selected to Compensate for Capacitive Load

A similar but alternative technique may be used for the LH0101:

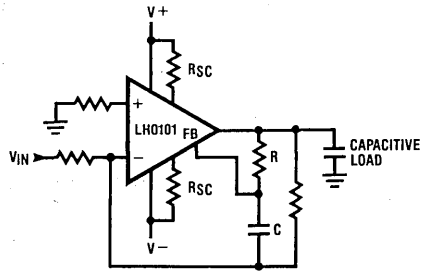


FIGURE 5. Alternate Compensation for Capacitive Load

Output Swing Enhancement

When the feedback pin is connected directly to the output, the output voltage swing is limited by the driver stage and not by output saturation. Output swing can be increased as shown by taking gain in the output stage as shown in High Power Voltage Follower with Swing Enhancement below. Whenever gain is taken in the output stage, as in swing enhancement, either the output stage, or the entire op amp must be appropriately compensated to account for the additional loop gain.

Output Resistance

The open loop output resistance of the LH0101 is a function of the load current. No load output resistance is approximately 10Ω. This decreases to under an ohm for load currents exceeding 100mA.

Typical Applications

See AN261 for more information

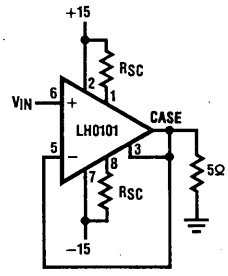


FIGURE 6. High Power Voltage Follower

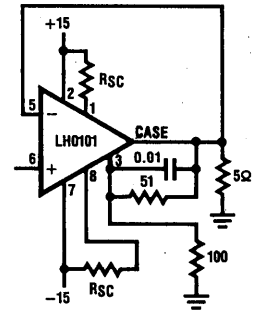


FIGURE 7. High Power Voltage Follower with Swing Enhancement

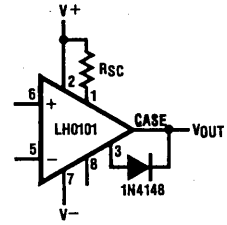


FIGURE 8. Restricting Outputs to Positive Voltages only

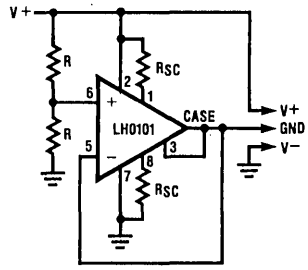


FIGURE 9. Generating a Split Supply from a Single Voltage Supply

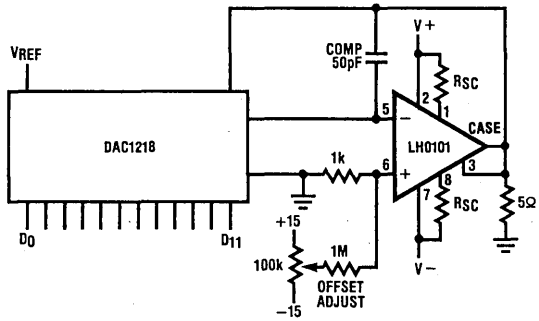


FIGURE 10. Power DAC

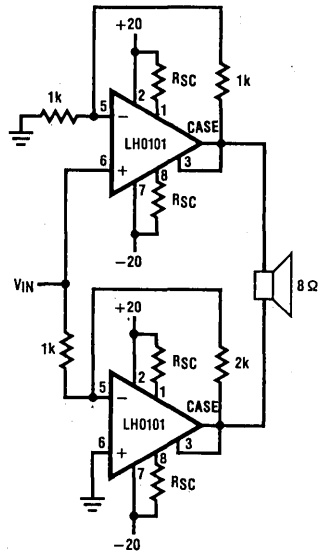


FIGURE 11. Bridge Audio Amplifier

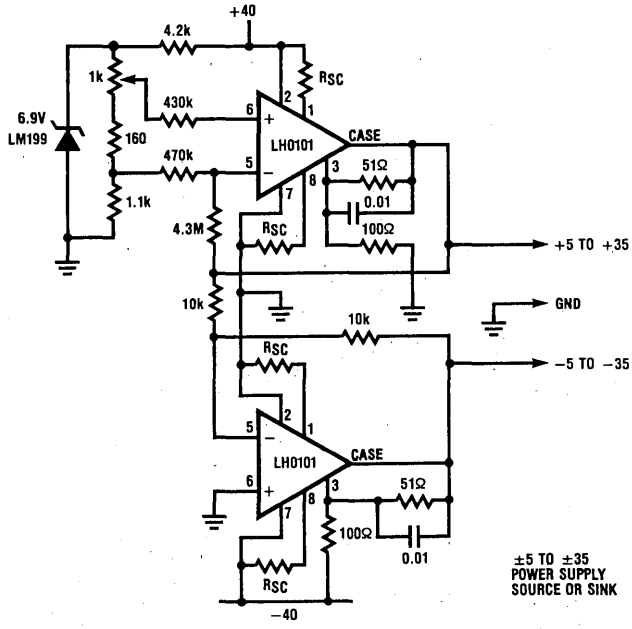


FIGURE 12. ±5 to ±35 Power Source or Sink

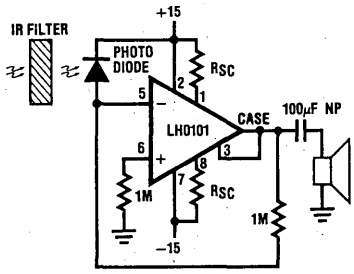


FIGURE 13. Remote Loudspeaker via Infrared Link

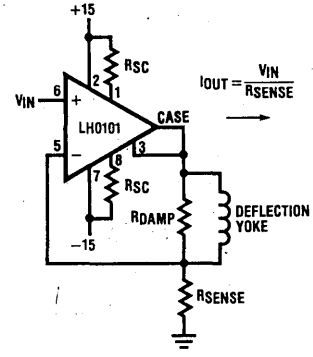


FIGURE 14. CRT Deflection Yoke Driver

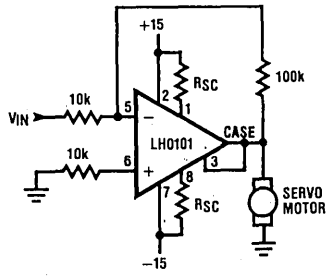


FIGURE 15. DC Servo Amplifier

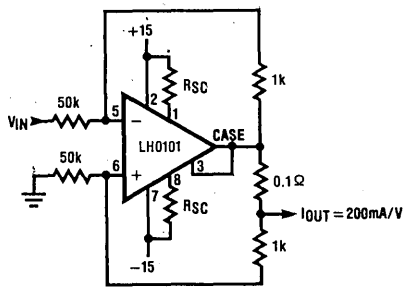


FIGURE 16. High Current Source/Sink

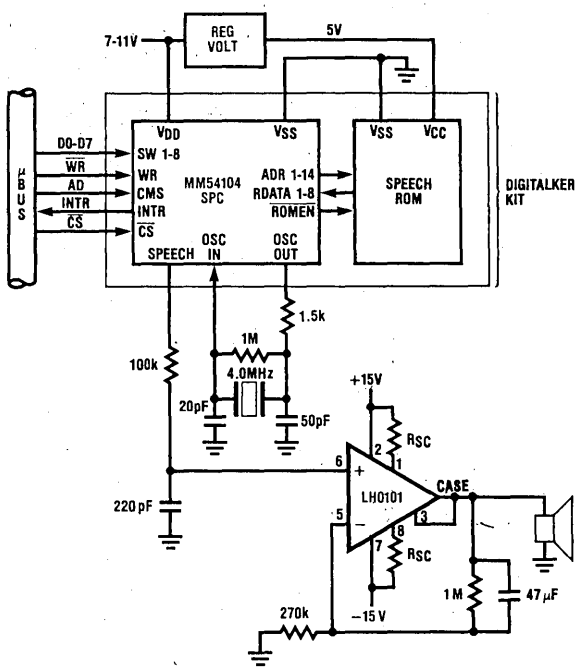


FIGURE 17. "DIGISHOUTER"

National Semiconductor

LH740A/LH740AC FET Input Operational Amplifier

General Description

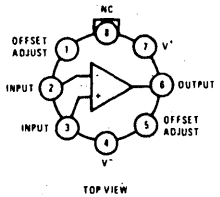
The LH740A/LH740AC is a FET input, general purpose operational amplifier with high input impedance, closely matched input characteristics, and good slew rates. Input offset voltage is typically 10.0 mV at 25°C, while input bias current is less than 100 pA at 25°C. Offset current is typically less than 40 pA at 25°C. Other important design features include:

- Internal 6 dB/octave frequency compensation
- Unity gain slew rate in excess of 6 V/μs
- Unity gain bandwidth of 1 MHz
- Input offset is adjustable with a single 10k pot
- Pin compatible with LM741, LM709, LM101A.
- Excellent offset current match over temperature, typically 100 pA
- Output is continuously short-circuit proof
- Excellent open loop gain, typically in excess of 100 dB
- Guaranteed over the full military temperature range

The LH740A/LH740AC is intended to fulfill a wide variety of applications requiring extremely low bias currents such as integrators, sample and hold amplifiers, and general purpose operational amplifier applications.

The LH740A is specified for operation over the -55°C to +125°C military temperature range. The LH740AC is specified for operation over the 0°C to +85°C temperature range.

Connection Diagram

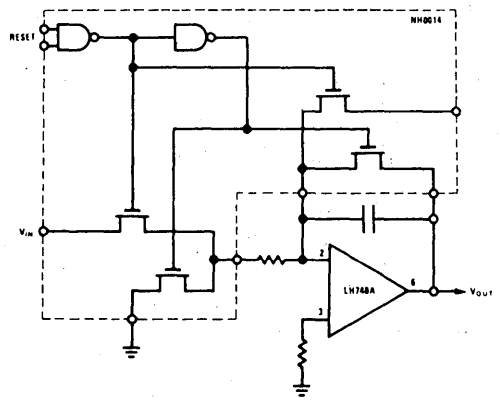


TOP VIEW

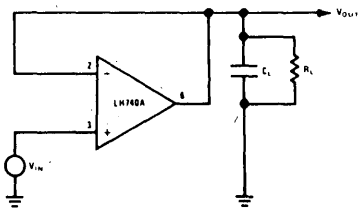
Order Number LH740AH or LH740ACH
See Package H08A

Typical Applications

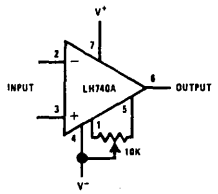
Integrator



Transient Response



Offset Null



Absolute Maximum Ratings

Supply Voltage		±22V
Maximum Power Dissipation		500 mW
Differential Input Voltage		±5V
Input Voltage		±15V
Short Circuit Duration		Continuous
Operating Temperature Range	LH740A	-55°C to +125°C
	LH740AC	0°C to +85°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (soldering, 10 sec.)		300°C

Electrical Characteristics (Note 1) ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted)

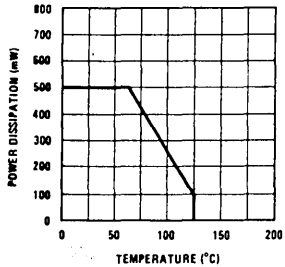
PARAMETER	CONDITIONS	LH740A MIN	LH740A TYP	LH740A MAX	LH740AC MIN	LH740AC TYP	LH740AC MAX	UNITS
Input Offset Voltage	$R_S \leq 100\ k\Omega$		10	15		10	20	mV
Input Offset Current	$T_J = 25°C$ (Note 2)		40	100		60	150	pA
Input Current (either input)	$T_J = 25°C$ (Note 2)		100	200		100	500	pA
Input Resistance	$T_J = 25°C$ (Note 2)		1,000,000			1,000,000		MΩ
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10V$	50,000	100,000		50,000	100,000		V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			20			20		mA
Common Mode Rejection Ratio		80			80			dB
Supply Voltage Rejection Ratio		80			80			dB
Supply Current			3.0	4.0		3.0	4.0	mA
Slew Rate			6.0			6.0		V/μs
Unity Gain Bandwidth			1.0			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100\ pF$, $R_L = 2\ k\Omega$, $V_{IN} = 100\ mV$							
Risetime			110			300		ns
Overshoot			10	20		10		%
(These specifications apply for $-55°C \leq T_A \leq 125°C$ for the LH740A and $0°C \leq T_A \leq 85°C$ for the LH740AC unless otherwise noted.)								
Input Voltage Range		±12			±12			V
Common Mode Rejection Ratio		80			80			dB
Supply Voltage Rejection Ratio		80			80			dB
Large Signal Voltage Gain		40,000			40,000			V/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		V
Input Offset Voltage			15	20		30		mV
Input Offset Current			100	500		60	500	pA
Input Current (either input)			2.5	4.0		1.1	5.0	nA
Offset Voltage Drift	$R_S \leq 100K$		5.0			5.0		μV/°C

Note 1: For supply voltages less than ±10V, the absolute maximum input voltage is equal to the supply voltage.

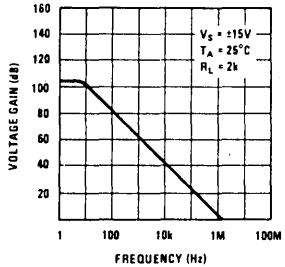
Note 2: Due to high speed automatic testing, these parameters are correlated to junction temperature.

Typical Performance Characteristics

Maximum Power Dissipation



Open Loop Frequency Response



National Semiconductor

LH2011/LH2011B/LH2011C Dual Operational Amplifiers

General Description

The LH2011 series of dual operational amplifiers contain a pair of LM11 op amps in a single hermetic package, combining the best features of existing bipolar and FET op amps. The LH2011 is similar to the LH2108A, except that input currents have been reduced by more than a factor of ten. Offset voltage and drift have also been improved.

Compared to FETs, the device provides inherently lower offset voltage and offset voltage drift, along with at least an order of magnitude better long-term stability. Low frequency noise is also somewhat reduced. Bias current is significantly lower even under laboratory conditions, and the low drift makes compensation practical. Offset current is almost unmeasurable. Although not as fast as FETs, it does have a much lower power drain. This low dissipation has the added advantage of eliminating warm up time in critical applications.

Typical characteristics for 25°C (**– 55°C** to **125°C**) are:

- Offset voltage: 100 μV (**200 μV**)
- Bias current: 25 pA (**65 pA**)
- Offset current: 0.5 pA (**3 pA**)
- Temperature drift: **1 μV/°C**
- Long-term stability: 10 μV/year

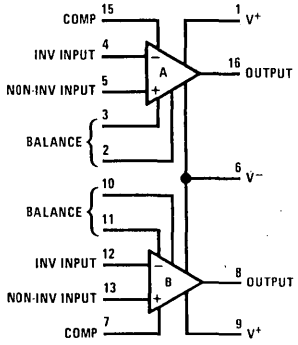
The LH2011 is internally compensated, but external compensation may be added for improved frequency stability, particularly with capacitive loads. Offset voltage balancing is also provided, with the balance range determined by a low-resistance potentiometer.

Otherwise, the device is the electrical equivalent of the LH2108, except that the negative common-mode limit is 0.6V less, performance is specified down to ±2.5V and the guaranteed output drive has been increased to ±2 mA. The input noise is somewhat higher, but amplifier noise is obscured by resistor noise with higher source resistances.

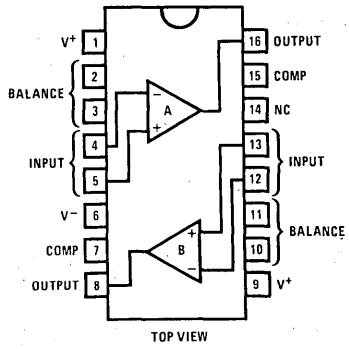
The LH2011 has applications as electrometer amplifiers, charge integrators, analog memories, low frequency active filters or for frequency shaping in slow servo loops. It can be substituted for existing circuits to provide improved performance or eliminate trimming operations. The greater precision can also be used to extend the dynamic range of logarithmic amplifiers, light meters and solid-state particle detectors.

The LH2011 is manufactured with standard bipolar processing using super-gain transistors.

Connection Diagrams

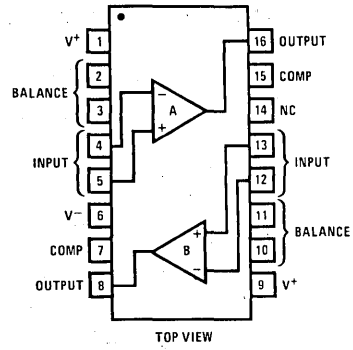


Dual-In-Line Package



Order Number LH2011D, LH2011BD, or LH2011CD
See Package D16C

Flat Package



Order Number LH2011F or LH2011BF
See Package F16B

Absolute Maximum Ratings

V_S	Total Supply Voltage	40V
I_{IN}	Input Current (Note 1)	± 10 mA
P_D	Power Dissipation at 25°C Derate Linearly above 100°C at 100°C/W	500 mW
I_{SC}	Output Short-Circuit Duration (Note 2)	Indefinite
T_J	Junction Temperature	150°C
T_{stg}	Storage Temperature Range	−65°C to +150°C
T_A	Operating Temperature Range	
	LH2011CD	−25°C to +85°C
	LH2011D, LH2011F	−55°C to +125°C
	LH2011BD, LH2011BF	−55°C to +125°C
	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_J \leq T_{MAX}$ unless noted.

Parameter		Conditions		LH2011			LH2011B			LH2011C			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	Note 3	$T_J = 25°C$		0.1	0.3		0.2	0.6		0.5	1	mV
						0.6			1.1			1.3	
I_{OS}	Input Offset Current		$T_J = 25°C$		0.5	10		1	10		4	25	pA
						30			30			50	
I_B	Input Bias Current		$T_J = 25°C$		25	50		40	100		70	180	pA
						150			300			400	
R_{IN}	Input Resistance				10^{11}			10^{11}			10^{11}		Ω
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift	Note 4			1	3		2	5		3		μV/°C
$\Delta I_B/\Delta T$	Bias Current Drift				0.5	1.5		0.8	3		1.4		pA/°C
$\Delta I_{OS}/\Delta T$	Offset Current Drift				20			20			50		fA/°C
A_V	Large Signal Voltage Gain	$V_S = \pm 15V$, $I_O = \pm 2$ mA	$T_J = 25°C$, $V_O = \pm 12V$	100	300		100	300		50	300		V/mV
		$V_O = \pm 11.5V$		50			50			15			
		$V_S = \pm 15V$, $I_O = \pm 0.5$ mA	$T_J = 25°C$, $V_O = \pm 12V$	250	1200		250	1200		90	800		
		$V_O = \pm 11.5V$		100			100			30			
CMRR	Common-Mode Rejection		$T_J = 25°C$	110	130		110	130		96	110		dB
		$V_{CM} = -13V, +14V$		100			100			90			
PSRR	Power Supply Rejection Ratio		$T_J = 25°C$	100	118		100	118		84	100		dB
		$V_S = \pm 2.5V$ to $\pm 20V$		96			96			80			
I_S	Supply Current		$T_J = 25°C$		0.3	0.6		0.3	0.8		0.3	0.8	mA
						0.8			1			1	
I_{SC}	Output Short Circuit Current	$T_J = T_{MAX}$			±15			±15			±15		mA

Note 1: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used. In addition, a 2 kΩ minimum resistance in each input is advised to avoid possible latch-up initiated by supply reversals.

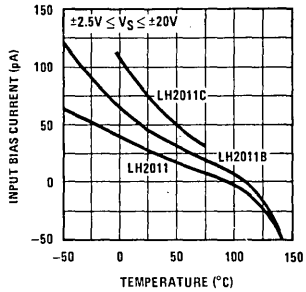
Note 2: Current limiting protects the output when it is shorted to ground or any voltage less than the supplies. With continuous overloads, package dissipation must be taken into account and heat sinking provided when necessary.

Note 3: These specifications apply for test at $V_S = \pm 15V$ and $V_{CM} = -12.5V$ (−13V at 25°C), 14V; $V_S = \pm 20V$ and $V_{CM} = 0V$; in addition, V_{OS} is also tested at $V_S = \pm 2.5V$ and $V_{CM} = 0V$.

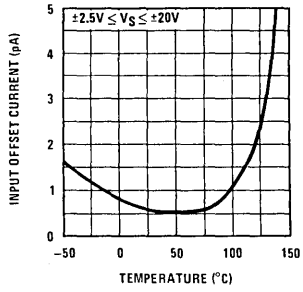
Note 4: Drift parameters are sample tested to 5% LTPD at the same conditions as Note 3. The values are average-calculated from measurements at 25°C and 125°C.

Typical Characteristics (for single device)

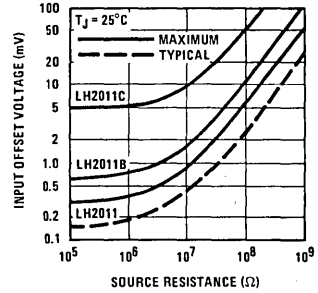
Input Bias Current



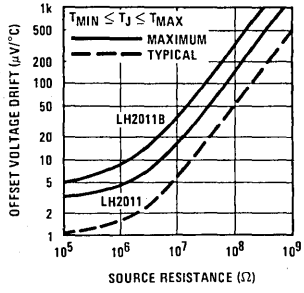
Input Offset Current



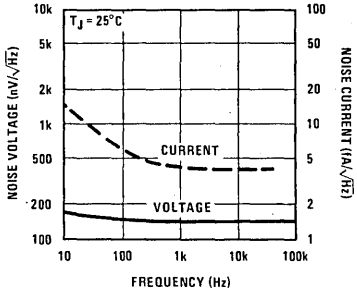
Offset: Single Source Resistor (Unbalanced)



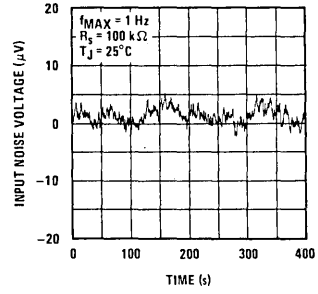
Drift: Single Source Resistor (Unbalanced)



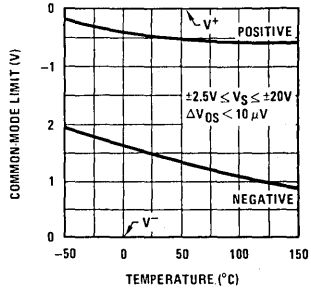
Equivalent Input Noise



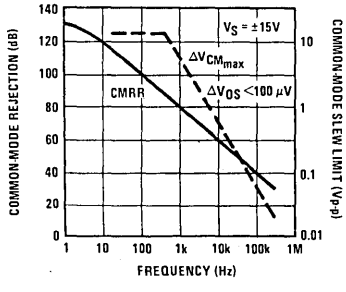
Input Noise



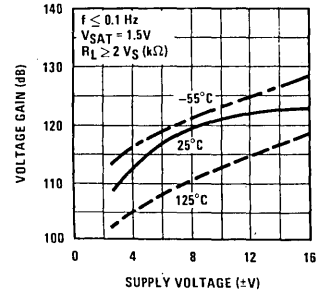
Input Common-Mode Limits



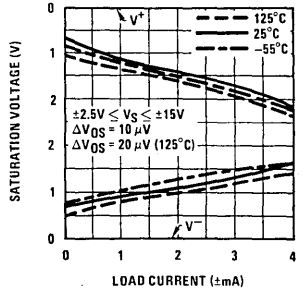
Common-Mode Rejection



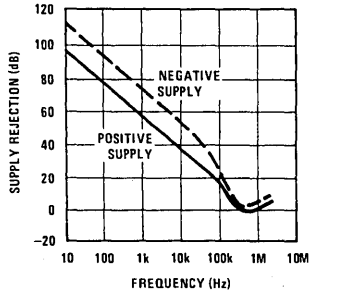
Large Signal Voltage Gain



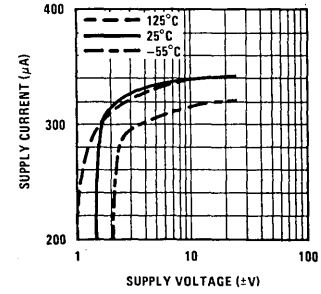
Output Saturation Threshold



Supply Rejection

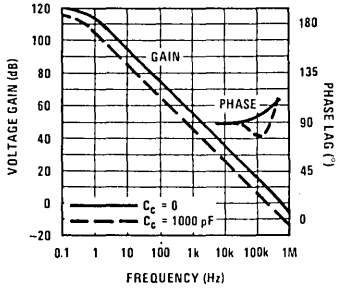


Supply Current (Each Amplifier)

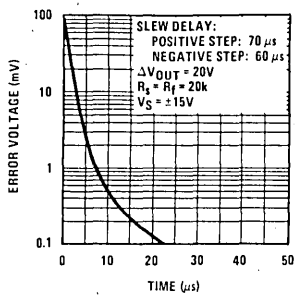


Typical Characteristics (Continued) (for single device)

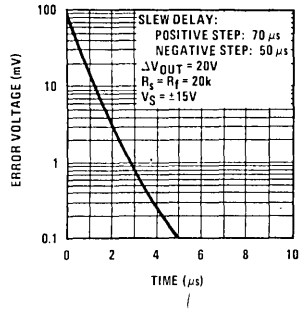
Open Loop Response



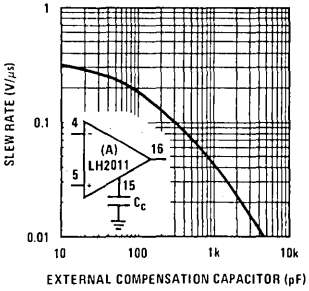
Follower Settling Time



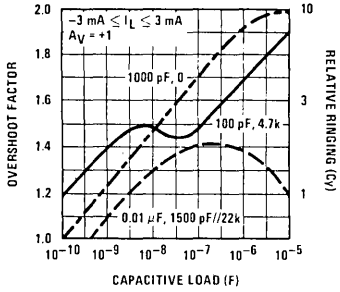
Inverter Settling Time



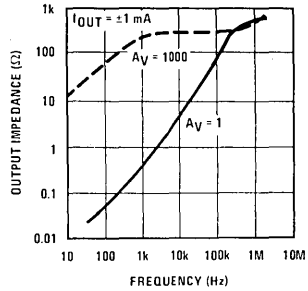
Slew Rate



Stability with Over-Compensation



Closed Loop Output Impedance



Application Hints

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs. For critical applications, the floating metal lid is best connected to the guard. This might be accomplished with a dab of conductive paint connecting the metal lid to the "no-connection" pin 14.

Electrostatic shielding of high impedance circuitry is advisable.

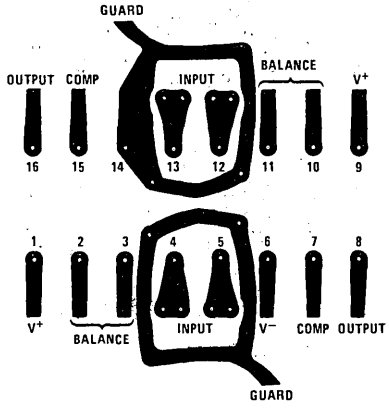
Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients. The most troublesome thermocouples are the junction of the IC package and the printed circuit board (35 µV/°C for copper-kovar) and internal resistor connections. Problems can be avoided by keeping low level circuitry away from heat generating elements. Mounting the IC directly to the PC board while keeping package leads short and the input leads close together can also help.

With the LH2011 there is a temptation to remove the bias-current-compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than about 3V. The potential problem involves the loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the input of the device is not limited to less than 100 mA or if there is much more than 1 µF bypass on the supply buss.

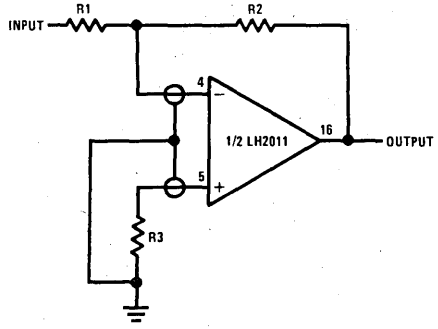
Although these difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LH2011.

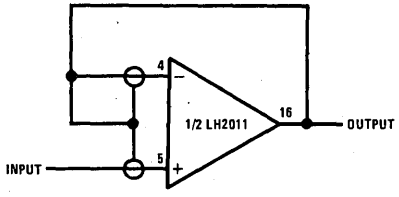
Input Guarding

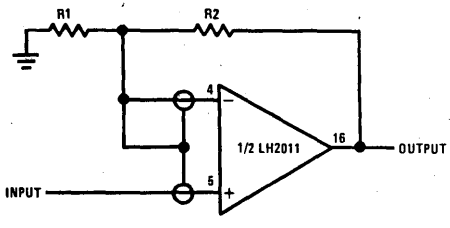
Input guarding can drastically reduce surface leakage. Layout for the LH2011 is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.



Guard ring is connected to low impedance point at same potential as sensitive input leads. Connections for various op amp configurations are shown here.

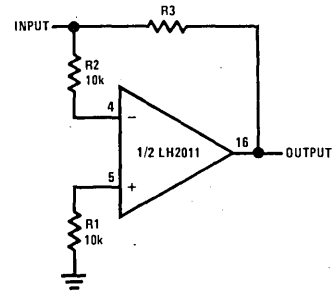




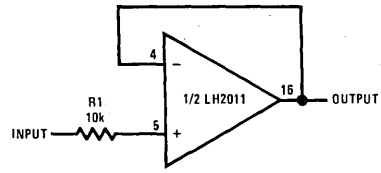


Input Protection

Current is limited by R2 even when input is connected to voltage source outside common-mode range. If one supply reverses, current is limited by R1. These resistors do not affect normal operation.

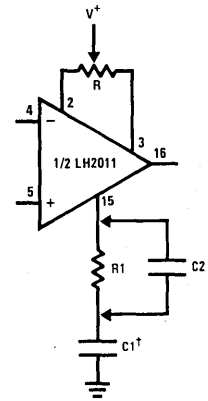


Input resistor limits current when input exceeds supply voltages, when power for op amp is turned off or when output is shorted.



Balancing and Over-Compensation

Over-compensation will improve stability with capacitive loading (see curves). Offset voltage adjustment range is determined by balance potentiometer resistance as indicated in the table.

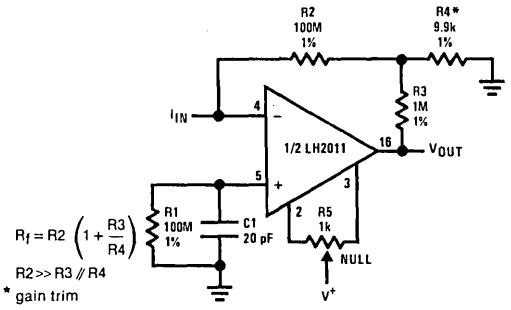


Min Adj Range	R
±5 mV	100 kΩ
±2	10k
±1	3k
±0.8	3k
±0.4	1k

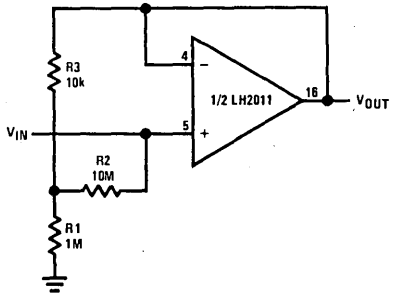
†See stability with over-compensation curve

Resistance Multiplication

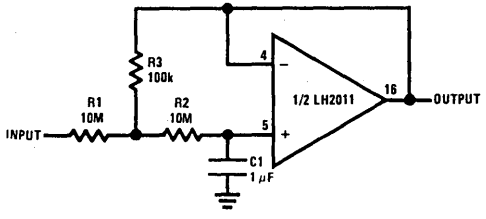
Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.



Follower input resistance is 1 GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not significant because the op amp offset is low.



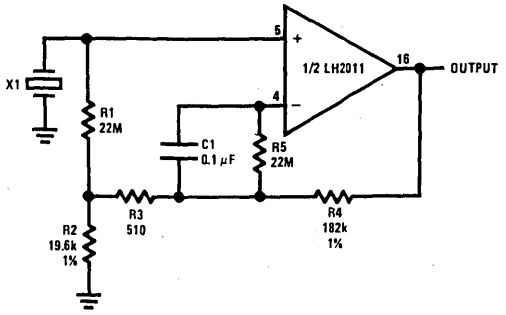
This circuit multiplies RC time constant to 1000 seconds and provides low output impedance.



$$\tau = \frac{R1\,C}{R3}(R2+R3)$$

$$\Delta V_{OUT} = \frac{R1+R3}{R3}(I_B R2 + V_{OS})$$

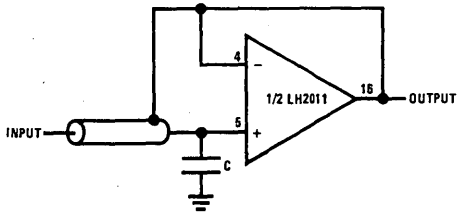
A high-input-impedance ac amplifier for a piezoelectric transducer. Input resistance of 880 MΩ and gain of 10 is obtained.



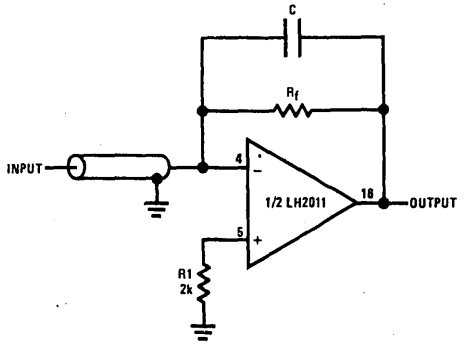
$$R_{IN} = R1\left(1+\frac{R2}{R3}\right) \quad A_V = \frac{R2+R3+R4}{R2+R3}$$

Cable Bootstrapping

Bootstrapping input shield for a follower reduces cable capacitance, leakage, and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.



With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.

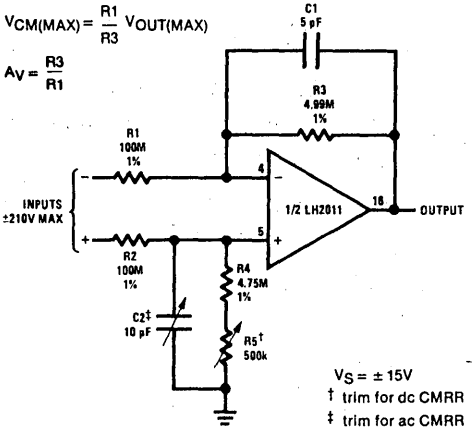


Differential Amplifiers

This differential amplifier handles high input voltages. Resistor mismatches and stray capacitors should be balanced out for best common-mode rejection.

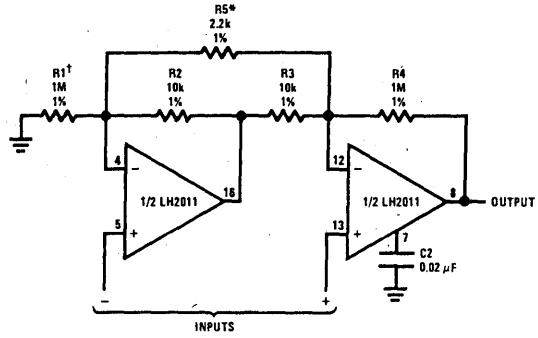
$V_{CM(MAX)} = \frac{R1}{R3} V_{OUT(MAX)}$

$A_V = \frac{R3}{R1}$



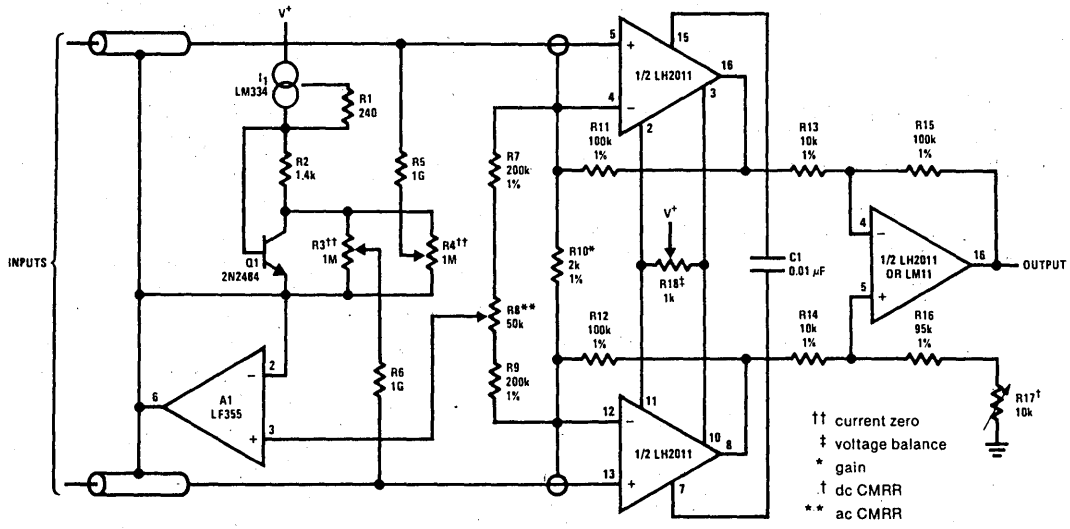
$V_S = \pm 15V$
† trim for dc CMRR
‡ trim for ac CMRR

Two op-amp instrumentation amplifier has poor ac common-mode rejection. This can be improved at the expense of differential bandwidth with C2.

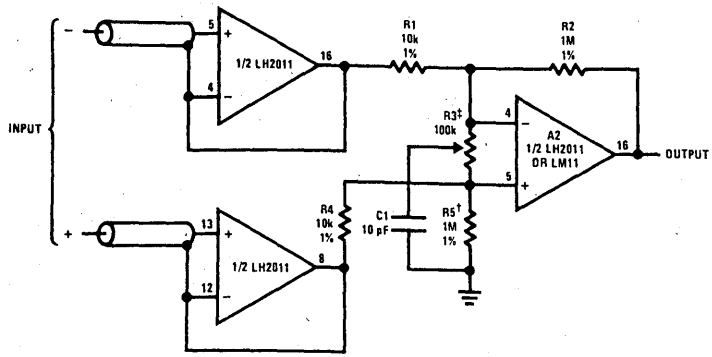


* gain set
† trim for dc CMRR
$f_O = 10$ Hz

High gain differential instrumentation amplifier includes input guarding, cable bootstrapping and bias current compensation. Differential bandwidth is reduced by C1 which also makes common-mode rejection less dependent on matching of input amplifiers.



For moderate-gain instrumentation amplifiers, input amplifiers can be connected as followers. This simplifies circuitry, but A2 must also have low drift.



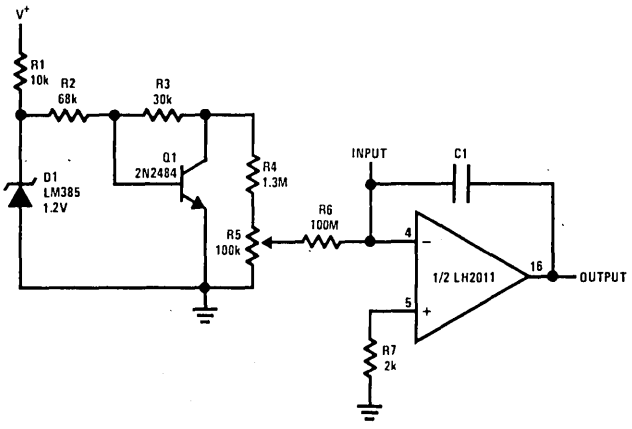
$R1 = R3;\ R2 = R4$

$A_V = \frac{R2}{R1}$

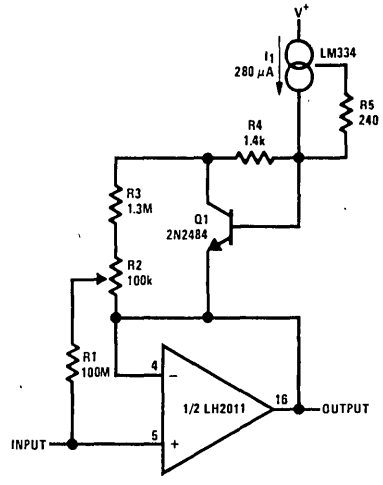
†trim for dc CMRR
‡set for ac CMRR

Bias Current Compensation

Precise bias current compensation for use with unregulated supplies. Reference voltage is available for other circuitry.

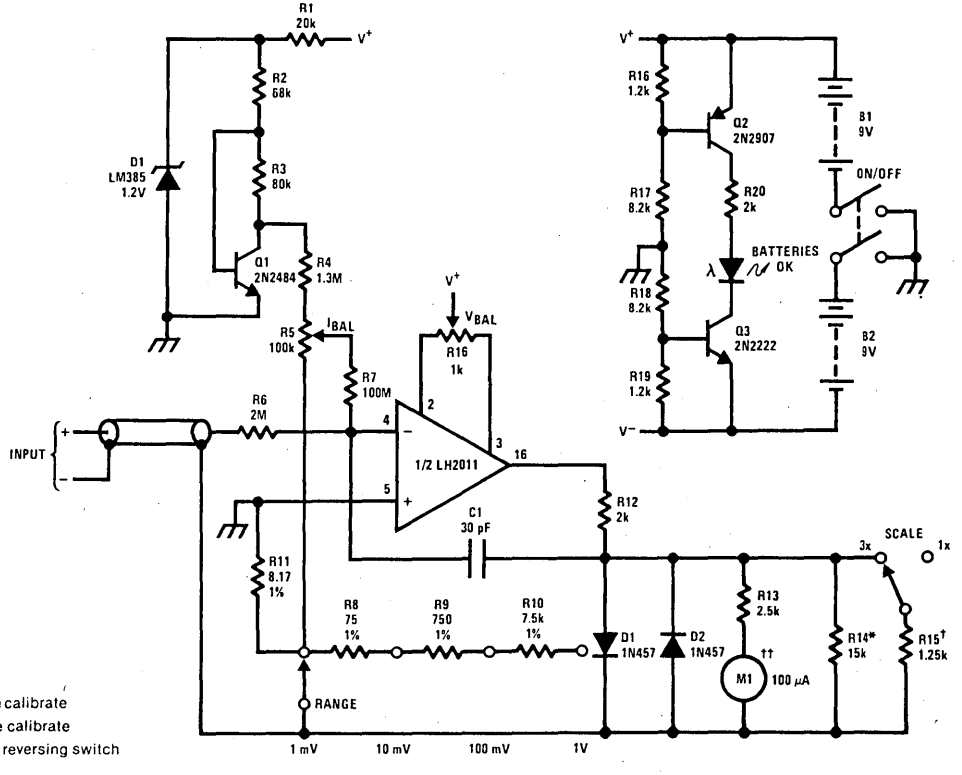


This circuit shows how bias current compensation can be used on a voltage follower.



Voltmeter

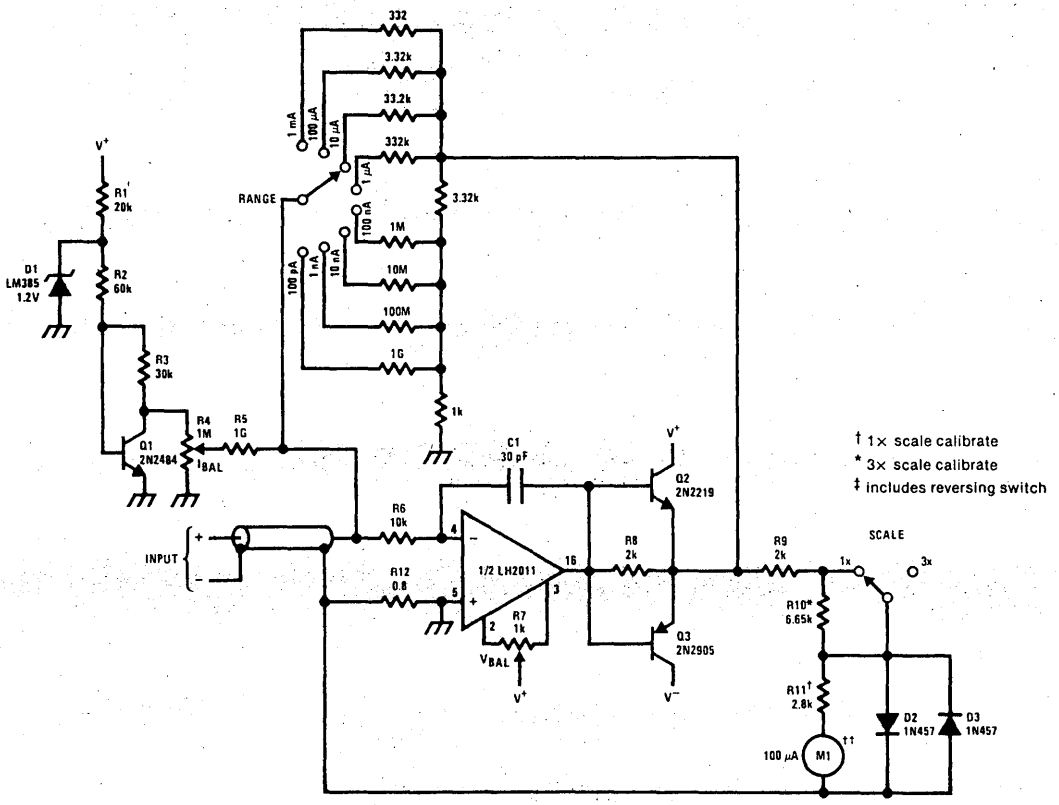
High-input-impedance millivoltmeter. Input current is proportional to input voltage, about 10 pA at full-scale. Reference could be used to make direct reading linear ohmmeter.



* 1× scale calibrate
† 3× scale calibrate
‡ includes reversing switch

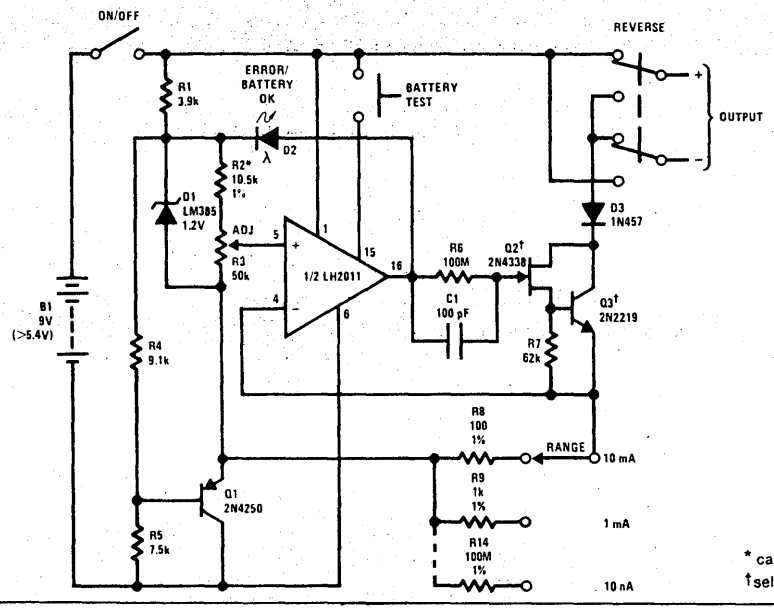
Ammeter

Current meter ranges from 100 pA to 3 mA full-scale. Voltage across input is 100 μV at lower ranges rising to 3 mV at 3 mA. Buffers on op amp are to remove ambiguity with high-current overload. Output can also drive DVM or DPM.



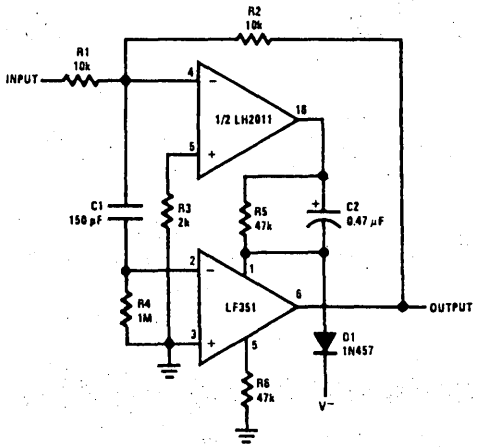
Current Source

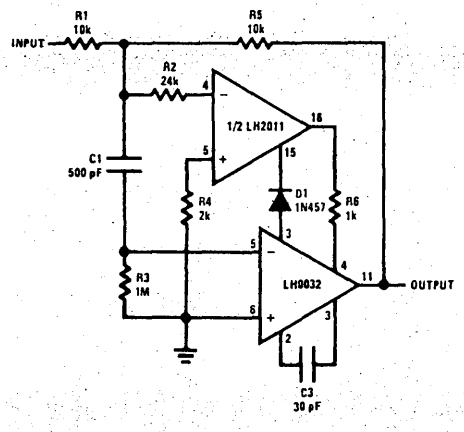
Precision current source has 10 μA to 10 mA ranges with output compliance of 30V to −5V. Output current is fully adjustable on each range with a calibrated, ten-turn potentiometer. Error light indicates saturation.



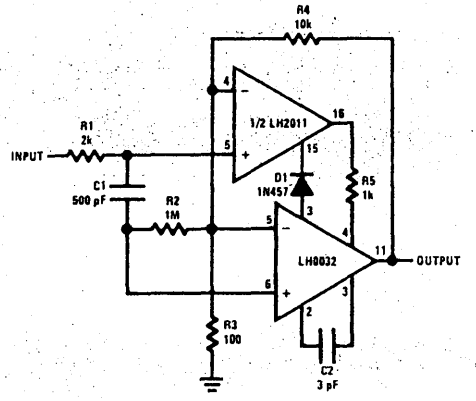
Fast Amplifiers

These inverters have bias current and offset voltage of LH2011 along with speed of the FET op amps. Open loop gain is about 140 dB and settling time to 1 mV about 8 μs. Overload-recovery delay can be eliminated by direct coupling the FET amplifier to summing node.

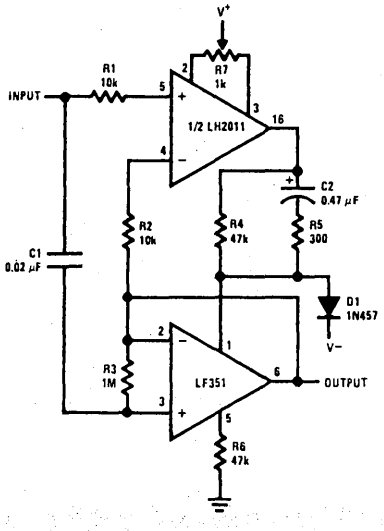




This 100× amplifier has small and large signal bandwidth of 1 MHz. The LH2011 greatly reduces offset voltage, bias current and gain error. Eliminating long recovery delay for greater than 100% overload requires direct coupling of A2 to input.

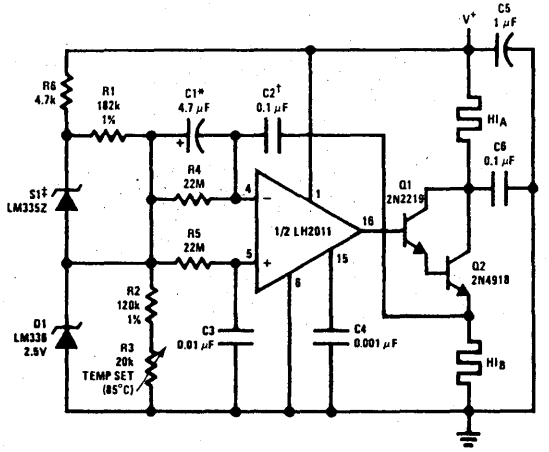


Follower has 10 μs settling to 1 mV, but signal repetition frequency should not exceed 10 kHz if the FET amplifier is ac coupled to input. The circuit does not behave well if common-mode range is exceeded.



Heater Control

Proportional control crystal oven heater uses lead/lag compensation for fast settling. Time constant is changed with R4 and compensating resistor R5. If Q2 is inside oven, a regulated supply is recommended for 0.1°C control.



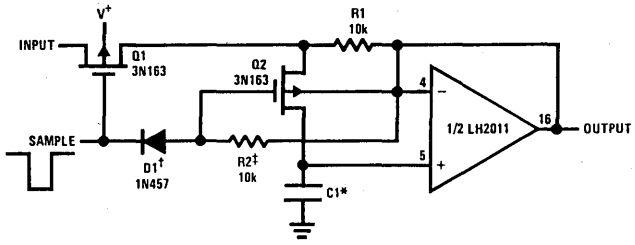
* solid tantalum

† mylar

‡ close thermal coupling between sensor and oven shell is recommended.

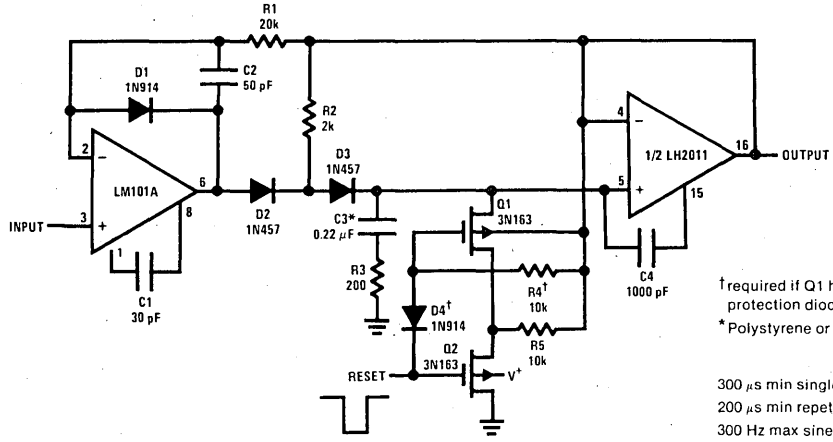
Leakage Isolation

Switch leakage in this sample and hold does not reach storage capacitor.



* Polystyrene or Teflon
† required if protected-gate switch is used

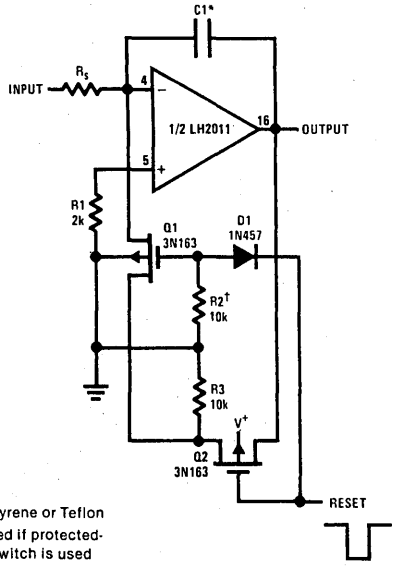
A peak detector designed for extended hold. Leakage currents of peak-detecting diodes and reset switch are absorbed before reaching storage capacitor.



† required if Q1 has gate-protection diode
* Polystyrene or Teflon

300 μs min single pulse
200 μs min repetitive pulse
300 Hz max sine wave error < 5 mV

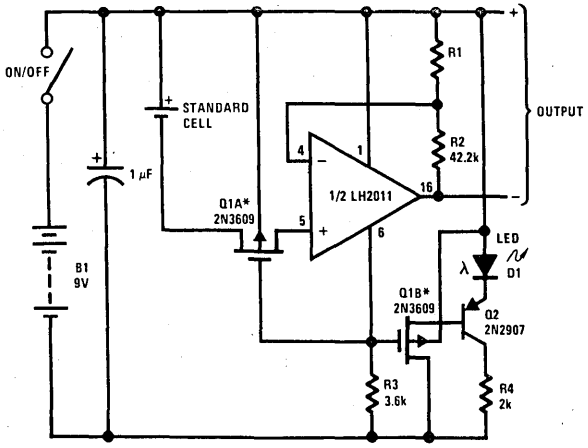
Reset is provided for this integrator and switch leakage is isolated from the summing junction. Greater precision can be provided if bias-current compensation is included.



* Polystyrene or Teflon
† required if protected-gate switch is used

Standard-Cell Buffer

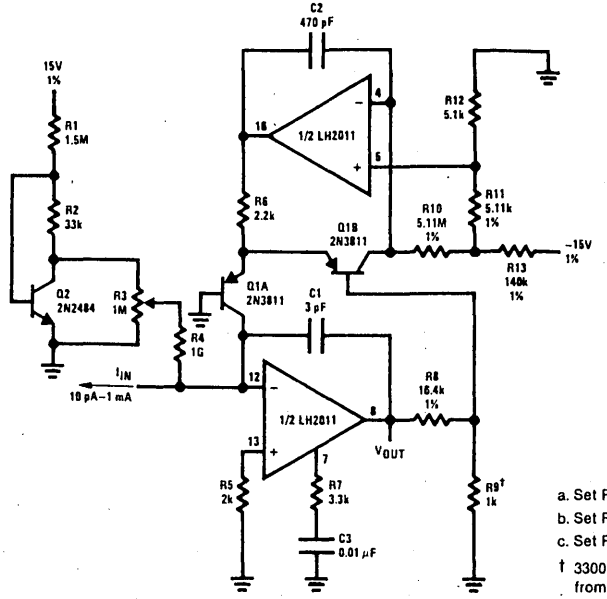
Battery powered buffer amplifier for standard cell has negligible loading and disconnects cell for low supply voltage or overload on output. Indicator diode extinguishes as disconnect circuitry is activated.



* cannot have gate-protection diode; $V_{TH} > V_{OUT}$

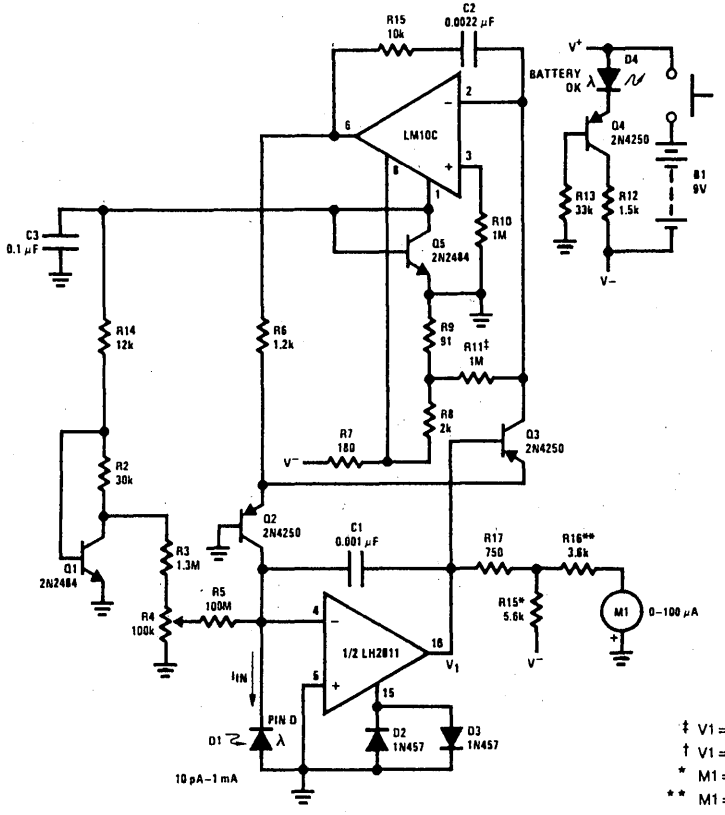
Logarithmic Amplifiers

Unusual frequency compensation gives this logarithmic converter a 100 μs time constant from 1 mA down to 100 μA, increasing from 200 μs to 200 ms from 10 nA to 10 pA. Optional bias current compensation can give 10 pA resolution from −55°C to 100°C. Scale factor is 1V/decade and temperature compensated.



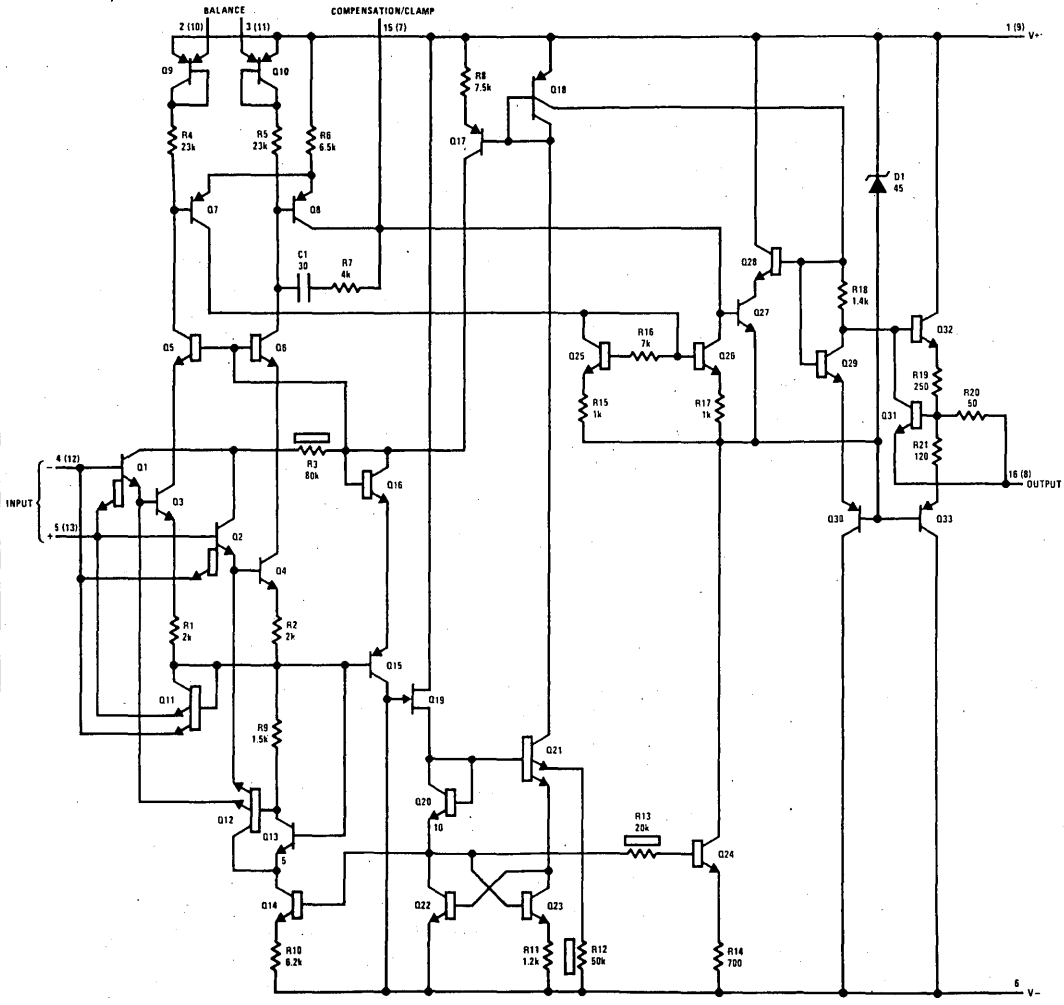
a. Set R11 for $V_{OUT} = 0$ at $I_{IN} = 100\ \mu A$
b. Set R8 for $V_{OUT} = 3V$ at $I_{IN} = 100\ \mu A$
c. Set R3 for $V_{OUT} = -4V$ at $I_{IN} = 10$ pA
† 3300 ppm/°C. Type Q209 available from Tel Labs, Inc., Manchester, N.H.

Light meter has eight-decade range. Bias current compensation can give input current resolution of better than ±2 pA over 15°C to 55°C.



‡ $V1 = 0$ @ $I_{IN} = 100$ nA
† $V1 = -0.24V$ @ $I_{IN} = 10$ pA
* $M1 = 0$ @ $I_{IN} = 10$ pA
** $M1 = f_S$ @ $I_{IN} = 1$ mA

Schematic Diagram (for single device)



Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the output is unloaded in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Temperature drift: The change of a parameter measured at 25°C and either temperature extreme divided by the temperature change.

Supply-voltage rejection: The ratio of the specified supply-voltage change (either or both supplies) to the change in offset voltage between the extremes.

Supply current: The current required from the power source to operate the amplifier with the output unloaded and operating in the linear range.

National Semiconductor

LH2101A/LH2201A/LH2301A Dual High Performance Op Amp

General Description

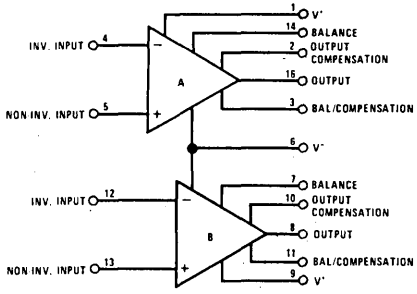
The LH2101A series of dual operational amplifiers are two LM101A type op amps in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two singles. For additional information, see the LM101A data sheet and National's Linear Application Handbook.

The LH2101A is specified for operation over the −55°C to +125°C military temperature range. The LH2201A is specified for operation over the −25°C to +85°C temperature range. The LH2301A is specified for operation over the 0°C to +70°C temperature range.

Features

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

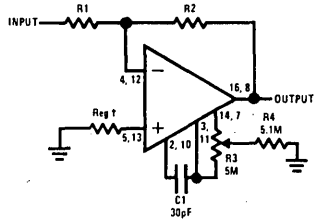
Connection Diagram



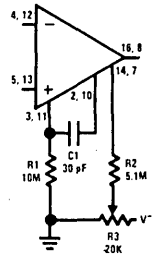
Order Number LH2101AD or LH2201AD or LH2301AD, see Package D16C
LH2101AF, LH2201AF, LH2301AF, see Package F16B
LH2101AJ, LH2201AJ, LH2301AJ, see Package J16A

Auxiliary Circuits

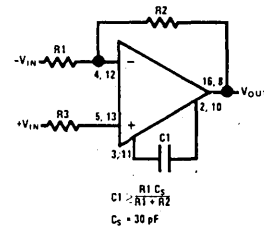
Inverting Amplifier with Balancing Circuit



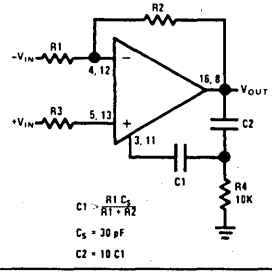
Alternate Balancing Circuit



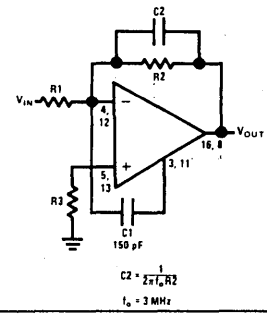
Single Pole Compensation



Two Pole Compensation



Feedforward Compensation



Absolute Maximum Ratings

Supply Voltage	±22V	Operating Temperature Range	LH2101A	-55°C to 125°C
Power Dissipation (Note 1)	500 mW		LH2201A	-25°C to 85°C
Differential Input Voltage	±30V		LH2301A	0°C to 70°C
Input Voltage (Note 2)	±15V	Storage Temperature Range		-65°C to 150°C
Output Short-Circuit Duration	Continuous	Lead Temperature (Soldering, 10 sec)		300°C

Electrical Characteristics Each Side (Note 3)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2101A	LH2201A	LH2301A	
Input Offset Voltage	$T_A = 25°C$, $R_S < 50\ k\Omega$	2.0	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	75	75	250	nA Max
Input Resistance	$T_A = 25°C$	1.5	1.5	0.5	MΩ Min
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$	3.0	3.3	3.0	mA Max
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	50	25	V/mV Min
Input Offset Voltage	$R_S \leq 50\ k\Omega$	3.0	3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	15	30	µV/°C Max
Input Offset Current		20	20	70	nA Max
Average Temperature Coefficient of Input Offset Current	$25°C < T_A < 125°C$ $-55°C \leq T_A \leq 25°C$	0.1 0.2	0.1 0.2	0.3 0.6	nA/°C Max nA/°C Max
Input Bias Current		100	100	300	nA Max
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$	2.5	2.5		mA Max
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25	25	15	V/mV Min
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10	±12 ±10	±12 ±10	V Min V Min
Input Voltage Range	$V_S = \pm 20V$	±15	±15	±12	V Min
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	80	70	dB Min
Supply Voltage Rejection Ratio	$R_S < 50\ k\Omega$	80	80	70	dB Min

Note 1: The maximum junction temperature of the LH2101A is 150°C, while that of the LH2201A is 100°C. For operating temperatures of devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LH2201A, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$. For the LH2301A these specifications apply for $0°C \leq T_A \leq 70°C$, and $\pm 5V \leq V_S \leq \pm 15V$. Supply current and input voltage range are specified as $V_S = \pm 15V$ for the LH2301A. $C_1 = 30\ pF$ unless otherwise specified.

National Semiconductor

LH2108/LH2208/LH2308, LH2108A/LH2208A/LH2308A Dual Super Beta Op Amp

General Description

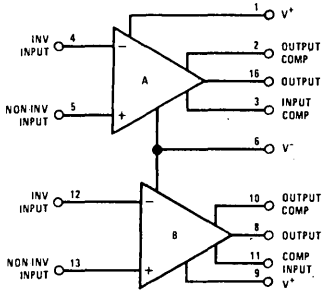
The LH2108A/LH2208A/LH2308A and LH2108/LH2208/LH2308 series of dual operational amplifiers are two LM108A or LM108 type op amps in a single hermetic package. Featuring all the same performance characteristics of the single device, these duals also offer closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two single devices. For additional information see the LM108A or LM108 data sheet and National's Linear Application Handbook.

The LH2108A/LH2108 is specified for operation over the -55°C to +125°C military temperature range. The LH2208A/LH2208 is specified for operation over the -25°C to +85°C temperature range. The LH2308A/LH2308 is specified for operation over the 0°C to +70°C temperature range.

Features

- Low offset current — 50 pA
- Low offset voltage — 0.7 mV
- Low offset voltage — LH2108A 0.3 mV; LH2108 0.7 mV
- Wide input voltage range — ±15V
- Wide operating supply range — ±3V to ±20V

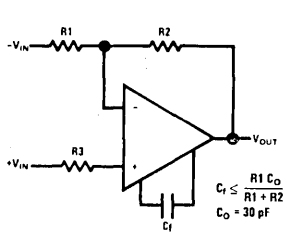
Connection Diagram



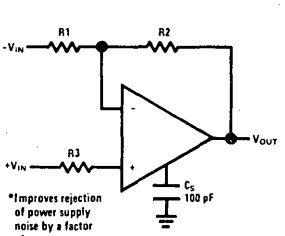
Order Number LH2108AD, LH2208AD, LH2308AD, LH2108D, LH2208D, or LH2308D
See Package D16C
Order Number LH2108AF, LH2208AF, LH2308AF, LH2108F, LH2208F, or LH2308F
See Package F16B
Order Number LH2108AJ, LH2208AJ, LH2308AJ, LH2108J, LH2208J, or LH2308J
See Package J16A

Auxiliary Circuits

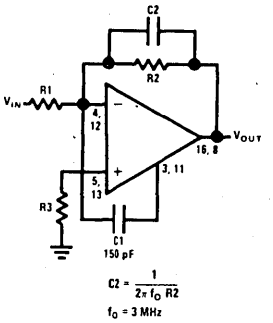
Standard Compensation Circuit



Alternate * Frequency Compensation



Feedforward Compensation



Absolute Maximum Ratings

Supply Voltage	±20V	Operating Temperature Range	
Power Dissipation (Note 1)	500 mW	LH2108A/LH2108	−55°C to +125°C
Differential Input Current (Note 2)	±10 mA	LH2208A/LH2208	−25°C to +85°C
Input Voltage (Note 3)	±15V	LH2308A/LH2308	0°C to +70°C
Output Short Circuit Duration	Continuous	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics each side (Note 4)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2108	LH2208	LH2308	
Input Offset Voltage	T_A = 25°C	2.0	2.0	7.5	mV Max
Input Offset Current	T_A = 25°C	0.2	0.2	1.0	nA Max
Input Bias Current	T_A = 25°C	2.0	2.0	7.0	nA Max
Input Resistance	T_A = 25°C	30	30	10	MΩ Min
Supply Current	T_A = 25°C	0.6	0.6	0.8	mA Max
Large Signal Voltage Gain	T_A = 25°C V_S = ±15V V_{OUT} = ±10V, R_L > 10 kΩ	50	50	25	V/mV Min
Input Offset Voltage		3.0	3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	15	30	μV/°C Max
Input Offset Current		0.4	0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	2.5	10	pA/°C Max
Input Bias Current		3.0	3.0	10	nA Max
Supply Current	T_A = +125°C	0.4	0.4	–	mA Max
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L > 10 kΩ	25	25	15	V/mV Min
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±13	±13	±13	V Min
Input Voltage Range	V_S = ±15V	±13.5	±13.5	±14	V Min
Common Mode Rejection Ratio		85	85	80	dB Min
Supply Voltage Rejection Ratio		80	80	80	dB Min

Electrical Characteristics each side (Note 4)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2108A	LH2208A	LH2308A	
Input Offset Voltage	T_A = 25°C	0.5	0.5	0.5	mV Max
Input Offset Current	T_A = 25°C	0.2	0.2	1.0	nA Max
Input Bias Current	T_A = 25°C	2.0	2.0	7.0	nA Max
Input Resistance	T_A = 25°C	30	30	10	MΩ Min
Supply Current	T_A = 25°C	0.6	0.6	0.8	mA Max
Large Signal Voltage Gain	T_A = 25°C V_S = ±15V V_{OUT} = ±10V, R_L > 10 kΩ	80	80	80	V/mV Min
Input Offset Voltage		1.0	1.0	0.73	mV Max
Average Temperature Coefficient of Input Offset Voltage		5	5	5	μV/°C Max
Input Offset Current		0.4	0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	2.5	10	pA/°C Max
Input Bias Current		3.0	3.0	10	nA Max
Supply Current	T_A = +125°C	0.4	0.4	–	mA Max
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L > 10 kΩ	40	40	60	V/mV Min
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±13	±13	±13	V Min
Input Voltage Range	V_S = ±15V	±13.5	±13.5	±14	V Min
Common Mode Rejection Ratio		96	96	96	dB Min
Supply Voltage Rejection Ratio		96	96	96	dB Min

Note 1: The maximum junction temperature of the LH2108A/LH2108 is 150°C, while that of the LH2208A/LH2208 is 100°C and that of the LH2308A/LH2308 is 85°C. For operating devices in the flat package at elevated temperatures, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ 125°C, unless otherwise specified. With the LH2208A/LH2208, however, all temperature specifications are limited to −25°C ≤ T_A ≤ 85°C and with the LH2308A/LH2308 for ±5V ≤ V_S ≤ 15V and 0°C ≤ T_A ≤ 70°C.

National Semiconductor

LH24250/LH24250C Dual Programmable Micropower Op Amp

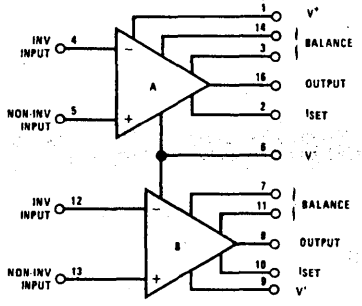
General Description

The LH24250/LH24250C series of dual programmable micropower operational amplifiers are two LM4250 type op amps in a single hermetic package. Featuring all the same performance characteristics of the LM4250, the LH24250/LH24250C duals also offer closer thermal tracking, lower weight, reduced insertion cost and smaller size than two single devices. For additional information, see the LM4250 data sheet and National's Linear Application Handbook.

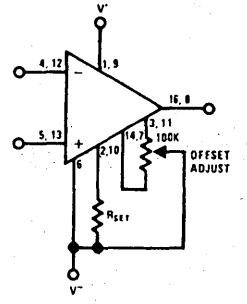
Features

- ±1V to ±18V power supply operation
- Standby power consumption as low as 20 μW
- Offset current programmable from less than 0.5 nA to 30 nA
- Programmable slew rate
- May be shut-down using standard open collector TTL
- Internally compensated and short circuit proof

Connection Diagram and Auxiliary Circuit



Offset Null Circuit



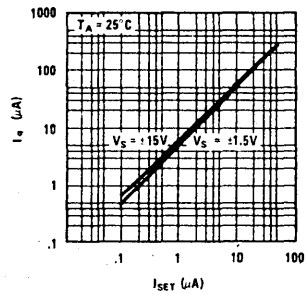
Ordering Information
Order Number LH24250D or LH24250CD, See Package D16C
LH24250F or LH24250CF, See Package F16B
LH24250J or LH24250CJ, See Package J16A

Typical Quiescent Current Setting Resistor

Set Current Setting Resistor to V−

	I_{SET}				
V_S	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

Quiescent Current (I_Q) vs I_{SET}



Absolute Maximum Ratings

Supply Voltage	±18V	Output Short-Circuit Duration	Continuous
Power Dissipation (Note 1)	500mW	Operating Temperature Range LH24250	−55°C to 125°C
Differential Input Voltage	±15V	LH24250C	0°C to 70°C
Input Voltage (Note 2)	±15V	Storage Temperature Range	−65°C to 150°C
I_{SET} Current	150μA	Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics

LH24250, each amplifier (−55°C ≤ T_A ≤ 125°C unless otherwise specified)

Parameters	Conditions	$V_S = \pm 1.5V$				Units
		$I_{SET} = 1\mu A$		$I_{SET} = 10\mu A$		
		Min.	Max.	Min.	Max.	
V_{OS}	$T_A = 25°C$, $R_S \leq 100k\Omega$		3		5	mV
I_{OS}	$T_A = 25°C$		3		10	nA
I_{bias}	$T_A = 25°C$		7.5		50	nA
Large Signal Voltage Gain	$T_A = 25°C$, $R_L = 100k\Omega$	40				k
	$V_O = \pm 0.6V$, $R_L = 10k\Omega$			50		k
Supply Current	$T_A = 25°C$		7.5		80	μA
Power Consumption	$T_A = 25°C$		23		240	μW
V_{OS}	$R_S \leq 10k\Omega$		4		6	mV
I_{OS}	$T_A = 25°C$		5		10	nA
	$T_A = 25°C$		3		10	nA
I_{bias}			7.5		50	nA
Input Voltage Range		±0.7		±0.7		V
Large Signal Voltage Gain	$V_O = \pm 0.6V$, $R_L = 100k\Omega$	30				k
	$R_L = 10k\Omega$			30		k
Output Voltage Swing	$R_L = 100k\Omega$	±0.6				V
	$R_L = 10k\Omega$			±0.6	V	
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70		70		dB
Supply Voltage Rejection Ration	$R_S \leq 10k\Omega$	76		76		dB
Supply Current			8		90	μA
Power Consumption			24		270	μW

Parameters	Conditions	$V_S = \pm 15V$				Units
		$I_{SET} = 1\mu A$		$I_{SET} = 10\mu A$		
		Min.	Max.	Min.	Max.	
V_{OS}	$T_A = 25°C$, $R_S \leq 10k\Omega$		3		5	mV
I_{OS}	$T_A = 25°C$		3		10	na
I_{bias}	$T_A = 25°C$		7.5		50	nA
Large Signal Voltage Gain	$T_A = 25°C$, $R_L = 100k\Omega$	100				k
	$V_O = \pm 10V$, $R_L = 10k\Omega$			100		k
Supply Current	$T_A = 25°C$		10		90	μA
Power Consumption	$T_A = 25°C$		300		2.7	μW/mW
V_{OS}	$R_S \leq 10k\Omega$		4		6	mV
I_{OS}	$T_A = 25°C$		25		25	nA
	$T_A = 25°C$		3		10	nA
I_{bias}			7.5		50	nA
Input Voltage Range		±13.5		±13.5		V
Large Signal Voltage Gain	$V_O = \pm 15V$, $R_L = 100\Omega$	50				k
	$R_L = 10k\Omega$			50		k
Output Voltage Swing	$R_L = 100k\Omega$	±12				V
	$R_L = 10k\Omega$			±12		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70		70		dB
Supply Voltage Rejection ratio	$R_S \leq 10k\Omega$	76		76		dB
Supply Current		11		100		μA
Power Consumption			330		3	μW/mW

Note 1: The maximum junction temperature of the LH24250 is 150°C, while that of the LH24250C is 100°C. The thermal resistance of the dual-in-line package is 100°C/W junction to ambient. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16 inch thick epoxy glass board with ten, 0.03 inch wide, 2 ounce copper conductors.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

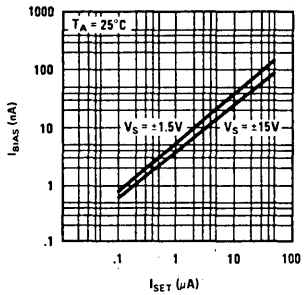
Electrical Characteristics LH24250C, each amplifier (0°C ≤ T_A ≤ 70°C unless otherwise specified)

Parameters	Conditions	$V_S = \pm 1.5V$				Units
		$I_{SET} = 1\mu A$		$I_{SET} = 10\mu A$		
		Min.	Max.	Min.	Max.	
V_{OS}	$T_A = 25°C$, $R_S \leq 100k\Omega$		5		6	mV
I_{OS}	$T_A = 25°C$		6		20	nA
I_{bias}	$T_A = 25°C$		10		75	nA
Large Signal Voltage Gain	$T_A = 25°C$, $R_L = 100k\Omega$	25				k
	$V_O = \pm 0.6V$, $R_L = 10k\Omega$			25		k
Supply Current	$T_A = 25°C$		8		90	μA
Power Consumption	$T_A = 25°C$		24		270	μW
V_{OS}	$R_S \leq 10k\Omega$		6.5		7.5	mV
I_{OS}			8		25	nA
I_{bias}			10		80	nA
Input Voltage Range		±0.6		±0.6		V
Large Signal Voltage Gain	$V_O = \pm 0.6V$, $R_L = 100k\Omega$	25				k
	$R_L = 10k\Omega$			25		k
Output Voltage Swing	$R_L = 100k\Omega$	±0.6				V
	$R_L = 10k\Omega$			±0.6	V	
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70		70	dB	
Supply Voltage Rejection Ration	$R_S \leq 10k\Omega$	74		74	dB	
Supply Current			8		90	μA
Power Consumption			24		270	μW

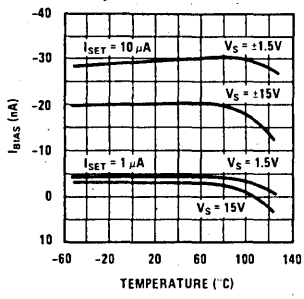
Parameters	Conditions	$V_S = \pm 15V$				Units
		$I_{SET} = 1\mu A$		$I_{SET} = 10\mu A$		
		Min.	Max.	Min.	Max.	
V_{OS}	$T_A = 25°C$, $R_S \leq 10k\Omega$		5		6	mV
I_{OS}	$T_A = 25°C$		6		20	na
I_{bias}	$T_A = 25°C$		10		75	nA
Large Signal Voltage Gain	$T_A = 25°C$, $R_L = 100k\Omega$	60				k
	$V_O = \pm 10V$, $R_L = 10k\Omega$			60		k
Supply Current	$T_A = 25°C$		11		100	μA
Power Consumption	$T_A = 25°C$		330		3	μW/mW
V_{OS}	$R_S \leq 10k\Omega$		6.5		7.5	mV
I_{OS}	$R_S \leq 10k\Omega$		8		25	nA
I_{bias}			10		80	nA
Input Voltage Range		±13.5		±13.5		V
Large Signal Voltage Gain	$V_O = \pm 15V$, $R_L = 100\Omega$	50				k
	$R_L = 10k\Omega$			50		k
Output Voltage Swing	$R_L = 100k\Omega$	±12				V
	$R_L = 10k\Omega$			±12		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70		70		dB
Supply Voltage Rejection ratio	$R_S \leq 10k\Omega$	74		74		dB
Supply Current		11		100		μA
Power Consumption			300		3	μW/mW

Typical Performance Charateristics

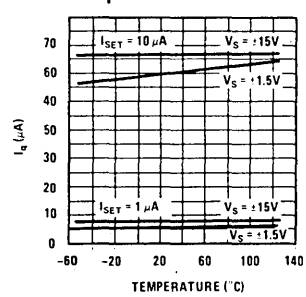
Input Bias Current vs I_{SET}



Input Bias Current vs Temperature



Quiescent Current (I_q) vs Temperature



Section 2

Buffers

2

Section 2. Buffer Amplifiers

Features	Voltage Gain (min.)	Output Current	Slew Rate	Input Impedance	Part Number		Page Number
					−55°C to 125°C	−25°C to 85°C	
Bipolar Input, medium speed	0.95	±100mA	200V/μs	180kΩ	LH0002H	LH0002CH LH0002CN	2-4 2-4
FET Input, high speed	0.97	±100mA	1000V/μs	10^{10}Ω	LH0033G	LH0033CG LH0033CJ	2-7 2-7
FET Input, very high speed	0.95	±250mA	6000V/μs	10^{10}Ω	LH0063K	LH0063CK	2-7
Bipolar Input, dual	0.999	±24mA	30V/μs	10^{10}Ω	LH2110	LH2210	2-18

National Semiconductor

LH0002/LH0002C Current Amplifier

General Description

The LH0002/LH0002C is a general purpose thick film hybrid current amplifier that is built on a single substrate. The circuit features:

- High Input Impedance 400 kΩ
- Low Output Impedance 6Ω
- High Power Efficiency
- Low Harmonic Distortion
- DC to 30 MHz Bandwidth
- Output Voltage Swing that Approaches Supply Voltage
- 400 mA Pulsed Output Current
- Slew rate is typically 200V/μs
- Operation from ±5V to ±20V

These features make it ideal to integrate with an operational amplifier inside a closed loop configuration to increase current output. The symmetrical output portion of the circuit also provides a low output impedance for both the positive and negative slopes of output pulses.

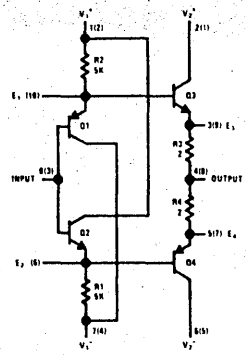
The LH0002 is available in an 8-lead low-profile TO-5 header; the LH0002C is also available in an 8-lead TO-5, and a 10-pin molded dual-in-line package.

The LH0002 is specified for operation over the −55°C to +125°C military temperature range. The LH0002C is specified for operation over the 0°C to +85°C temperature range.

Applications

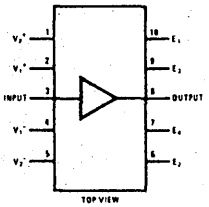
- Line driver
- 30 MHz buffer
- High speed D/A conversion
- Instrumentation buffer
- Precision current source

Schematic and Connection Diagrams



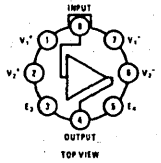
Pin numbers in parentheses denote pin connections for dual-in-line package.

Dual-In-Line Package



Order Number LH0002CN
See Package N10B

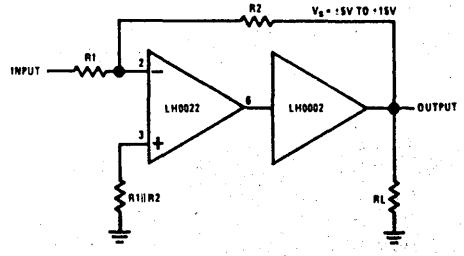
Metal Can Package



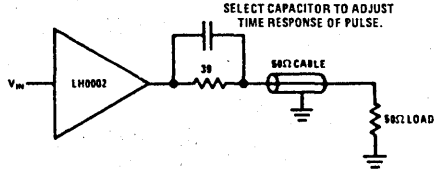
Order Number LH0002H or LH0002CH
See Package H08A

Typical Applications

High Current Operational Amplifier



Line Driver



*Previously called NH0002/NH0002C

Absolute Maximum Ratings

Supply Voltage	±22V
Power Dissipation Ambient	600mW
Input Voltage (Equal to Power Supply Voltage)	
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
LH0002	−55°C to +125°C
LH0002C	0°C to +85°C
Steady State Output Current	±100mA
Pulsed Output Current (50ms On/1 sec. Off)	±400mA

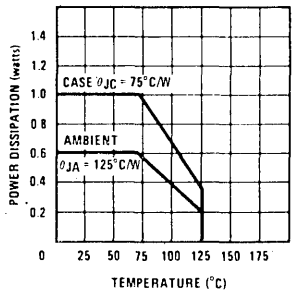
Electrical Characteristics (Note 1)

Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Gain	$R_S = 10k\Omega$, $R_L = 1.0k\Omega$, $V_{IN} = \pm 10V$	0.95	0.97		
AC Current Gain	$V_{IN} = 1.0V_{rms}$, f = 1.0kHz		40		A/ma
Input Impedance	$R_S = 200k\Omega$, $V_{IN} = \pm 1.0V$, $R_L = 1.0k\Omega$	180	400	—	kΩ
Output Impedance	$V_{IN} = \pm 1.0V$, $R_L = 50\Omega$, $R_S = 10k\Omega$	—	6.0	10	Ω
Output Voltage Swing	$R_L = 1.0k\Omega$, $V_{IN} = \pm 12V$	±10	±11	—	V
Output Voltage Swing	$V_S = \pm 15V$, $V_{IN} = \pm 12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $T_A = 25°C$	±10			V
DC Output Offset Voltage	$R_S = 300\Omega$, $R_L = 1.0k\Omega$	—	±10	±30	mV
DC Input Offset Current	$R_S = 10k\Omega$, $R_L = 1.0k\Omega$	—	±6.0	±10	μA
Harmonic Distortion	$V_{IN} = 5.0V_{rms}$, f = 1.0kHz	—	0.1	—	%
Rise Time	$R_L = 50\Omega$, $\Delta V_{IN} = 100mV$		7.0	12	ns
Positive Supply Current	$R_S = 10k\Omega$, $R_L = 1.0k\Omega$	—	+6.0	+10	mA
Negative Supply Current	$R_S = 10k\Omega$, $R_L = 1.0k\Omega$	—	−6.0	−10	mA

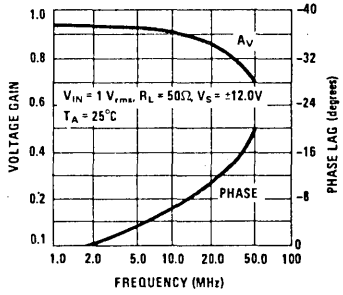
Note 1: Specification applies for $T_A = 25°C$ with +12V on Pins 1 and 2; −12V on Pins 6 and 7 for the metal can package and +12V on Pins 1 and 2; −12V on Pins 4 and 5 for the dual-in-line package unless otherwise specified. The parameter guarantees for LH0002C apply over the temperature range of 0°C to +85°C, while parameters for the LH0002 are guaranteed over the temperature range −55°C to 125°C unless otherwise specified.

Typical Performance

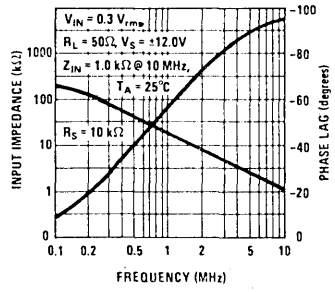
Maximum Power Dissipation



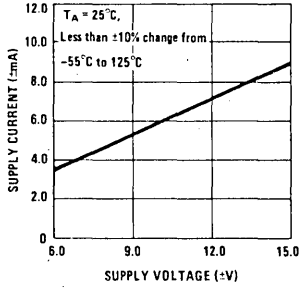
Frequency Response



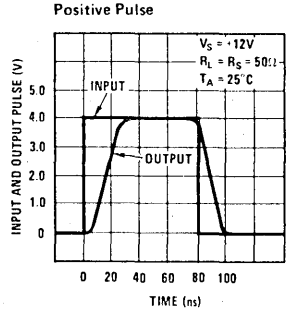
Input Impedance (Magnitude & Phase)



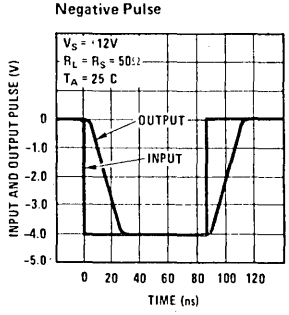
Supply Current



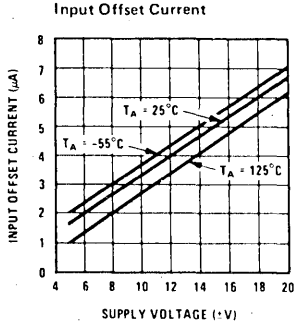
Positive Pulse



Negative Pulse



Input Offset Current



LH0033/LH0033C, LH0063/LH0063C Fast and Damn Fast Buffer Amplifiers

General Description

The LH0033/LH0033C and LH0063/LH0063C are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. The LH0033/LH0033C will provide ±10 mA into 1 kΩ loads (±100 mA peak) at slew rates of 1500V/μs. The LH0063/LH0063C will provide ±250 mA into 50Ω loads (±500 mA peak) at slew rates of up to 6000V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

Both are intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffer for driving reactive loads and high impedance input buffers for high speed A to D's and comparators. In addition, the LH0063/LH0063C can continuously drive 50Ω coaxial cables or be used as a diddle yoke driver for high resolution CRT displays. For additional applications information, see AN-48.

Advantages

- Only +10V supply needed for 5 V_{P-P} video out
- Speed does not degrade system performance
- Wide data rate range for phase encoded systems
- Output drive adequate for most loads
- Single pre-calibrated package

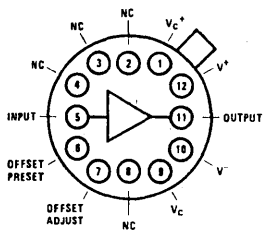
Features

■ Damn fast (LH0063)	6000V/μs
■ Wide range single or dual supply operation	
■ Wide power bandwidth	DC to 100 MHz
■ High output drive	±10V with 50Ω load
■ Low phase non-linearity	2 degrees
■ Fast rise times	2 ns
■ High current gain	120 dB
■ High input resistance	$10^{10}\Omega$

These devices are constructed using specially selected junction FET's and active laser trimming to achieve guaranteed performance specifications. The LH0033 and LH0063 are specified for operation from −55°C to +125°C; whereas, the LH0033C and LH0063C are specified from −25°C to +85°C. The LH0033/LH0033C is available in a 1.5W metal TO-8 package and a special 1/2 x 1 inch 8 pin ceramic dual-in-line package while the LH0063/LH0063C is available in a 5W 8-pin TO-3 package.

Connection Diagrams

Metal Can Package

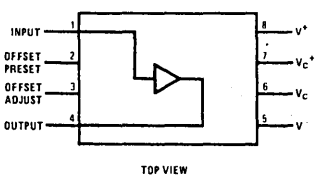


TOP VIEW

CASE IS ELECTRICALLY ISOLATED

Order Number LH0033G or LH0033CG
See Package H12B

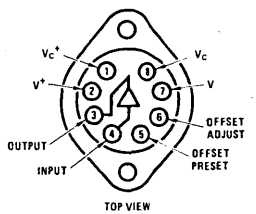
Dual-In-Line Package



TOP VIEW

Order Number LH0033J or LH0033CJ
See Package HY08A

Metal Can Package



TOP VIEW

CASE IS ELECTRICALLY ISOLATED

Order Number LH0063K or LH0063CK
See Package K08A

Absolute Maximum Ratings

Supply Voltage ($V^+ - V^-$)	40V
Maximum Power Dissipation (See Curves)	
LH0063/LH0063C	5W
LH0033/LH0033C	1.5W
Maximum Junction Temperature	175°C
Input Voltage	Equal to Supplies
Continuous Output Current	
LH0063/LH0063C	±250 mA
LH0033/LH0033C	±100 mA
Peak Output Current	
LH0063/LH0063C	±500 mA
LH0033/LH0033C	±250 mA
Operating Temperature Range	
LH0033 and LH0063	−55°C to +125°C
LH0033C and LH0063C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified

Parameter	Conditions	Limits						Units
		LH0033			LH0033C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Offset Voltage	$R_S = 100\Omega$, $T_J = 25°C$, $V_{IN} = 0V$ (see note 1)		5.0	10		12	20	mV
	$R_S = 100\Omega$			15			25	mV
Average Temperature Coefficient of Offset Voltage	$R_S = 100\Omega$, $V_{IN} = 0V$		50			50		µV/°C
Input Bias Current	$V_{IN} = 0V$ $T_J = 25°C$ (Note 1)			250			500	pA
	$T_A = 25°C$ (Note 2)			2.5			5.0	nA
	$T_J = T_A = T_{MAX}$			10			20	nA
Voltage Gain	$V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0k\Omega$	0.97	0.98	1.00	0.96	0.98	1.00	V/V
Input Impedance	$R_L = 1k\Omega$	10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	$V_{IN} = \pm 1.0V$, $R_L = 1.0k$		6.0	10		6.0	10	Ω
Output Voltage Swing	$V_I = \pm 14V$, $R_L = 1.0k$	±12			±12			V
	$V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$	±9.0			±9.0			V
Supply Current	$V_{IN} = 0V$		20	22		21	24	mA
Power Consumption	$V_{IN} = 0V$		600	660		630	720	mW

Note 1 is Note 2 of LH0032

Note 2 is Note 3 of LH0032

AC Electrical Characteristics $T_C = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1.0k\Omega$

Parameter	Conditions	Limits						Units
		LH0033			LH0033C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Slew Rate	$V_{IN} = \pm 10V$	1000	1500		1000	1400		V/µs
Bandwidth	$V_{IN} = 1.0V_{rms}$		100			100		MHz
Phase Non-Linearity	BW = 1.0 to 20 MHz		2.0			2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		2.9			3.2		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.2			1.5		ns
Harmonic Distortion	f > 1 kHz		<0.1			<0.1		%

Note 1: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40–60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs. temperature graph for expected values.

Note 2: Measured in still air 7 minutes after application of power.

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified

Parameter	Conditions	Limits						Units
		LH0063			LH0063C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Offset	$R_S \leq 100k\Omega$, $T_J = 25°C$ $R_L = 100\Omega$		10	25 100		10	50 100	mV mV
Average Temperature Coefficient of Output Offset Voltage	$R_S \leq 100k\Omega$		300			300		µV/°C
Input Bias Current	$T_J = 25°C$		0.1	10^{-5}		0.1	5^{-5}	nA
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100k\Omega$, $R_L = 1k\Omega$	0.94	0.96	1.0	0.94	0.96	1.0	V/V
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100k\Omega$, $R_L = 50\Omega$, $T_J = 25°C$	0.92	0.93	0.98	0.91	0.93	0.98	V/V
Input Capacitance	Case Shorted to Output		8.0			8.0		pF
Output Impedance	$V_{OUT} = \pm 10V$, $R_S \leq 100k\Omega$, $R_L = 50\Omega$		1.0	4.0		1.0	4.0	Ω
Output Current Swing	$V_{IN} = \pm 10V$, $R_S \leq 100k\Omega$	0.2	0.25		0.2	0.25		Amps
Output Voltage Swing	$R_L = 50\Omega$	±10	±13		±10	±13		V
Output Voltage Swing	$V_S = \pm 5.0V$, $R_L = 50\Omega$, $T_J = 25°C$	5.0	7.0		5.09	7.0		V
Supply Current	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		35	65		35	65	mA
Supply Current	$V_S = \pm 5.0V$		50			50		mA
Power Consumption	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		1.05	1.95		1.05	1.95	W
Power Consumption	$V_S = \pm 5.0V$		500			500		mW

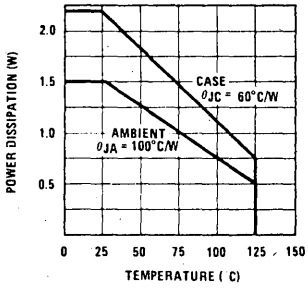
AC Electrical Characteristics LH0063/LH0063C ($T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50k\Omega$, $R_L = 50\Omega$)

Parameter	Conditions	Limits						Units
		LH0063			LH0063C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Slew Rate	$R_L = 1.0k\Omega$, $V_{IN} = \pm 10V$		6000			6000		V/µs
Slew Rate	$R_L = 50\Omega$, $V_{IN} = \pm 10V$, $T_J = 25°C$	2000	2400		2000	2400		V/µs
Bandwidth	$V_{IN} = 1.0V_{rms}$		200			200		MHz
Phase Non-Linearity	BW = 1.0 to 20MHz		2.0			2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		1.6			1.9		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.9			2.1		ns
Harmonic Distortion			<0.1			<0.1		%

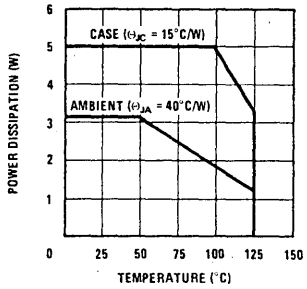
Note 1: Unless otherwise specified, these specifications apply for +15V applied to pins 1 and 12, −15V applied to pins 9 and 10, and pin 6 shorted to pin 7 for the LH0033/LH0033C. For the LH0063/LH0063C, specifications apply for +15V applied to pins 1 and 2, −15V applied to pins 7 and 8, and pin 5 shorted to pin 6. Unless otherwise noted, specifications apply over a temperature range of $-55°C \leq T_J \leq +125°C$ for the LH0033 and LH0063; and $-25°C \leq T_J \leq +85°C$ for the LH0033C and LH0063C. Typical values shown are for $T_J = 25°C$.

Typical Performance Characteristics

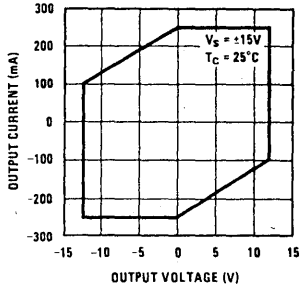
LH0033 Power Dissipation



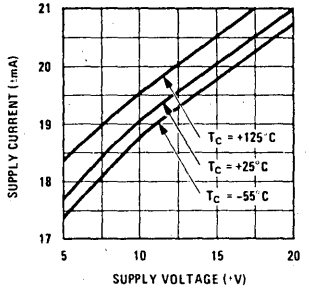
LH0063 Power Dissipation



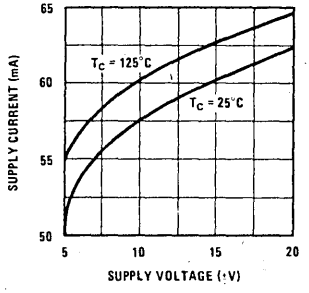
LH0063 DC Safe Operating Area



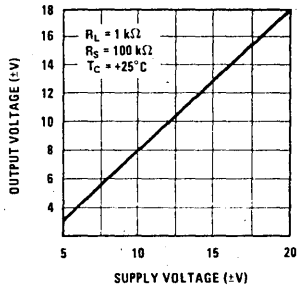
LH0033 Supply Current vs Supply Voltage



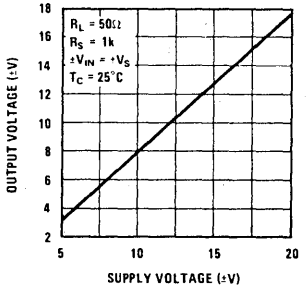
LH0063 Supply Current vs Supply Voltage



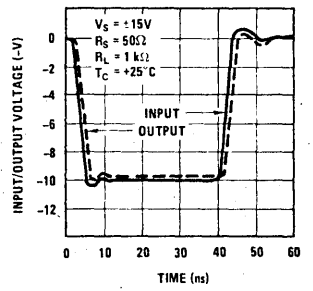
LH0033 Output Voltage vs Supply Voltage



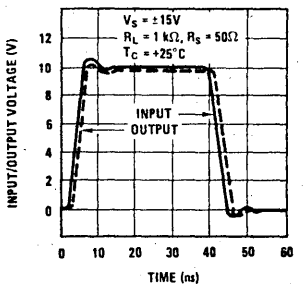
LH0063 Output Voltage vs Supply Voltage



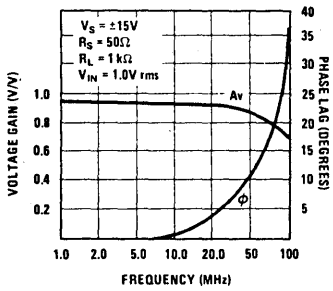
LH0033 Negative Pulse Response



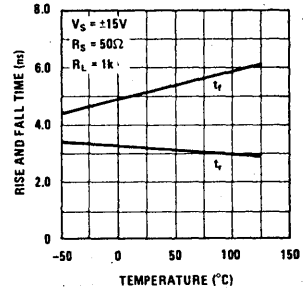
LH0033 Positive Pulse Response



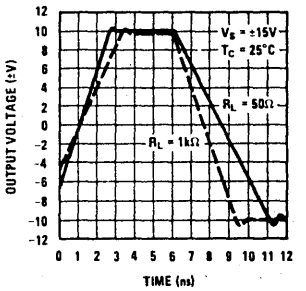
LH0033 Frequency Response



LH0033 Rise and Fall Time vs Temperature

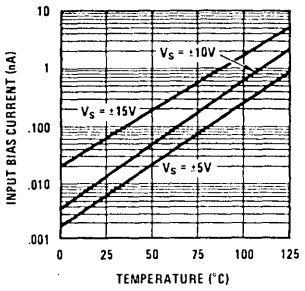


LH0063 Large Signal Pulse Response

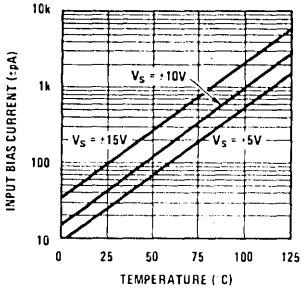


Typical Performance Characteristics (continued)

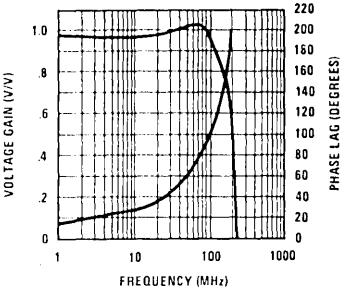
LH0033 Input Bias Current vs Temperature



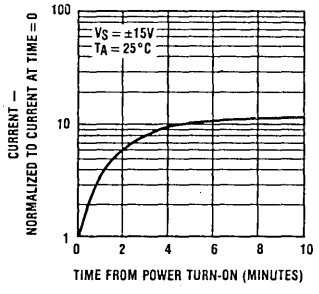
LH0063 Input Current



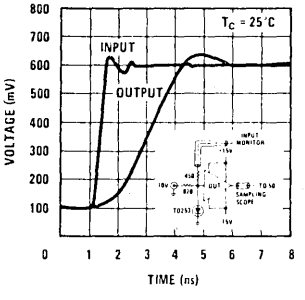
LH0063 Frequency Response



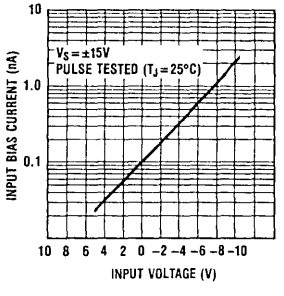
LH0033 Normalized Input Bias Current During Warm-up



LH0063 Small Signal Rise Time



LH0033 Input Bias Current vs Input Voltage



Application Hints

Recommended Layout Precautions: RF/video printed circuit board layout rules should be followed when using the LH0033 and LH0063 since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively the case should be connected to the output to minimize input capacitance.

Offset Voltage Adjustment: Both the LH0033's and LH0063's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω for the LH0033 or 1 kΩ for the LH0063 between the offset adjust pin and V^- as illustrated in Figures 1 and 2.

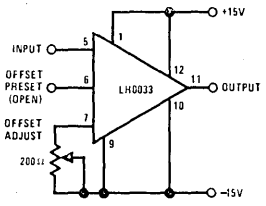


FIGURE 1. Offset Zero Adjust for LH0033 (Pin nos. shown for TO-8)

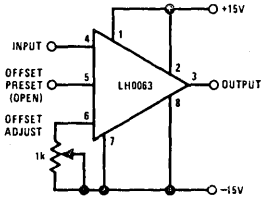


FIGURE 2. Offset Zero Adjust for LH0063

Applications Hints (Cont'd)

Operation from Single or Asymmetrical Power Supplies: Both device types may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V) \frac{(V^+ - V^-)}{2} = .005\,(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically .99

V^+ = Positive supply voltage

V^- = Negative supply voltage

For the above example, ΔV_O would be −35 mV. This may be adjusted to zero as described in Section 2. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the "typical applications" section.

Short Circuit Protection: In order to optimize transient response and output swing, output current limit has been omitted from the LH0033 and LH0063. Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in Figures 3 and 4. Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where: $I_{SC} \leq 100$ mA for LH0033

$I_{SC} \leq 250$ mA for LH0063

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C^+ and V_C^- pins with capacitors to ground will retain full output swing for transient pulses. Alternate active current limit techniques that retain full DC output swing are shown in Figures 5, 6 and 7. In Figures 5 and 6, the current sources are saturated during normal operation thus apply full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload. For Figure 5:

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{.6V}{60\text{ mA}} = 10\Omega$$

In Figure 6, quad transistor arrays are used to minimize can count and:

$$R_{LIM} = \frac{V_{BE}}{1/3\ (I_{SC})} = \frac{.6V}{1/3\ (200\text{ mA})} = 8.2\Omega$$

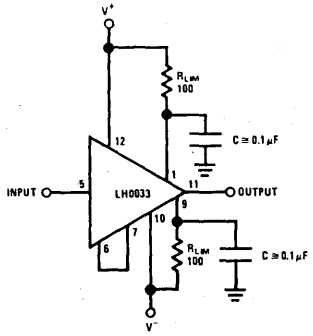


FIGURE 3. LH0033 Using Resistor Current Limiting

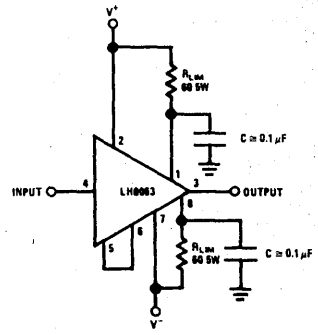


FIGURE 4. LH0063 Using Resistor Current Limiting

Applications Hints (Cont'd)

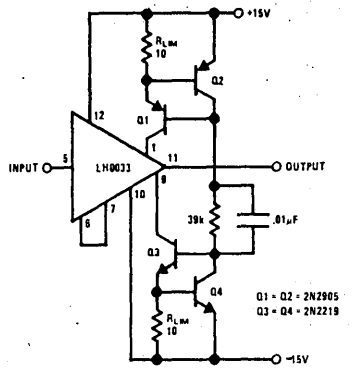


FIGURE 5. LH0033 Current Limiting Using Current Sources

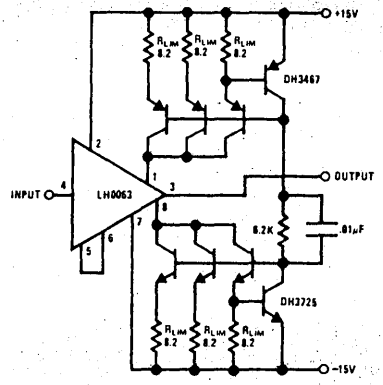


FIGURE 6. LH0063 Current Limiting Using Current Sources

Capacitive Loading: Both the LH0033 and LH0063 are designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from $(C \times d_V/d_t)$ should be limited below absolute maximum peak current ratings for the devices.

Thus for the LH0033:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250\ mA$$

and for the LH0063:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\ mA$$

Applications Hints (Cont'd)

In addition, power dissipation resulting from driving capacitative loads plus standby power should be kept below total package power rating:

$$P_{diss\ pkg} \geq P_{DC} + P_{AC}$$

$$P_{diss\ pkg} \geq (V^+ - V^-) \times I_S + P_{AC}$$

$$P_{AC} \cong (V_{P\text{-}P})^2 \times f \times C_L$$

where $V_{P\text{-}P}$ = Peak-to-peak output voltage swing
f = frequency
C_L = Load Capacitance

Operation Within an Op Amp Loop: Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LH0062, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH0033. The wide bandwidths and high slew rates of the LH0033 and LH0063 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

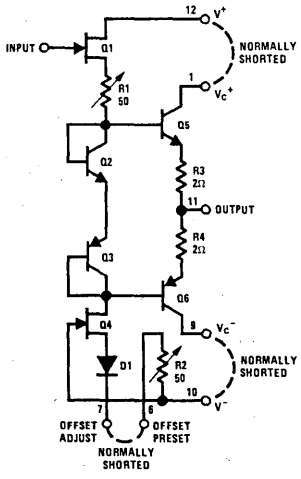
Hardware: In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to system chassis.

ACHTUNG!

Power supply bypassing is necessary to prevent oscillation with both the LH0033 and LH0063 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within < ¼ to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1μF in parallel for the LH0033; adding a 4.7μF solid tantalum capacitor will help in troublesome instances. For the LH0063, two 0.1μF ceramic and one 4.7μF solid tantalum capacitors in parallel will be necessary on each supply lead.

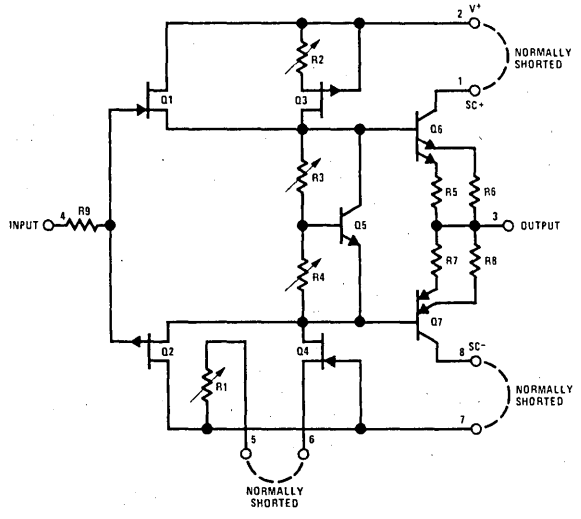
Schematic Diagrams

LH0033/LH0033C



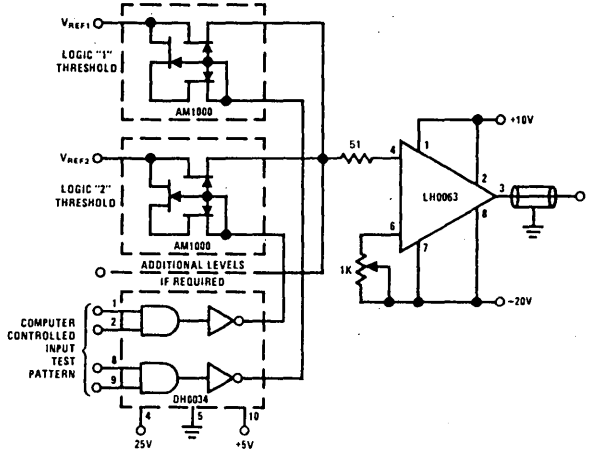
PIN NUMBERS SHOWN FOR TO-8 ("G") PACKAGE.

LH0063/LH0063C

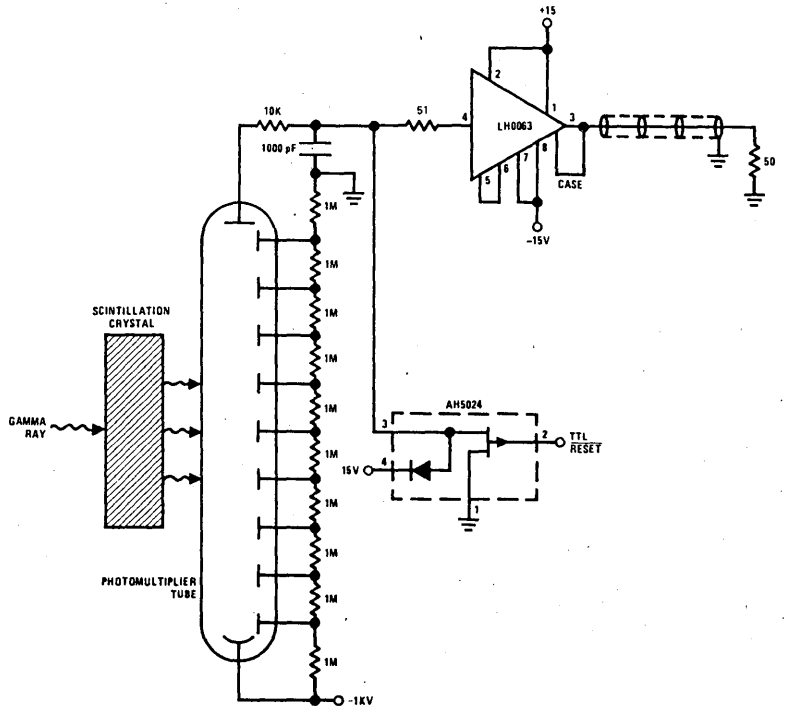


Typical Applications

High Speed Automatic Test Equipment
Forcing Function Generator

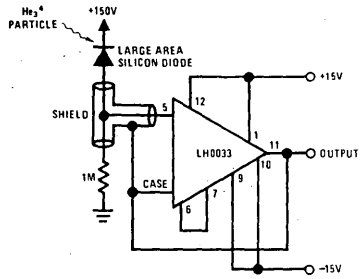


Gamma Ray Pulse Integrator

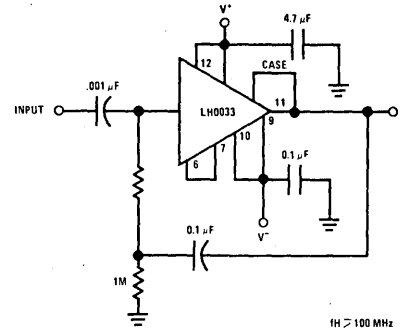


Typical Applications (Cont'd)

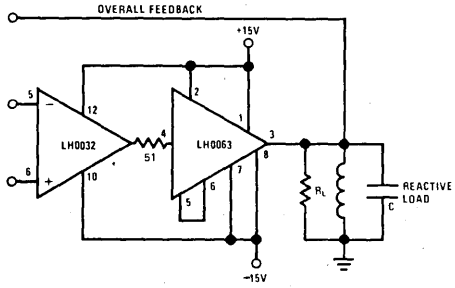
Nuclear Particle Detector



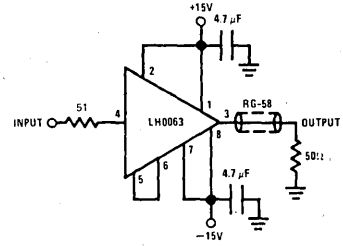
High Input Impedance AC Coupled Amplifier



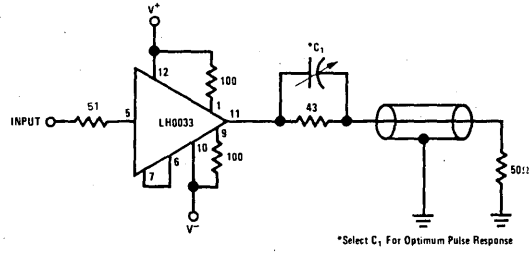
Isolation Buffer



Coaxial Cable Driver

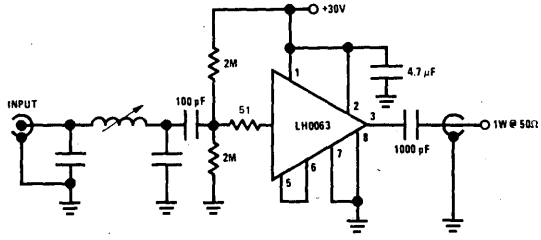


Coaxial Cable Driver



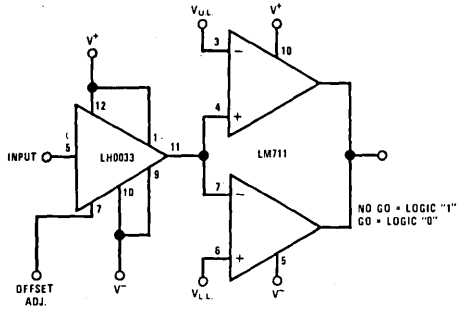
*Select C_1 For Optimum Pulse Response

1W CW Final Amplifier

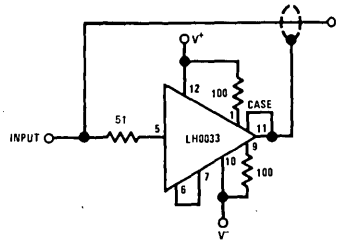


Typical Applications (Cont'd)

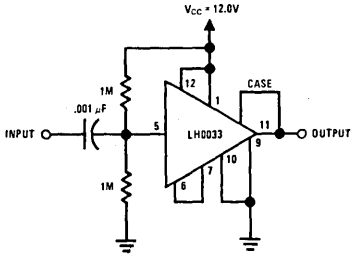
High Input Impedance Comparator With Offset Adjust



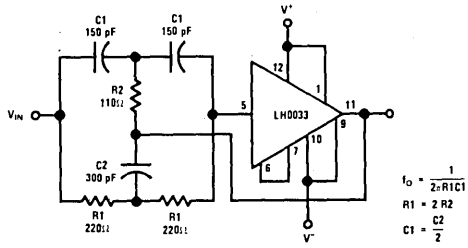
Instrumentation Shield/Line Driver



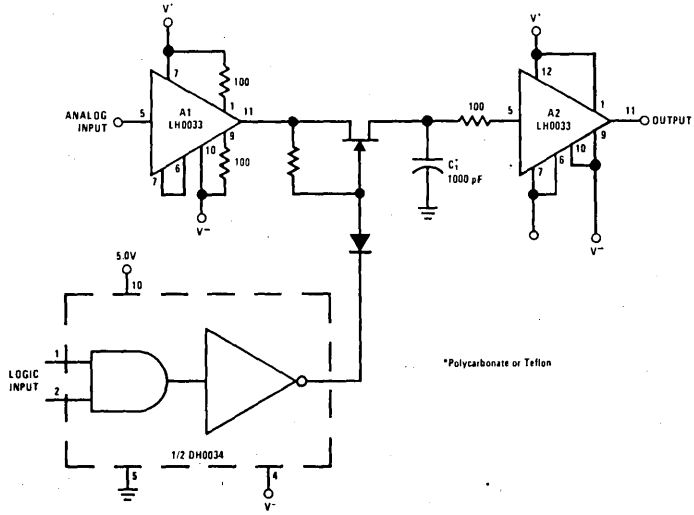
Single Supply AC Amplifier



4.5 MHz Notch Filter



High Speed Sample & Hold



National Semiconductor

LH2110/LH2210/LH2310 Dual Voltage Follower

General Description

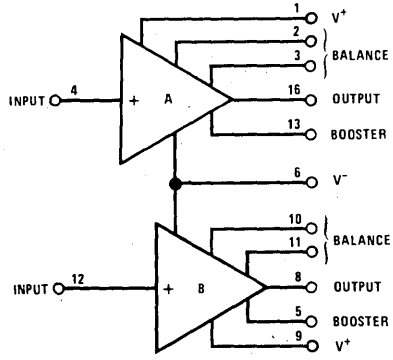
The LH2110 series of dual voltage followers are two LM110 type followers in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information, see the LM110 data sheet and National's Linear Application Notebook.

The LH2110 is specified for operation over the −55°C to +125°C military temperature range. The LH2210 is specified for operation over the −25°C to +85°C temperature range. The LH2310 is specified for operation over the 0°C to +70°C temperature range.

Features

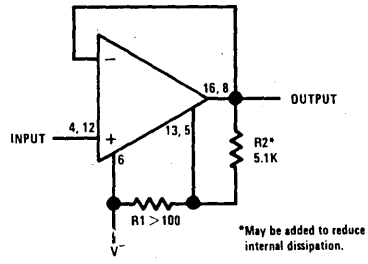
- Low input current — 1 nA
- High input resistance — 10^{10} ohms
- High slew rate — 30V/μs
- Wide bandwidth — 20 MHz
- Wide operating supply range — ±5V to ±18V
- Output short circuit proof

Connection Diagram

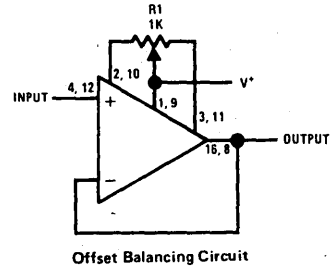


Order Number LH2110D, LH2210D or LH2310D, See Package D16C
Order Number LH2110F, LH2210F or LH2310F, See Package F16B
Order Number LH2110J, LH2210J or LH2310J, See Package J16A

Auxiliary Circuits



Increasing Negative Swing Under Load



Offset Balancing Circuit

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range LH2110	−55°C to 125°C
LH2210	−25°C to 85°C
LH2310	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics Each Side (Note 4)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2110	LH2210	LH2310	
Input Offset Voltage	$T_A = 25°C$	4.0	4.0	7.5	mV Max
Input Bias Current	$T_A = 25°C$	3.0	3.0	7.0	nA Max
Input Resistance	$T_A = 25°C$	10^{10}	10^{10}	10^{10}	Ω Min
Input Capacitance		1.5	1.5	1.5	pF Typ
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L = 8\ kΩ$	.999	.999	.999	V/V Min
Output Resistance	$T_A = 25°C$	2.5	2.5	2.5	Ω Max
Supply Current (Each Amplifier)	$T_A = 25°C$	5.5	5.5	5.5	mA Max
Input Offset Voltage		6.0	6.0	10	mV Max
Offset Voltage	$-55°C \leq T_A \leq 85°C$	6	6	10	μV/°C Typ
Temperature Drift	$T_A = 125°C$	12	12	–	μV/°C Typ
Input Bias Current		10	10	10	nA Max
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L = 10\ kΩ$	.999	.999	.999	V/V Min
Output Voltage Swing (Note 5)	$V_S = ±15V$, $R_L = 10\ kΩ$	±10	±10	±10	V Min
Supply Current (Each Amplifier)	$T_A = 125°C$	4.0	4.0	–	mA Max
Supply Voltage Rejection Ratio	$±5V \leq V_S \leq ±18V$	70	70	70	dB Min

Note 1: The maximum junction temperature of the LH2110 is 150°C, while that of the LH2210 is 100°C and that of the LH2310 is 85°C. For operating devices in the flat package at elevated temperatures, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.

Note 4: These specifications apply for $±5V \leq V_S \leq ±18V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM210, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$, and for the LH2310, all temperature specifications are limited to $0°C \leq T_A \leq 70°C$.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals.

Section 3

Instrumentation Amplifiers

Section 3. Instrumentation Amplifiers

All of the amplifiers in this section are true differential input instrumentation amplifiers with very high common mode rejection and adjustable gain.

Features	I_B Max.	V_{IOS} Max.	Characteristics $\frac{\Delta V_{IOS}}{\Delta T}$	Characteristics Gain Lin.	Gain Tempco	Gain Error	Part Number −25°C to 85°C	Part Number −55°C to 125°C	Page Number
90μW dissipation, wide supply range, one external gain set resistor	125nA 100nA	2mV 1mV	10μV/°C 10μV/°C	0.03% 0.03%	*	3% max. 1% max.	LH0036C	LH0036	3-4
Low cost, one external gain set resistor	500nA	2mV 1mV	10μV/°C 10μV/°C	0.03% 0.03%	* *	1% 0.3%	LH0037C	LH0037	3-12
Ultra low drift, all gain set resistors internal, very low noise, very linear, guard drive amplifier included	100nA	150μV 100μV	1μV/°C max. 0.25μV/°C max.	1ppm 1ppm	7ppm/°C 7ppm/°C	0.1% 0.1%	LH0038C	LH0038	3-15
Programmable gain fast settling	500pA 500pA	10mV 5mV	10μV/°C 10μV/°C	20ppm 20ppm	1ppm/°C 1ppm/°C	0.3% max. 0.3% max.	LH0084C	LH0084	3-26
Digitally programmable gain amplifier	500pA 500pA	10mV 5mV	10μV/°C 10μV/°C	20ppm 20ppm	1ppm/°C 1ppm/°C	0.3% max. 0.2% max.	LH0086C	LH0086	3-38

*Dependent upon external resistors.

National Semiconductor

LH0036/LH0036C Instrumentation Amplifier

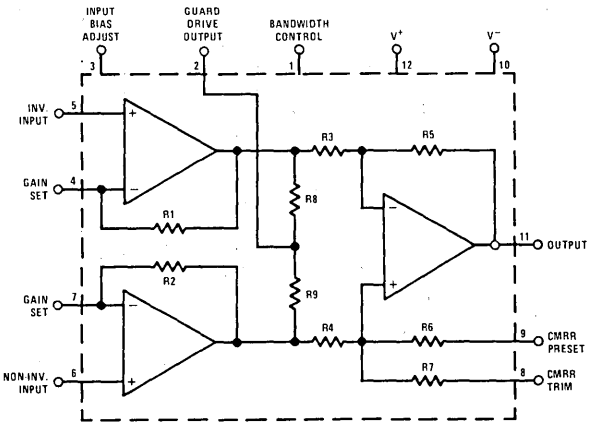
General Description

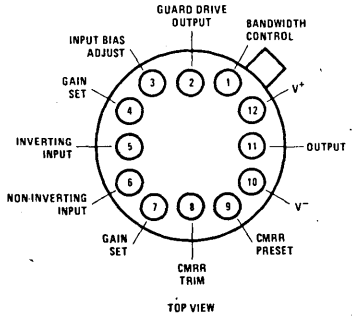
The LH0036/LH0036C is a true micro power instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable with one external resistor from 1 to 1000. Power supply operating range is between ±1V and ±18V. Input bias current and output bandwidth are both externally adjustable or can be set by internally set values. The LH0036 is specified for operation over the −55°C to +125°C temperature range and the LH0036C is specified for operation over the −25°C to +85°C temperature range.

Features

- High input impedance 300 MΩ
- High CMRR 100 dB
- Single resistor gain adjust 1 to 1000
- Low power 90μW
- Wide supply range ±1V to ±18V
- Adjustable input bias current
- Adjustable output bandwidth
- Guard drive output

Equivalent Circuit and Connection Diagrams





Order Number LH0036G or LH0036CG
See NS Package H12B

Absolute Maximum Ratings

Supply Voltage	±18V	Short Circuit Duration	Continuous
Differential Input Voltage	±30V	Operating Temperature Range	
Input Voltage Range	$\pm V_S$	LH0036	−55°C to +125°C
Shield Drive Voltage	$\pm V_S$	LH0036C	−25°C to +85°C
CMRR Preset Voltage	$\pm V_S$	Storage Temperature Range	−65°C to +150°C
CMRR Trim Voltage	$\pm V_S$	Lead Temperature, Soldering 10 seconds	300°C
Power Dissipation (Note 3)	1.5W		

Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0036			LH0036C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{IOS})	R_S = 1.0kΩ, T_A = 25°C		0.5	1.0		1.0	2.0	mV
	R_S = 1.0kΩ			2.0			3.0	mV
Output Offset Voltage (V_{OOS})	R_S = 1.0kΩ, T_A = 25°C		2.0	5.0		5.0	10	mV
	R_S = 1.0kΩ			6.0			12	mV
Input Offset Voltage Tempco ($\Delta V_{IOS}/\Delta T$)	$R_S \leq$ 1.0kΩ		10			10		µV/°C
Output Offset Voltage Tempco ($\Delta V_{OOS}/\Delta T$)			15			15		µV/°C
Overall Offset Referred to Input (V_{OS})	A_V = 1.0		2.5			6.0		mV
	A_V = 10		0.7			1.5		mV
	A_V = 100		0.52			1.05		mV
	A_V = 1000		0.502			1.005		mV
Input Bias Current (I_B)	T_A = 25°C		40	100		50	125	nA
				150			200	nA
Input Offset Current (I_{OS})	T_A = 25°C		10	40		20	50	nA
				80			100	nA
Small Signal Bandwidth	A_V = 1.0, R_L = 10kΩ		350			350		kHz
	A_V = 10, R_L = 10kΩ		35			35		kHz
	A_V = 100, R_L = 10kΩ		3.5			3.5		kHz
	A_V = 1000, R_L = 10kΩ		350			350		Hz
Full Power Bandwidth	V_{IN} = ±10V, R_L = 10k, A_V = 1		5.0			5.0		kHz
Input Voltage Range	Differential	±10	±12		±10	±12		V
	Common Mode	±10	±12		±10	±12		V
Gain Nonlinearity			0.03			0.03		%
Deviation From Gain Equation Formula	A_V = 1 to 1000		±0.3	±1.0		±1.0	±3.0	%
PSRR	±5.0V ≤ V_S ≤ ±15V, A_V = 1.0		1.0	2.5		1.0	5.0	mV/V
	±5.0V ≤ V_S ≤ ±15V, A_V = 100		0.05	0.25		0.10	0.50	mV/V
CMRR	A_V = 1.0 DC to		1.0	2.5		2.5	5.0	mV/V
	A_V = 10 100 Hz		0.1	0.25		0.25	0.50	mV/V
	A_V = 100 ΔR_S = 1.0k		50	100		50	100	µV/V
Output Voltage	V_S = ±15V, R_L = 10kΩ,	±10	±13.5		±10	±13.5		V
	V_S = ±1.5V, R_L = 100kΩ	±0.6	±0.8		±0.6	±0.8		V
Output Resistance			0.5			0.5		Ω
Supply Current			300	400		400	600	µA
Equivalent Input Noise Voltage	0.1 Hz < f < 10 kHz, R_S < 50 Ω		20			20		µV/p-p
Slew Rate	ΔV_{IN} = ±10V, R_L = 10kΩ, A_V = 1.0		0.3			0.3		V/µs
Settling Time	To ±10 mV, R_L = 10kΩ, ΔV_{OUT} = 1.0V							
	A_V = 1.0		3.8			3.8		µs
	A_V = 100		180			180		µs

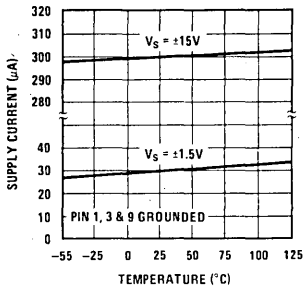
Note 1: Unless otherwise specified, all specifications apply for V_S = ±15V, Pins 1, 3, and 9 grounded, −25°C to +85°C for the LH0036C and −55°C to +125°C for the LH0036.

Note 2: All typical values are for T_A = 25°C.

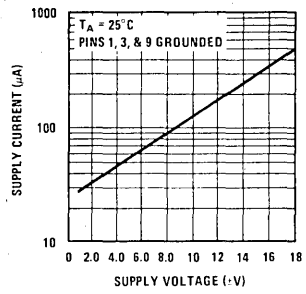
Note 3: The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W, above 25°C.

Typical Performance Characteristics

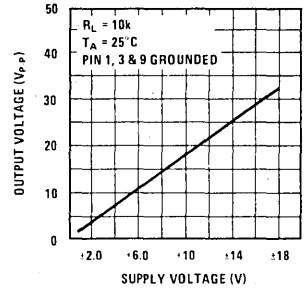
Supply Current vs Temperature



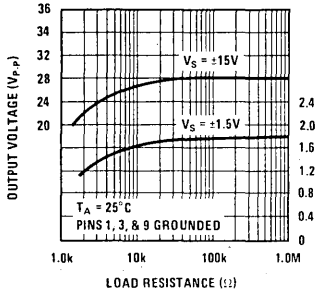
Supply Current vs Supply Voltage



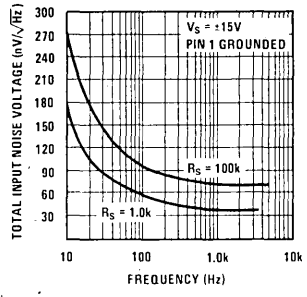
Output Voltage Swing vs Supply Voltage



Peak to Peak Output Voltage Swing vs R_L

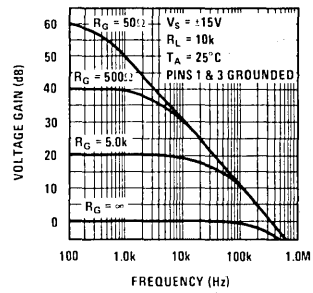


Total Input Noise Voltage* vs Frequency

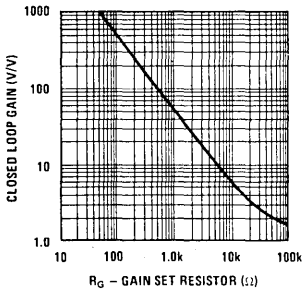


*Noise voltage includes contribution from source resistance

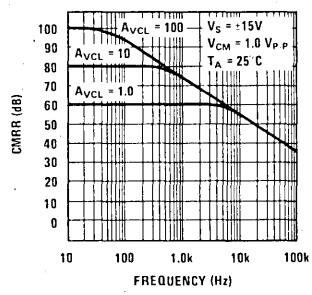
Closed Loop Voltage Gain vs Frequency



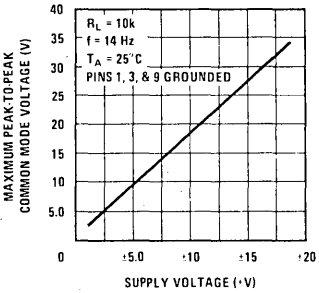
Closed Loop Voltage Gain



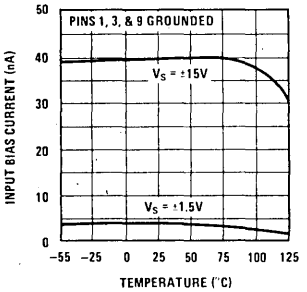
CMRR vs Frequency



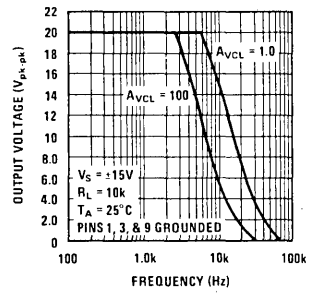
Common Mode Voltage vs Supply Voltage



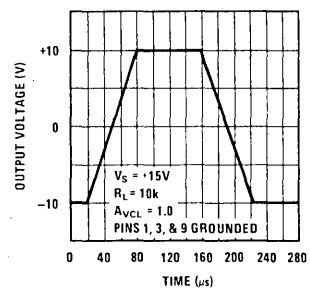
Input Bias Current



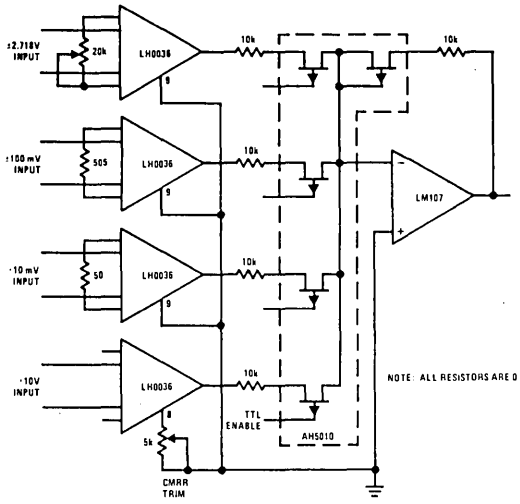
Output Voltage Swing vs Frequency



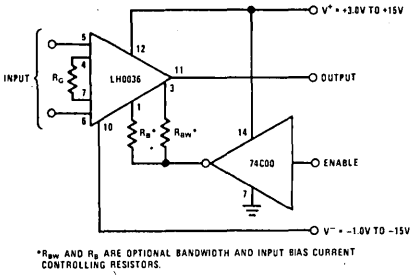
Large Signal Pulse Response



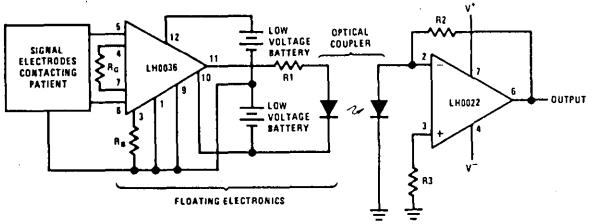
Typical Applications



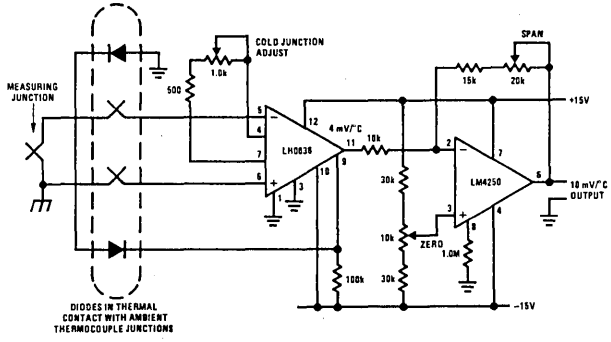
Pre MUX Signal Conditioning



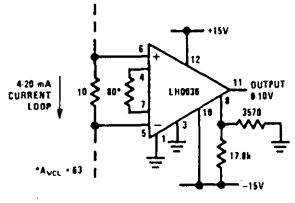
Instrumentation Amplifier with Logic Controlled Shut-Down



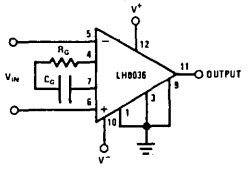
Isolation Amplifier for Medical Telemetry

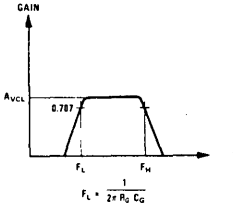


Thermocouple Amplifier with Cold Junction Compensation



Process Control Interface





F_H = A FUNCTION OF SELECTED A_{VCL}, R_B AND R_{BW}

High Pass Filter

Applications Information

THEORY OF OPERATION

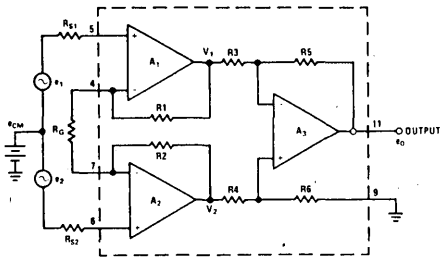


FIGURE 1. Simplified LH0036

The LH0036 is a 2 stage amplifier with a high input impedance gain stage comprised of A_1 and A_2 and a differential to single-ended unity gain stage, A_3. Operational amplifier, A_1, receives differential input signal, e_1, and amplifies it by a factor equal to $(R1 + R_G)/R_G$.

A_1 also receives input e_2 via A_2 and R2. e_2 is seen as an inverting signal with a gain of $R1/R_G$. A_1 also receives the common mode signal e_{CM} and processes it with a gain of +1.

Hence:

$$V_1 = \frac{R1 + R_G}{R_G} e_1 - \frac{R1}{R_G} e_2 + e_{CM} \quad (1)$$

By similar analysis V_2 is seen to be:

$$V_2 = \frac{R2 + R_G}{R_G} e_2 - \frac{R2}{R_G} e_1 + e_{CM} \quad (2)$$

For R1 = R2:

$$V_2 - V_1 = \left[\left(\frac{2R1}{R_G}\right) + 1\right](e_2 - e_1) \quad (3)$$

Also, for R3 = R5 = R4 = R6, the gain of $A_3 = 1$, and:

$$e_o = (1)(V_2 - V_1) = (e_2 - e_1)\left[1 + \left(\frac{2R1}{R_G}\right)\right] \quad (4)$$

As can be seen for identically matched resistors, e_{CM} is cancelled out, and the differential gain is dictated by equation (4).

For the LH0036, equation (4) reduces to:

$$A_{VCL} = \frac{e_o}{e_2 - e_1} = 1 + \frac{50k}{R_G} \quad (5a)$$

The closed loop gain may be set to any value from 1 ($R_G = \infty$) to 1000 ($R_G \cong 50\Omega$). Equation (5a) re-arranged in more convenient form may be used to select R_G for a desired gain:

$$R_G = \frac{50k}{A_{VCL} - 1} \quad (5b)$$

USE OF BANDWIDTH CONTROL (pin 1)

In the standard configuration, pin 1 of the LH0036 is simply grounded. The amplifier's slew rate in this configuration is typically 0.3V/μs and small signal bandwidth 350 kHz for $A_{VCL} = 1$. In some applications, particularly at low frequency, it may be desirable to limit bandwidth in order to minimize the overall noise bandwidth of the device. A resistor R_{BW} may be placed between pin 1 and ground to accomplish this purpose. Figure 2 shows typical small signal bandwidth versus R_{BW}.

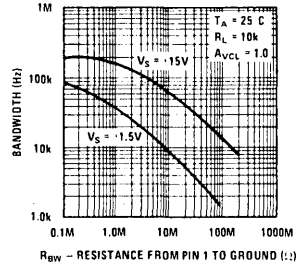


FIGURE 2. Bandwidth vs R_{BW}

It also should be noted that large signal bandwidth and slew rate may be adjusted down by use of R_{BW}. Figure 3 is plot of slew rate versus R_{BW}.

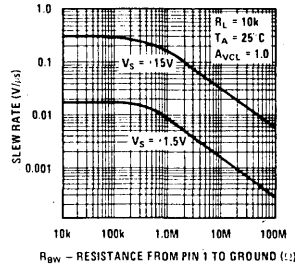


FIGURE 3. Output Slew Rate vs R_{BW}

CMRR CONSIDERATIONS

Use of Pin 9, CMRR Preset

Pin 9 should be grounded for nominal operation. An internal factory trimmed resistor, R6, will yield a CMRR in excess of 80 dB (for $A_{VCL} = 100$). Should a higher CMRR be desired, pin 9 should be left open and the procedure, in this section followed.

DC Off-set Voltage and Common Mode Rejection Adjustments

Off-set may be nulled using the circuit shown in Figure 4.

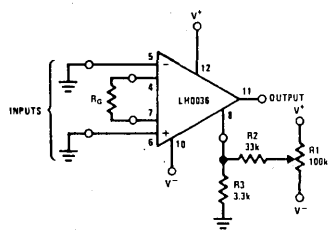


FIGURE 4. V_{OS} Adjustment Circuit

Pin 8 is also used to improve the common mode rejection ratio as shown in Figure 5. Null is

Applications Information (Cont'd)

achieved by alternately applying ±10V (for V^+ & V^- = 15V) to the inputs and adjusting R1 for minimum change at the output.

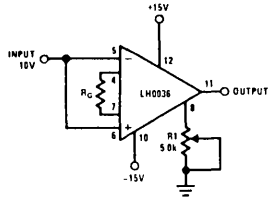


FIGURE 5. CMRR Adjustment Circuit

The circuits of Figure 4 and 5 may be combined as shown in Figure 6 to accomplish both V_{OS} and CMRR null. However, the V_{OS} and CMRR adjustment are interactive and several iterations are required. The procedure for null should start with the inputs grounded.

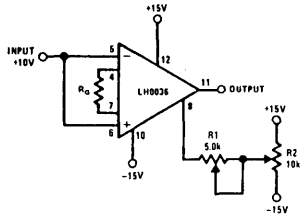
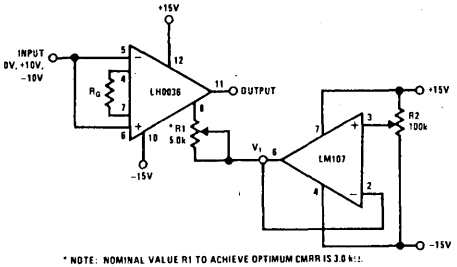


FIGURE 6. Combined CMRR, V_{OS} Adjustment Circuit

R2 is adjusted for V_{OS} null. An input of +10V is then applied and R1 is adjusted for CMRR null. The procedure is then repeated until the optimum is achieved.

A circuit which overcomes adjustment interaction is shown in Figure 7. In this case, R2 is adjusted first for output null of the LH0036. R1 is then adjusted for output null with +10V input. It is always a good idea to check CMRR null with a −10V input. The optimum null achievable will yield the highest CMRR over the amplifiers common mode range.



* NOTE: NOMINAL VALUE R1 TO ACHIEVE OPTIMUM CMRR IS 3.0 kΩ.

FIGURE 7. Improved V_{OS}, CMRR Nulling Circuit

AC CMRR Considerations

The ac CMRR may be improved using the circuit of Figure 8.

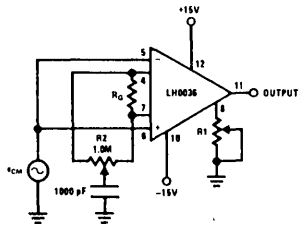


FIGURE 8. Improved AC CMRR Circuit

After adjusting R1 for best dc CMRR as before, R2 should be adjusted for minimum peak-to-peak voltage at the output while applying an ac common mode signal of the maximum amplitude and frequency of interest.

INPUT BIAS CURRENT CONTROL

Under nominal operating conditions (pin 3 grounded), the LH0036 requires input currents of 40 nA. The input current may be reduced by inserting a resistor (R_B) between 3 and ground or, alternatively, between 3 and V^-. For R_B returned to ground, the input bias current may be predicted by:

$$I_{BIAS} \cong \frac{V^+ - 0.5}{4 \times 10^8 + 800\ R_B} \qquad (6a)$$

or

$$R_B = \frac{V^+ - 0.5 - (4 \times 10^8)\ (I_{BIAS})}{800\ I_{BIAS}} \qquad (6b)$$

Where:

I_{BIAS} = Input Bias Current (nA)

R_B = External Resistor connected between pin 3 and ground (Ohms)

V^+ = Positive Supply Voltage (Volts)

Figure 9 is a plot of input bias current versus R_B.

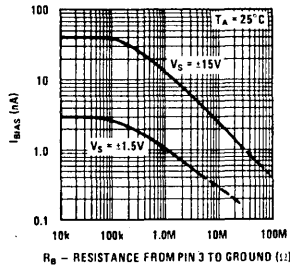


FIGURE 9. Input Bias Current as a Function of R_B

As indicated above, R_B may be returned to the negative supply voltage. Input bias current may then be predicted by:

$$I_{BIAS} \cong \frac{(V^+ - V^-) - 0.5}{4 \times 10^8 + 800\ R_B}$$

Applications Information (Cont'd)

or

$$R_B \cong \frac{(V^+ - V^-) - 0.5 - (4 \times 10^8)(I_{BIAS})}{800\ I_{BIAS}} \quad (8)$$

Where:

I_{BIAS} = Input Bias Current (nA)

R_B = External resistor connected between pin 3 and V^- (Ohms)

V^+ = Positive Supply Voltage (Volts)

V^- = Negative Supply Voltage (Volts)

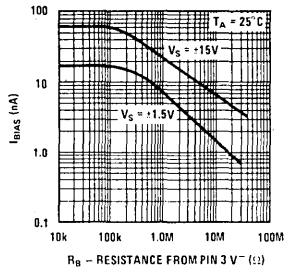


FIGURE 10. Input Bias Current as a Function of R_B

Figure 10 is a plot of input bias current versus R_B returned to V^- it should be noted that bandwidth is affected by changes in R_B. Figure 11 is a plot of bandwidth versus R_B.

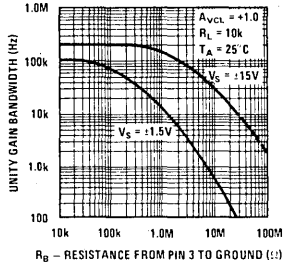


FIGURE 11. Unity Gain Bandwidth as a Function of R_B

BIAS CURRENT RETURN PATH CONSIDERATIONS

The LH0036 exhibits input bias currents typically in the 40 nA region in each input. This current must flow through R_{ISO} as shown in Figure 12.

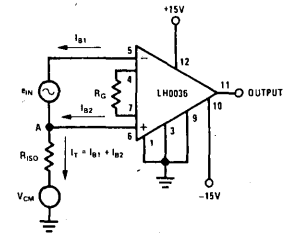


FIGURE 12. Bias Current Return Path

In a typical application, V_S = ±15V, $I_{B1} \cong I_{B2} \cong$ 40 nA, the total current, I_T, would flow through R_{ISO} causing a voltage rise at point A. For values of $R_{ISO} \geq 150$ MΩ, the voltage at point A exceeds the +12V common range of the device. Clearly, for $R_{ISO} = \infty$, the LH0036 would be driven to positive saturation.

The implication is that a finite impedance must be supplied between the input and power supply ground. The value of the resistor is dictated by the maximum input bias current, and the common mode voltage. Under worst case conditions:

$$R_{ISO} \leq \frac{V_{CMR} - V_{CM}}{I_T} \quad (9)$$

Where:

V_{CMR} = Common Mode Range (10V for the LH0036)

V_{CM} = Common Mode Voltage

$I_T = I_{B1} + I_{B2}$

In applications in which the signal source is floating, such as a thermocouple, one end of the source may be grounded directly or through a resistor.

GUARD OUTPUT

Pin 2 of the LH0036 is provided as a guard drive pin in those stringent applications which require very low leakage and minimum input capacitance. Pin 2 will always be biased at the input common mode voltage. The source impedance looking into pin 2 is approximately 15 kΩ. Proper use of the guard/shield pin is shown in Figure 13.

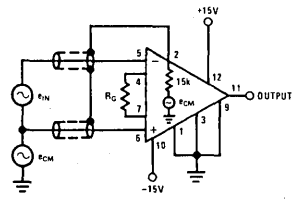


FIGURE 13. Use of Guard

For applications requiring a lower source impedance than 15 kΩ, a unity gain buffer, such as the LH0002 may be inserted between pin 2 and the input shields as shown in Figure 14.

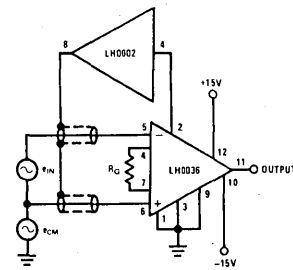


FIGURE 14. Guard Pin With Buffer

Definition of Terms

Bandwidth: The frequency at which the voltage gain is reduced to 0.707 of the low frequency (dc) value.

Closed Loop Gain, A_{VCL}: The ratio of the output voltage swing to the input voltage swing determined by $A_{VCL} = 1 + (50k/R_G)$. Where: R_G = Gain Set Resistor.

Common Mode Rejection Ratio: The ratio of input voltage range to the peak-to-peak change in offset voltage over this range.

Gain Equation Accuracy: The deviation of the actual closed loop gain from the predicted closed loop gain, $A_{VCL} = 1 + (50k/R_G)$ for the specified closed loop gain.

Input Bias Current: The current flowing at pin 5 and 6 under the specified operating conditions.

Input Offset Current: The difference between the input bias current at pins 5 and 6; i.e. $I_{OS} = |I_5 - I_6|$.

Input Stage Offset Voltage, V_{IOS}: The voltage which must be applied to the input pins to force the output to zero volts for $A_{VCL} = 100$.

Output Stage Offset Voltage, V_{OOS}: The voltage which must be applied to the input of the output stage to produce zero output voltage. It can be measured by measuring the overall offset at unity gain and subtracting V_{IOS}.

$$V_{OOS} = \left[V_{OS}\Big|_{A_{VCL}=1}\right] - \left[V_{OS}\Big|_{A_{VCL}=1000}\right]$$

Overall Offset Voltage:

$$V_{OS} = V_{IOS} + \frac{V_{OOS}}{A_{VCL}}$$

Power Supply Rejection Ratio: The ratio of the change in offset voltage, V_{OS}, to the change in supply voltage producing it.

Resistor, R_B: An optional resistor placed between pin 3 of the LH0036 and ground (or V^-) to reduce the input bias current.

Resistor, R_{BW}: An optional resistor placed between pin 1 of the LH0036 and ground (or V^-) to reduce the bandwidth of the output stage.

Resistor, R_G: A gain setting resistor connected between pins 4 and 7 of the LH0036 in order to program the gain from 1 to 1000.

Settling Time: The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

National Semiconductor

LH0037/LH0037C Low Cost Instrumentation Amplifier

General Description

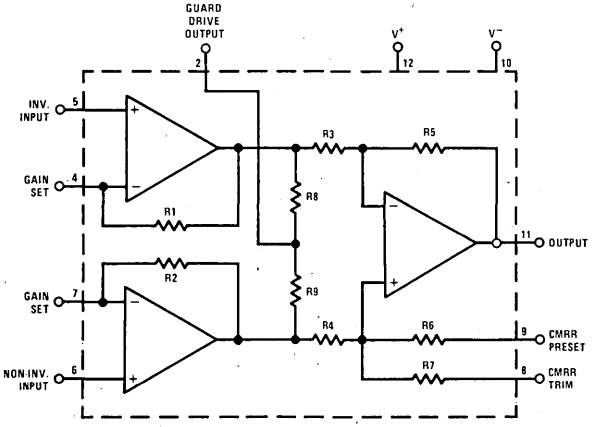
The LH0037/LH0037C is a true instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common-mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable with one external resistor from 1 to 1000. Power supply operating range is between ±5V and ±22V.

The LH0037 is specified for operation over the −55°C to +125°C temperature range and the LH0037C is specified for operation over the −25°C to +85°C temperature range.

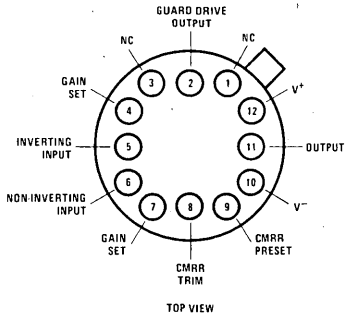
Features

- High input impedance 300 MΩ
- High CMRR 100 dB
- Single resistor gain adjust 1 to 1000
- Low power 250 mW
- Wide supply range ±5V to ±22V
- Guard drive output

Equivalent Circuit and Connection Diagrams

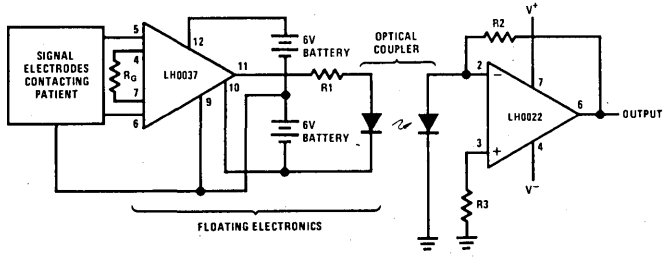


Metal Can Package



Order Number LH0037G or LH0037CG
See Package H12B

Typical Applications



Isolation Amplifier for Medical Telemetry

Absolute Maximum Ratings

Supply Voltage	±22V	Short Circuit Duration	Continuous
Differential Input Voltage	±30V	Operating Temperature Range	
Input Voltage Range	$\pm V_S$	LH0037	−55°C to +125°C
Shield Drive Voltage	$\pm V_S$	LH0037C	−25°C to +85°C
CMRR Preset Voltage	$\pm V_S$	Storage Temperature Range	−65°C to +150°C
CMRR Trim Voltage	$\pm V_S$	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (Note 3)	1.5W		

Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0037			LH0037C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (V_{IOS})	R_S = 1.0 kΩ, T_A = 25°C		0.5	1.0		1.0	2.0	mV
	R_S = 1.0 kΩ			2.0			3.0	mV
Output Offset Voltage (V_{OOS})	R_S = 1.0 kΩ, T_A = 25°C		2.0	5.0		5.0	10	mV
	R_S = 1.0 kΩ			6.0			12	mV
Input Offset Voltage Tempco ($\Delta V_{IOS}/\Delta T$)	$R_S \leq$ 1.0 kΩ		10			10		µV/°C
Output Offset Voltage Tempco ($\Delta V_{OOS}/\Delta T$)			15			15		µV/°C
Overall Offset Referred to Input (V_{OS})	A_V = 1.0		2.5			6.0		mV
	A_V = 10		0.7			1.5		mV
	A_V = 100		0.52			1.05		mV
	A_V = 1000		0.502			1.005		mV
Input Bias Current (I_B)	T_A = 25°C		200	500		200	500	nA
				1.5			0.8	µA
Input Offset Current (I_{OS})	T_A = 25°C			100			250	nA
				200			250	
Small Signal Bandwidth	A_V = 1.0, R_L = 2 kΩ		350			350		kHz
	A_V = 10, R_L = 2 kΩ		35			35		kHz
	A_V = 100, R_L = 2 kΩ		3.5			3.5		kHz
	A_V = 1000, R_L = 2 kΩ		350			350		Hz
Full Power Bandwidth	V_{IN} = ±10V, R_L = 2 kΩ A_V = 1		5.0			5.0		kHz
Input Voltage Range	Differential	±12			±12			V
	Common Mode	±12			±12			V
Gain Nonlinearity			0.03			0.03		%
Deviation From Gain Equation Formula	A_V = 1 to 1000		±0.3	±1		±1.0	±3	%
PSRR	±5.0V ≤ V_S ≤ ±15V, A_V = 1.0		1.0	2.5		1.0	5	mV/V
	±5.0V ≤ V_S ≤ ±15V, A_V = 100		0.05	0.25		0.10	0.25	mV/V
CMRR	A_V = 1.0 DC to		1.0	2.5		2.5	5.0	mV/V
	A_V = 10 100 Hz		0.1	0.25		0.25	1.0	mV/V
	A_V = 100 ΔR_S = 1.0k		25	100		25	100	µV/V
Output Voltage	R_L = 2 kΩ	10	13		10	13		V
Output Resistance			0.5			0.5		Ω
Supply Current			4.5	8.4		4.5	8.4	mA
Slew Rate	ΔV_{IN} = ±10V, R_L = 2 kΩ, A_V = 1.0		0.5			0.5		V/µs
Settling Time	To ±10 mV, R_L = 2 kΩ ΔV_{OUT} = 1.0V							
	A_V = 1.0		3.8			3.8		µs
	A_V = 100		180			180		µs

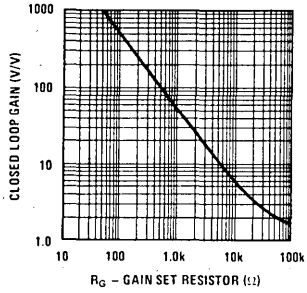
Note 1: Unless otherwise specified, all specifications apply for V_S = ±15V, pin 9 grounded, −25°C to +85°C for the LH0037C and −55°C to +125°C for the LH0037.

Note 2: All typical values are for T_A = 25°C.

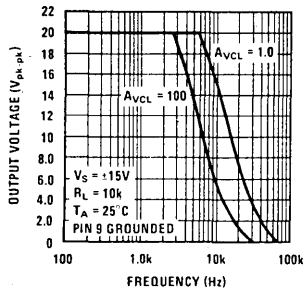
Note 3: The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W, above 25°C.

Typical Performance Characteristics

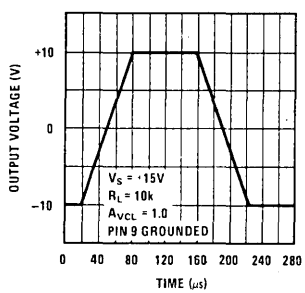
Closed Loop Voltage Gain



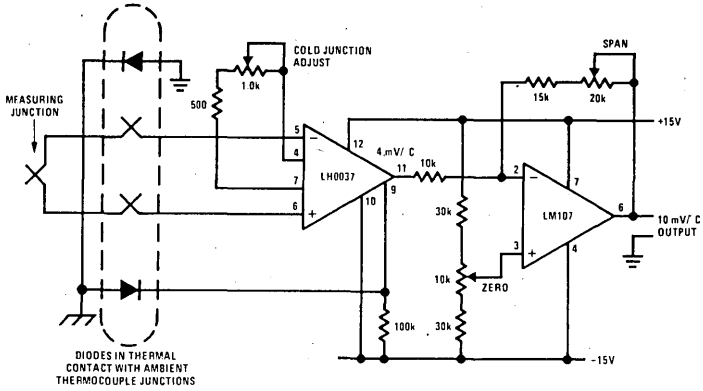
Output Voltage Swing vs Frequency



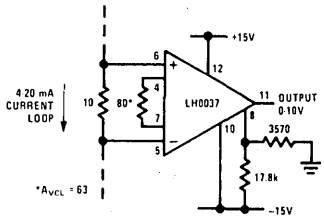
Large Signal Pulse Response



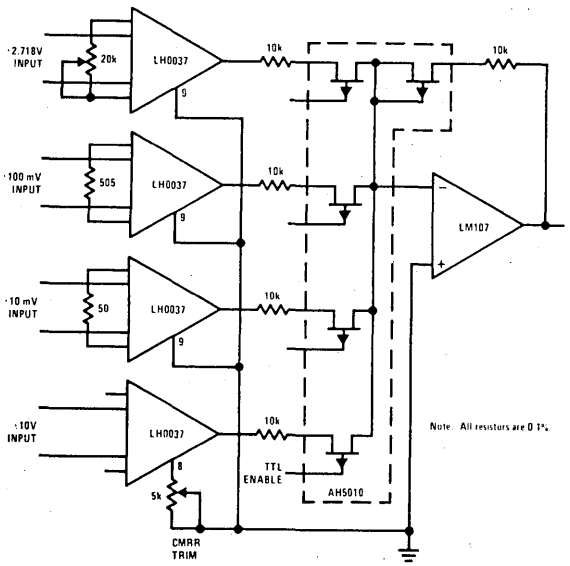
Typical Applications (Cont'd)



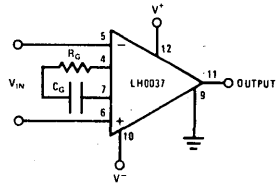
Thermocouple Amplifier with Cold Junction Compensation

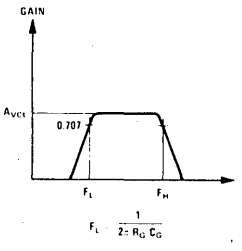


Process Control Interface



Pre MUX Signal Conditioning





High Pass Filter

National Semiconductor

LH0038/LH0038C True Instrumentation Amplifier

General Description

The LH0038/LH0038C is a precision true instrumentation amplifier (TIA) capable of amplifying very low level signals, such as thermocouple and low impedance strain guage outputs. Precision thin film gain setting resistors are included in the package to allow the user to set the closed-loop gain from 100 to 2000. Since the resistors are of a homogeneous single chip construction, they track almost perfectly so that temperature variations of closed loop gain are virtually eliminated.

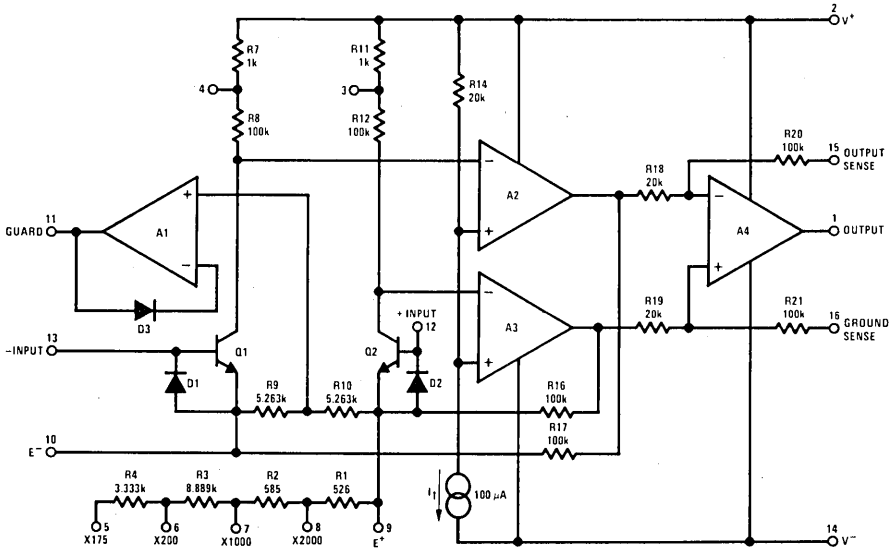
LH0038 exhibits excellent CMRR, PSRR, gain linearity, as well as extremely low input offset voltage, offset voltage drift and input noise voltage.

The devices are provided in a hermetically sealed 16-lead DIP. The LH0038 is guaranteed from −55°C to +125°C; whereas the LH0038C is guaranteed from −25°C to +85°C.

Features

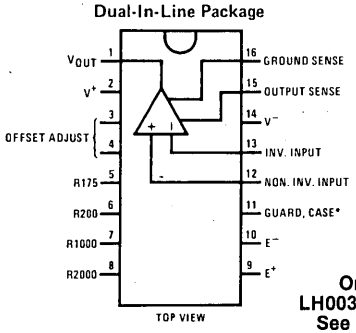
- Ultralow offset voltage — 25 μV typ., 100 μV max
- Ultralow offset drift — 0.25 μV/C max
- Ultralow input noise — 0.2 μVp-p
- Pin strap gain options — 100, 200, 400, 500, 1k, 2k
- Excellent PSRR and CMRR — 120 dB

Simplified Schematic Diagram



Connection Diagram

Dual-In-Line Package



Order Number
LH0038D or LH0038CD
See Package D16D

*Guard output is connected to the case.

Absolute Maximum Ratings

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±1V
Input Voltage	$\pm V_S$
Power Dissipation (See Curve)	500 mW
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0038	−55°C to +125°C
LH0038C	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 20 seconds)	300°C

DC Electrical Characteristics (Note 2)

PARAMETER		CONDITIONS		LH0038			LH0038C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IOS}	Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$	$T_A = 25°C$		25	100		30	150	µV
						125			220	
$\Delta V_{IOS}/\Delta T$	Input Offset Voltage Tempco				0.1	0.25		0.2	1.0	µV/°C
V_{OOS}	Output Offset Voltage		$T_A = 25°C$		3	10		5	25	mV
						15			30	
$\Delta V_{OOS}/\Delta T$	Output Offset Voltage Tempco				25			25		µV/°C
I_B	Input Bias Current	$V_{CM} = 0V$	$T_A = 25°C$		50	100		50	100	nA
						200			200	
I_{OS}	Input Offset Current		$T_A = 25°C$		2	5		7	10	
						8			15	
$\Delta I_B/\Delta T$	Input Bias Current Tempco				500			500		pA/°C
A_{VCL}	Closed Loop Gain	Gain Pins Jumpered								V/V
		None			100			100		
		6–10			200			200		
		6–9, 10–5			400			400		
		6–10, 5–9			500			500		
		7–10			1000			1000		
		8–10			2000			2000		
	Closed Loop Gain Error	A_{VCL} = 100, 200			0.1	0.3		0.1	0.4	%
		A_{VCL} = 400, 500			0.2	0.3		0.2	0.6	
		A_{VCL} = 1000			0.3	0.5		0.5	1.0	
		A_{VCL} = 2000			1.0	2.0		1.5	3.0	
	Gain Temperature Coefficient	A_{VCL} = 1k			7			7		ppm/°C
	Gain Nonlinearity	$100 \leq A_{VCL} \leq 2k$			1			1		ppm
V_{INCM}	Common-Mode Input Voltage Range			±10	±12		±10	±12		V
V_O	Output Voltage	$R_L \geq 10\ k\Omega$		±10	±12		±10	±12		
V_S	Supply Voltage Range			±5		±18	±5		±18	
	Guard Voltage Error	$-10V < V_{CM} < +10V$			±10	±100		±10	±100	mV

DC Electrical Characteristics (Note 2) (Continued)

PARAMETER		CONDITIONS		LH0038			LH0038C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±10V	A_{VCL} = 100	94	110		86	110		dB
			A_{VCL} = 1000	114	120		106	110		
PSRR	Power Supply Rejection Ratio	±5V ≤ ΔV_S ≤ ±15V	A_{VCL} = 100	94	110		94	110		
			A_{VCL} = 1000	110	120		100	110		
I_{OSC}	Output Short Circuit Current	T_A = 25°C		±2	±5	±10	±2	±5	±10	mA
I_S	Supply Current	T_A = 25°C			1.6	2.0		1.6	3.0	
R_{IN} DIFF	Input Resistance	A_{VCL} = 1000, T_A = 25°C			5			5		MΩ
R_{IN} CM	Common-Mode Input Resistance				1			1		GΩ
R_{OUT}	Output Resistance				1			1		mΩ

AC Electrical Characteristics V_S = ±15V, T_A = 25°C

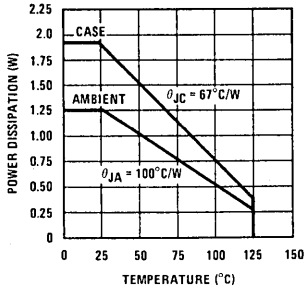
PARAMETER		COMMENT	CONDITIONS		TYP	UNITS
e_n	Equivalent Input Noise Voltage	*Figure 1*	R_S = 0, f = 0.1 to 10 Hz		0.2	μVp-p
$\overline{e_n}$	Equivalent Input Spot Noise Voltage	*Figure 1*	R_S = 100Ω	f = 10 Hz	6.5	nV/√Hz
				f = 100 Hz	6.0	
				f = 1 kHz	6.0	
				f = 10 kHz	6.0	
BW	Large Signal Bandwidth		V_{OUT} = ±10V		1.6	kHz
S_r	Slew Rate		V_{OUT} = ±10V		0.3	V/μs
t_s	Settling Time to 0.01%	*Figure 13*		20V Step	120	μs
				−10V Step	80	
				+10V Step	60	
t_r	Rise Time		ΔV_{OUT} = 100 mV	A_{VCL} = 100	6	μs
				A_{VCL} = 1000	13	
$\overline{i_n}$	Equivalent Input Spot Noise Current		R_S = 100 MΩ	f = 10 Hz	0.1	pA/√Hz

Note 1: The inputs are protected by diodes for overvoltage protection. Excessive currents will flow for differential voltages in excess of ±1V. Input current should be limited to less than 10 mA.

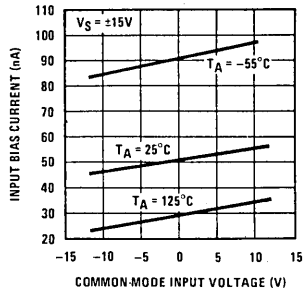
Note 2: Unless otherwise noted these specifications apply for V_S = ±15.0V, pin 15 connected to pin 1, pin 16 connected to ground, over the temperature range −55°C to +125°C for the LH0038 and −25°C to +85°C for LH0038C.

Typical Performance Characteristics

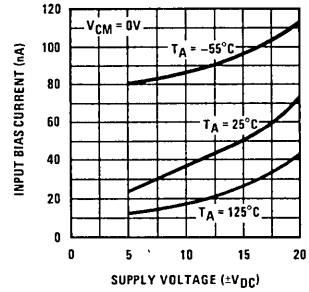
Power Dissipation



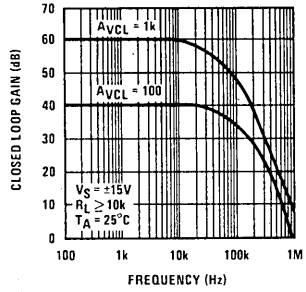
Input Bias Current



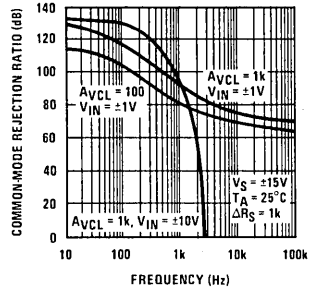
Input Bias Current



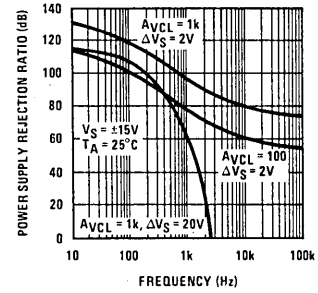
Closed Loop Frequency Response



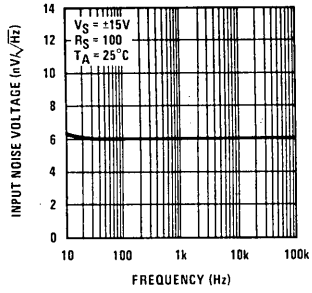
Common-Mode Rejection



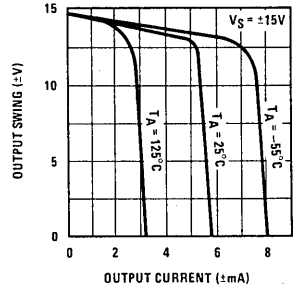
Power Supply Rejection



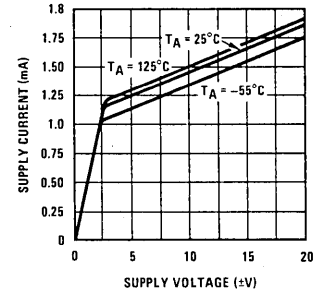
Input Noise Voltage (Includes Source Impedance)



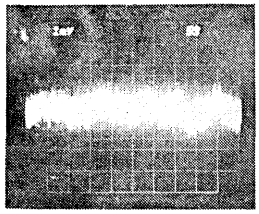
Output Swing



Supply Current

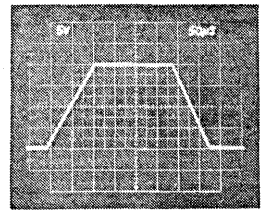


Wide Band Noise



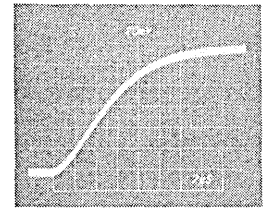
V_S = ±15V, R_S = 1kΩ, A_V = 10k, DUT = 1k
Vertical sensitivity: 0.1 μV/CM
Horizontal sensitivity: 5 sec/CM
Bandwidth: 0.1 Hz to 10 Hz

Pulse Response



V_S = ±15V
$R_L \geq 10k\Omega$
A_{VCL} = 1k

Rise Time



V_S = ±15V
$R_L \geq 10k\Omega$
A_{VCL} = 1k

Noise Test Circuit

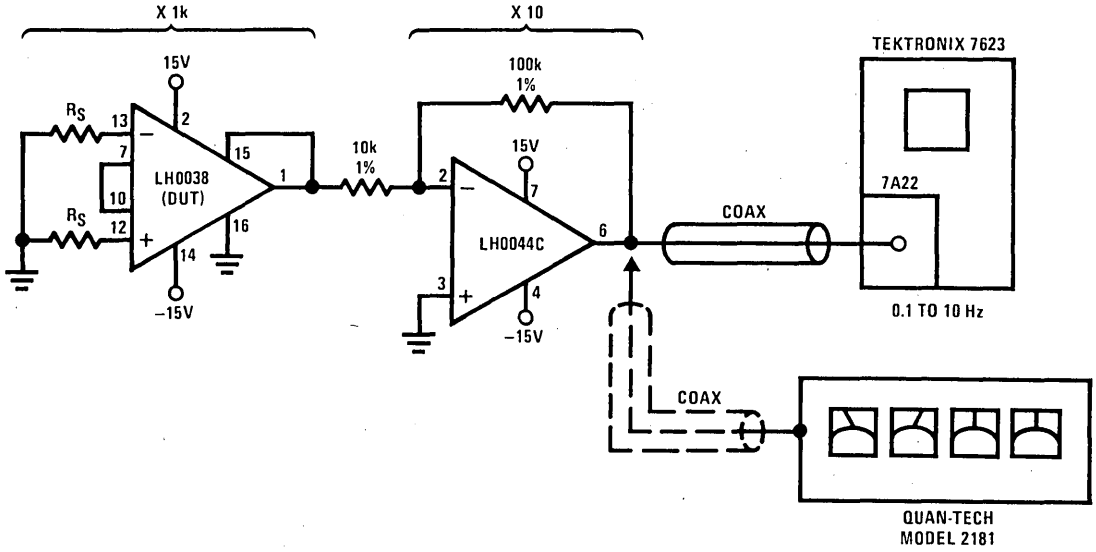


FIGURE 1.

Typical Application

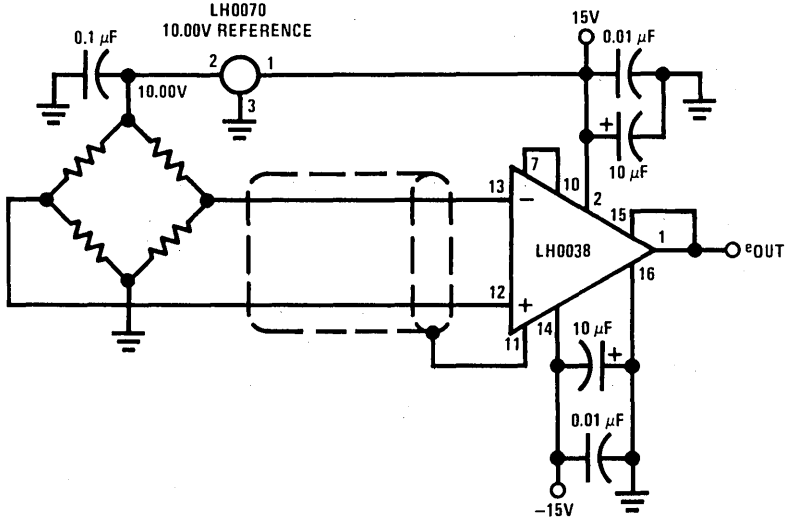


FIGURE 2. X1000 Bridge Amplifier

Applications Information

THEORY OF OPERATION

The LH0038 is a 3-stage, true instrumentation amplifier composed of a well matched transistor differential pair, Q1 and Q2, a common-mode loop amplifier, A2 and A3, and a differential to single ended amplifier, A4. A simplified schematic is shown in *Figure 3.*

Current source, I_A, establishes a voltage across R14 of approximately 2V, which results in a 2V drop across R8 and R12. This constant voltage forces the first stage current to be 20 μA per side. The action of A2 and A3 is such that 20 μA is maintained constant despite the presence of common-mode signals. The differential outputs of A2 and A3 are applied to differential amplifier, A4, which converts the signal to a single-ended output and provides a gain of 5. The total gain of the amplifier is, therefore, the fixed gain of 5 multiplied by the gain of the composite input stage.

Applications Information (Continued)

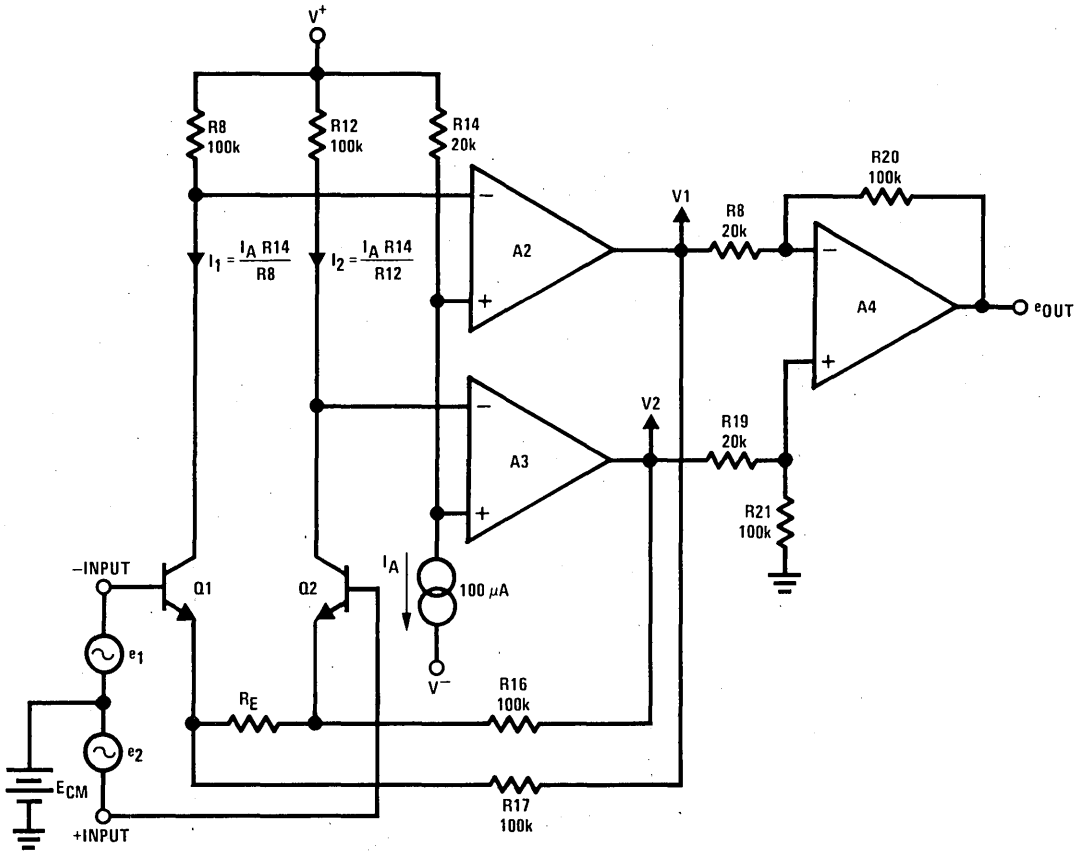


FIGURE 3. LH0038 Simplified Schematic

The closed loop gain of the composite amplifier may be better understood by referring to *Figure 3.* The Q1–A2 loop may be viewed as differential amplifier with the inverting input at the base and non-inverting input at the emitter. Combining small signal AC and large signal DC analysis =

$$v1 = e1\left(\frac{R17 + R_E}{R_E}\right) - e2\left(\frac{R17}{R_E}\right) + E_{CM} - V_{BE1} - I_1 R17 \quad (1)$$

By similar analysis:

$$v2 = e2\left(\frac{R16 + R_E}{R_E}\right) - e1\left(\frac{R16}{R_E}\right) + E_{CM} - V_{BE2} - I_2 R16 \quad (2)$$

For $I_1 \equiv I_2$, R17 ≡ R16, $V_{BE1} \equiv V_{BE2}$, subtracting equation (1) from (2) results in:

$$v2 - v1 = (e2 - e1)\left(\frac{R16 + R_E}{R_E}\right) + (e2 - e1)\left(\frac{R16}{R_E}\right) \quad (3)$$

$$\frac{v2 - v1}{e2 - e1} = \frac{2\,R16}{R_E} + 1 \quad (4)$$

Applications Information (Continued)

The differential input voltage (v2 − v1) is amplified by the closed loop gain of A4:

$$e_{OUT} = (A_{VCL4})\,(e2 - e1) \qquad (5)$$

where:

$$A_{VCL4} = \frac{R20}{R8}$$

$$= 5.00$$

$$\boxed{A_{VCL} = 5\left(\frac{2R16}{R_E} + 1\right)} \qquad (6)$$

As an example, with all gain pins open, R_E = 10.526 kΩ, and:

$$A_{VCL} = 5\left(\frac{(2)\,(100k)}{10.526k} + 1\right) \qquad (7)$$

$$= 100.0$$

All other closed loop gain configurations place a precision resistor in parallel with R_E(R9 + R10). For example, for a gain of 200, pin 6 is connected to pin 10 and the gain is predicted by:

$$A_{VCL} = 5.00\left[\frac{(2)\,(100k)}{(10.526k)\,||\,(10.000k)} + 1\right] \qquad (8)$$

$$= (5.00)\,(40) = 200$$

CLOSED LOOP GAIN CONSIDERATIONS USING INTERNAL RESISTORS

Table I summarizes the primary gain configurations available with the LH0038. Obviously, other gains are possible. Using the internally supplied resistors has the advantage that R16, R17, and R_E all track thermally, minimizing the device's gain error as a function of temperature.

Gain adjustment by paralleling or series padding internally supplied resistors is generally discouraged since external resistors will generally not thermally track. It is recommended that the gain adjustment be done in a subsequent stage as shown in *Figure 4.*

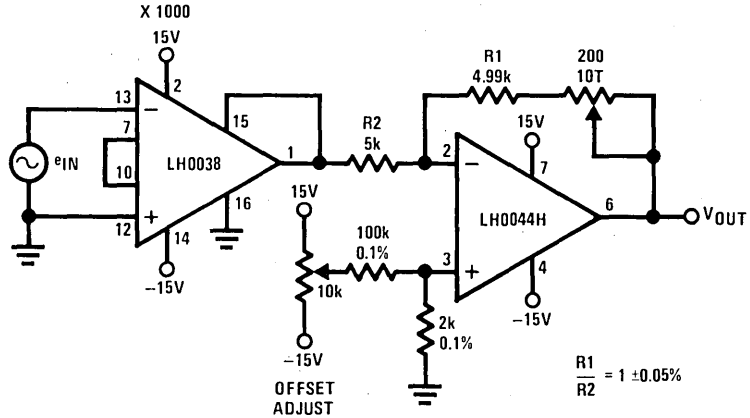


FIGURE 4. Recommended Gain Adjust Circuit

TABLE I. LH0038 INTERNAL GAIN CONFIGURATIONS

OVERALL GAIN	FIRST STAGE GAIN	PIN CONNECTIONS	EFFECTIVE R_E
100	20	All Gain Pins Open	10.5260 kΩ
200	40	Pin 6 to Pin 10	5.1281 kΩ
400	80	Pin 6 to Pin 9, Pin 10 to Pin 5	2.5316 kΩ
500	100	Pin 6 to Pin 10, Pin 9 to Pin 5	2.0202 kΩ
1000	200	Pin 7 to Pin 10	1.0050 kΩ
2000	400	Pin 8 to Pin 10	0.5013 kΩ

Applications Information (Continued)

GUARD DRIVE

The LH0038 is provided with a guard drive output, which will always be at the input common-mode voltage. The guard drive amplifier is short-circuit proof and is capable of driving several thousand pF without danger of latch-up or oscillation.

The guard drive tied to a shielded input cable will greatly reduce noise pick-up, and also improve AC CMRR by maintaining the shield at the common-mode voltage. *Figure 5* illustrates the proper use of the guard drive.

The guard drive output is also connected to the case to provide electrostatic shielding to the system.

REMOTE OUTPUT SENSE

The feedback network of the LH0038 may be closed directly at the load in order to eliminate errors due to lead resistance. Also, a unity gain buffer; e.g. LH0002, may be included within the feedback loop to increase output current capability as shown in *Figure 7*.

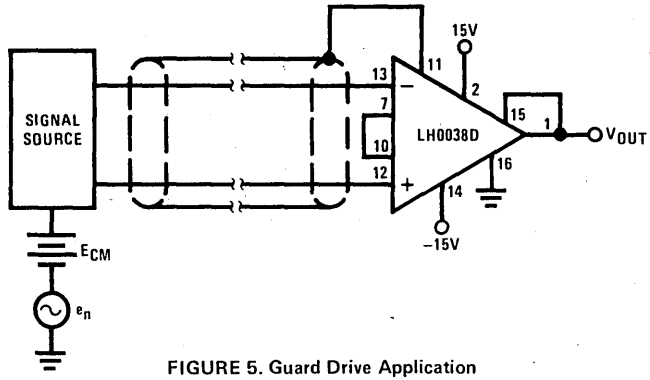


FIGURE 5. Guard Drive Application

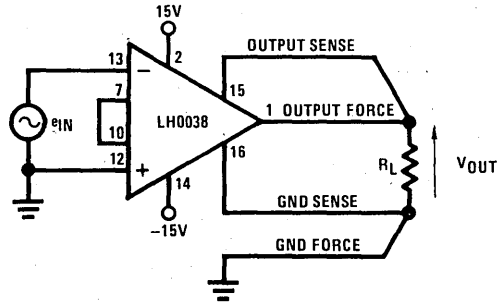


FIGURE 6. Remote Sense Connection

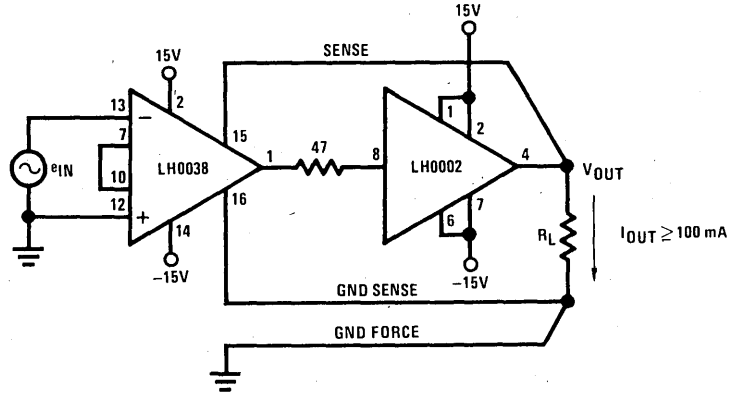


FIGURE 7. Output Buffer Connection

Applications Information (Continued)

OFFSET NULL

Offset of the LH0038 is trimmed by the factory to a very low value. The offset may be further trimmed using a 10 kΩ, 10 turn, 100 ppm/°C potentiometer as shown in *Figure 8.* However, a drift increase of 0.3 μV/°C will be caused for each 100 μV of offset adjusted. The recommended offset null is shown in *Figure 4* and is accomplished in the following stage.

BIAS CURRENT CONSIDERATIONS

The LH0038 exhibits bias current of approximately 50 nA per side, and requires a path to ground or supply. The practical limitation to the maximum resistance betwi · the inputs and ground is dictated by negative comm n-mode range as shown in *Figure 9.* For example, for $V_{CM} = -10V$, $R_{CM} \leq 20\ M\Omega$.

The LH0038 input stage bias was optimized for minimum voltage noise so the input bias currents are higher than might otherwise be expected. Note, however, that the input currents are very well matched, resulting in an offset current value much lower than one might infer from the bias current. In order to take advantage of this low offset current, the source impedances at both inputs should be matched to minimize DC drift. Further, bias current is relatively constant with temperature (as opposed to an FET stage), so one can consider bias current compensation schemes such as shown in *Figure 10.* The danger with such techniques is that the offset current and noise contributed by the bias current compensator will dominate the system noise.

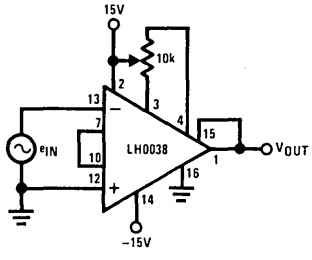


FIGURE 8. Offset Adjust Circuit
(See also *Figure 4*)

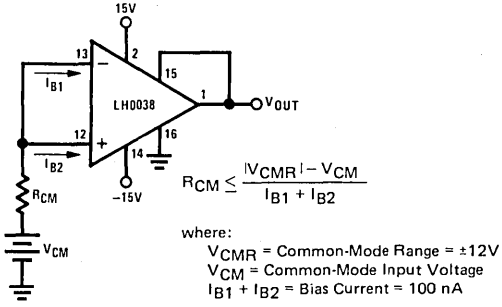


FIGURE 9. Bias Current Return

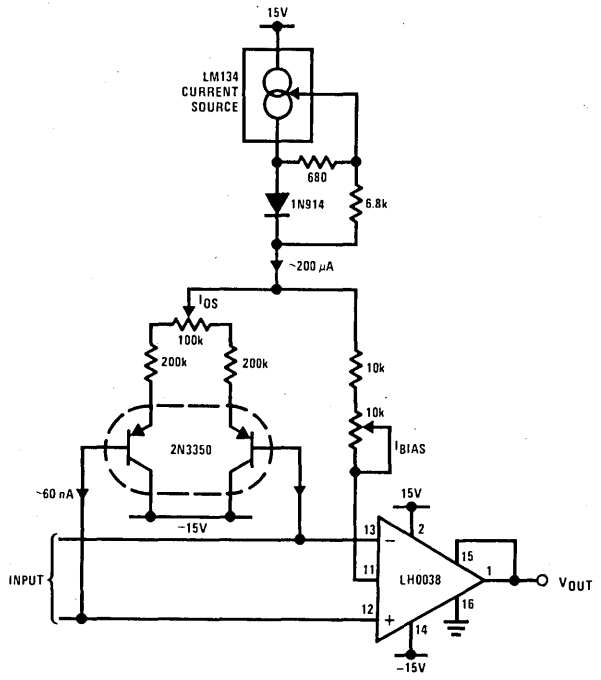


FIGURE 10. Bias Current Compensation

Applications Information (Continued)

SETTLING TIME

The LH0038 has been purposely over-compensated, and is therefore remarkably free from any undesirable transient response. Small signal settling time is governed by gain-bandwidth product; large signal settling time is dominated by slew rate.

Figure 11 shows an input voltage step of +10V to −10V applied, through a 1000 to 1 voltage divider, to the device configured for an inverting gain of 1000. The output of the device will therefore be equal to the negative of the input after the device is completely settled. By resistively subtracting the input before the divider from the device output, a pseudo summing node is generated. The voltage at this pseudo summing junction goes "off screen" on the photos, since in the first small time increment the input goes instantaneously to −10 mV and the output is still at +10V. About 130 μs after the input has gone negative, the output slews back in range and begins an exponential approach to the final value. *Figure 12* is the same set-up for a −10V to +10V input pulse. Note that there is no overshoot in either case. The test circuit is shown in *Figure 13*.

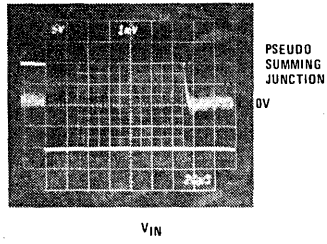
HIGH FREQUENCY CMRR

The LH0038 resistor ratios are carefully trimmed for optimum CMRR at DC through 60 Hz. Inevitably, this rejection will degrade at higher frequencies due to 2 separate effects: stray capacitance mismatch and slew rate limiting in the input stage. In most discrete instrumentation amplifier realizations, the stray capacitance mismatch dominates simply because the stray capacitances are relatively large (this can be trimmed out in a discrete amplifier). In a hybrid circuit such as the LH0038, stray capacitance is minimized, so the effects of mismatch are also minimized.

The response to a pulse or noise spike applied as a common-mode signal may be dominated by the slew characteristics of the input stage. Whenever the common-mode input slew rate exceeds 0.2 V/μs, the 2 input amplifiers will apply identical ramp signals to the final stage and cause its output to go to near 0V. Note that the amplifier is not really active under these conditions as normal mode signal variations will *not* be coupled to the output. Some time may be required for the amplifier to settle after a transient of this kind before the output can be considered representative of the input. Slew rate limiting will not normally be the limiting factor for sine wave common-mode signals as 0.2 V/μs corresponds to about 2 kHz (20 Vp-p).

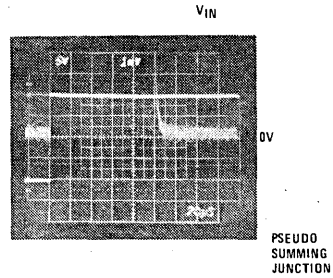
POWER SUPPLY DECOUPLING

Although the LH0038 exhibits in excess of 120 dB PSRR at DC, the figure degrades to 100 dB at 120 Hz. It is recommended that both V^+ and V^- leads be bypassed with 1 μF electrolytic in shunt with 0.01 μF ceramic disc no further than 1 inch from the device.



t_s, A_V = 100, V_{IN} = −20V

FIGURE 11. Settling Time



t_s, A_V = 100, V_{IN} = 20V

FIGURE 12. Settling Time

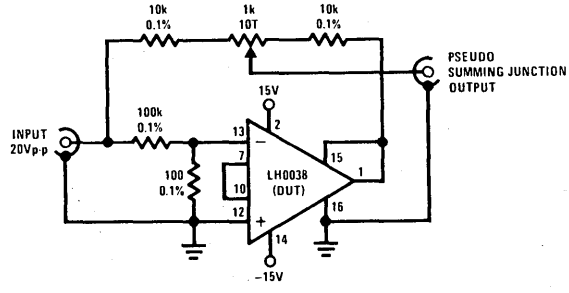


FIGURE 13. Settling Time Test Circuit

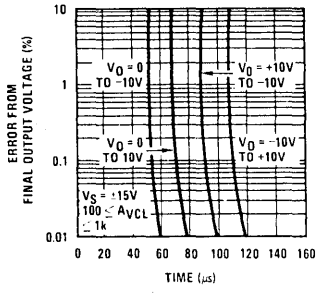


FIGURE 14. Settling Time

Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to 3 dB below the low frequency value.

Common-Mode Rejection Ratio, CMRR: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Input Offset Voltage, V_{IOS}: The voltage which must be applied to the inputs to force the outputs of the input stage to 0V. V_{IOS} can be calculated by measuring V_{OS} at closed loop gains of 100 and 2000 and using the following equation:

$$V_{IOS} = \frac{(V_{OS})\ 2k - (V_{OS})\ 100}{1900}$$

Where:

$(V_{OS})2k$ = overall offset voltage for A_{VCL} = 2k.

$(V_{OS})100$ = overall offset voltage for A_{VCL} = 100.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end points expressed as a percent of full-scale (10V for operations on ±15V supply). Note that this is a more stringent specification than deviation from the best straight line and is double the number that would be specified if the percentage were based on a 20V (±10V) range.

Guard Voltage Error: The voltage difference between the guard drive output and the average of the 2 input voltages.

Input Bias Current, I_B: The average of the 2 input currents.

Input Common-Mode Voltage Range, V_{INCM}: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Offset Current, I_{OS}: The difference in the currents into the 2 input terminals when the output is at zero.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Overall Offset Voltage, V_{OS}: The output voltage when both inputs are connected to 0V. V_{OS} is composed of input amplifier offset voltage effects, V_{IOS}, and output amplifier effects, V_{OOS}. It is given by:

$$V_{OS} = (A_{VCL})\ (V_{IOS}) - V_{OOS}$$

Where:

A_{VCL} = closed loop gain = 100 to 2k

V_{IOS} = input stage offset voltage

V_{OOS} = output stage offset voltage

Output Offset Voltage, V_{OOS}: The output voltage when the outputs of the input stage are forced to 0V. V_{OOS} may be calculated by measuring V_{OS} at closed loop gains of 100 and 2000 and using the following equation:

$$V_{OOS} = \frac{(20)\ (V_{OS})\ 100 - (V_{OS})\ 2k}{19}$$

Where:

$(V_{OS})\ 100$ = overall offset voltage for A_{VCL} = 100

$(V_{OS})\ 2k$ = overall offset voltage for A_{VCL}

Output Voltage, V_O: The peak output voltage swing, referred to zero.

Offset Voltage Temperature Drift, $\Delta V_{IOS}/\Delta T$: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection Ratio, PSRR: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Times, t_s: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate, S_r: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current, $\pm I_S$: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Supply Voltage Range: The range of voltages on the supply terminals for which the device is operational. Note that the specifications are not guaranteed over the full supply voltage range unless specifically stated.

Transient Response, t_r: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from DC to the frequency where the amplifier open loop gain rolls off to 1.

Closed Loop Gain, A_{VCL}: The ratio of output voltage to input voltage under the stated conditions of source resistance (R_S) and load resistance (R_L).

Voltage Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

National Semiconductor

LH0084/LH0084C Digitally-Programmable-Gain Instrumentation Amplifier

General Description

The LH0084/LH0084C is a self-contained, high speed, high accuracy, digitally-programmable-gain instrumentation amplifier. It consists of paired FET-input variable-gain voltage-follower input stages followed by a differential-to-single-ended output stage. The input stage is programmable in accurate gain steps of 1, 2, 5, or 10 controlled by the logic levels of a 2-bit TTL-compatible digital input word. For additional flexibility, the output stage is pin-strappable to fixed gains of 1, 4, or 10 for an overall gain range of 1 to 100.

Applications include increased dynamic range A-to-D converters, test systems, and post multiplexer amplifier for data acquisition systems.

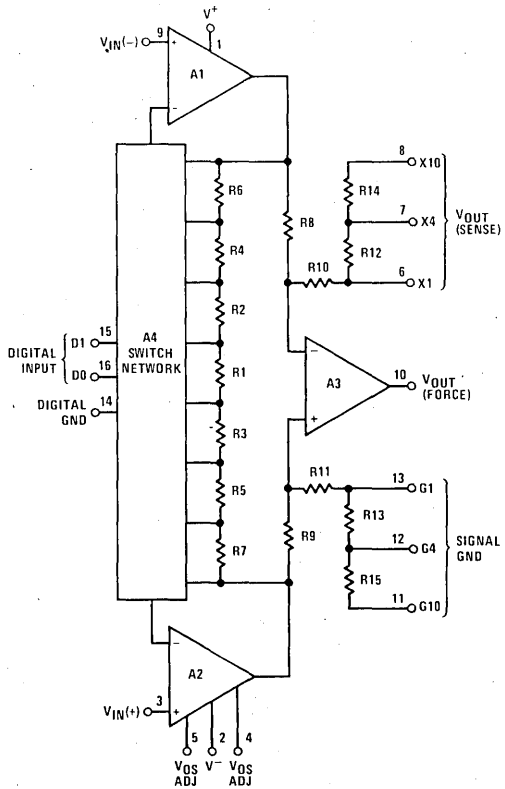
The device exhibits high input impedance, low offset voltage, high CMRR and PSRR, high speed, and excellent gain accuracy and gain non-linearity.

The LH0084 is guaranteed from −55°C to +125°C. The LH0084C is guaranteed from −25°C to +85°C. Both devices are provided in a hermetically sealed 16-lead dual-in-line metal package.

Features

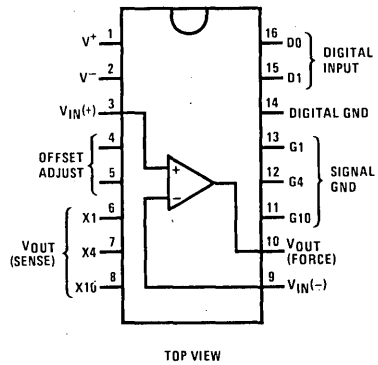
■ Excellent gain accuracy and gain non-linearity	0.05% max 0.01% typ
■ Extremely low gain drift	1 ppm/°C typ 10 ppm/°C max
■ High input impedance	$10^{11}\Omega$ typ
■ High CMRR and PSRR	70 dB min
■ TTL compatible digital inputs	
■ High speed, settling to 0.1%	4 μs max

Simplified Schematic



Connection Diagram

Dual-In-Line Package



TOP VIEW

Case is electrically isolated

Order Number LH0084D or LH0084CD
See NS Package D16D

Absolute Maximum Ratings

Supply Voltage (Note 1)	± 18V	Output Short Circuit Duration	Continuous
Analog Input Voltage (Note 2)	± 15V	Operating Temperature Range	
Differential Input Voltage (Note 2)	± 30V	LH0084	− 55°C to + 125°C
Digital Input Voltage	− 4V, + 18V	LH0084C	− 25°C to + 85°C
Power Dissipation (See Curve)	2.5W	Storage Temperature	− 65°C to + 150°C
		Lead Temperature (Soldering, 20 seconds)	+ 300°C

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$ unless noted

Parameter		Conditions		LH0084 Min	LH0084 Typ	LH0084 Max	LH0084C Min	LH0084C Typ	LH0084C Max	Units
V_{IOS}	Input Offset Voltage		$T_j = 25°C$		0.3	5		0.3	10	mV
						7			13	
$\Delta V_{IOS}/\Delta T$	Input Offset Voltage Change with Temperature	$R_S = 100\Omega$, $V_{CM} = 0$			10			10		µV/°C
V_{OOS}	Output Offset Voltage	(Note 3)	$T_j = 25°C$		0.6	5		0.6	10	mV
						7			13	
$\Delta V_{OOS}/\Delta T$	Output Offset Voltage Change with Temperature				20			20		µV/°C
I_B	Input Bias Current (Note 4)		$T_j = 25°C$		150	500		150	500	pA
						500			100	nA
I_{OS}	Input Offset Current		$T_j = 25°C$		50	200		50	200	pA
						200			50	nA
R_{IN}	Input Resistance	Differential			10^{11}			10^{11}		Ω
		Common-Mode			10^{11}			10^{11}		
V_{IN}	Input Voltage Range			± 10			± 10			V
A_V	Voltage Gain	See Table I			1 2 5 10 20 50 100			1 2 5 10 20 50 100		V/V
	Gain Error	$A_V = 1, 2, 5$	$T_A = 25°C$		0.01	0.05		0.02	0.1	%
		$A_V = 10, 20, 50, 100$			0.02	0.1		0.03	0.2	
		$A_V = 1, 2, 5$			0.02	0.2		0.02	0.2	
		$A_V = 10, 20, 50, 100$			0.03	0.3		0.03	0.3	
	Gain Nonlinearity		$T_A = 25°C$		0.002			0.002		
					0.005			0.005		
$\Delta A_V/\Delta T$	Gain Temperature Coefficient				1	10		1	10	ppm/°C
CMRR	Common-Mode Rejection Ratio	$V_{IN} = \pm 10V$	$A_V = 1$	70	80		70	80		dB
			$A_V = 10$	76	94		76	94		
			$A_V = 100$	80	94		80	94		
PSRR	Power Supply Rejection Ratio	$\pm 8V \le V_S \le \pm 18V$	$A_V = 1$	70	84		70	84		
			$A_V = 10$	76	92		76	92		
			$A_V = 100$	80	104		80	104		
V_O	Output Voltage Swing	$R_L \ge 10\ k\Omega$		± 10	± 12		± 10	± 12		V
I_C	Output Short-Circuit Current		$T_A = 25°C$	± 5	± 18	± 40	± 5	± 18	± 40	mA
				± 2		± 40	± 2		± 40	

DC Electrical Characteristics (Continued) $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$ unless noted

Parameter		Conditions	LH0084			LH0084C			Units
			Min	Typ	Max	Min	Typ	Max	
r_O	Output Resistance			0.05			0.05		Ω
V_{IL}	Digital "0" Input Voltage				0.7			0.7	V
V_{IH}	Digital "1" Input Voltage		2.0			2.0			V
I_{IL}	Digital "0" Input Current	$V_{IN} = 0.4V$		1.5	40		1.5	40	μA
I_{IH}	Digital "1" Input Current	$V_{IN} = 2.4V$		0.01			0.01		μA
V_S	Supply Voltage Range		±8		±18	±8		±18	V
$I_S(+)$	Positive Supply Current	$V_S \le \pm 18V$		12	18		12	26	mA
$I_S(-)$	Negative Supply Current	$V_S \le \pm 18V$		8	12		8	14	mA
P_D	Power Dissipation	$V_S = \pm 15V$		315	450		315	600	mW

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 10\ k\Omega$

Parameter		Conditions		Min	Typ	Max	Units
BW	Bandwidth (*Figure 1*)	Small Signal, −3 dB	$A_V = 1$		3250		kHz
			$A_V = 10$		500		
			$A_V = 100$		350		
		Small Signal, −1%	$A_V = 1$		300		
			$A_V = 10$		75		
			$A_V = 100$		55		
PBW	Power Bandwidth	$V_o = \pm 10V$			200		
SR	Slew Rate	$V_o = \pm 10V$		10	13		V/μs
t_S	Settling Time (*Figure 2*) ±0.1%	$\Delta V_o = \pm 20V$	$A_V = 1$		2.3	3.0	μs
			$A_V = 10$		2.7	3.5	
			$A_V = 100$		3.1	4.0	
	Gain Switching Time				3.5		
E_N	Equivalent Input Noise Voltage (*Figure 3*)	BW = 0.1 Hz-10 Hz	$A_V = 100$		7		μVp-p
		BW = 10 Hz-10 kHz			1.4		μVrms
I_N	Equivalent Input Noise Current (*Figure 3*)	BW = 10 Hz-10 kHz			30		pArms

Note 1: Improper supply power-on sequence may damage the device. See Power Supply Connection section under Applications Information.

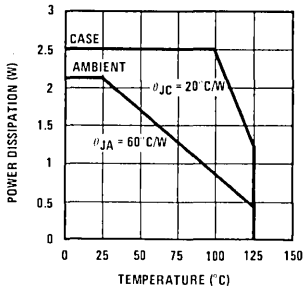
Note 2: For supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.

Note 3: Due to limited production test time, these parameters are specified at junction temperature, T_J. In normal operation the junction temperature rises above the ambient temperature, T_A, as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient.

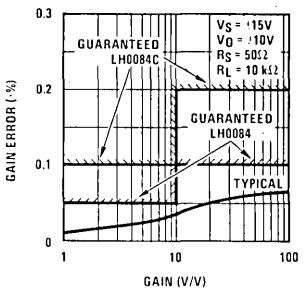
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

Typical Performance Characteristics

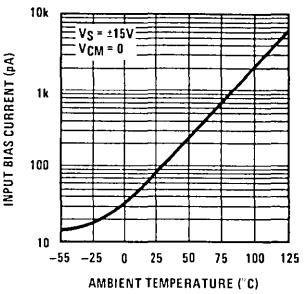
Power Dissipation



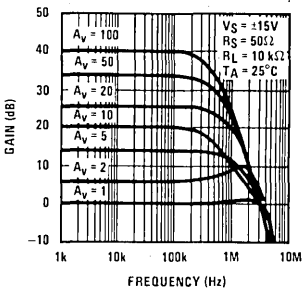
Gain Accuracy



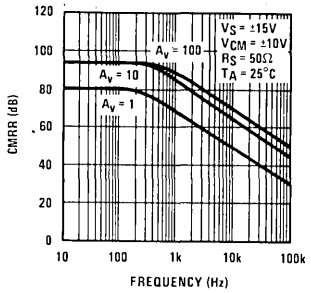
Input Bias Current



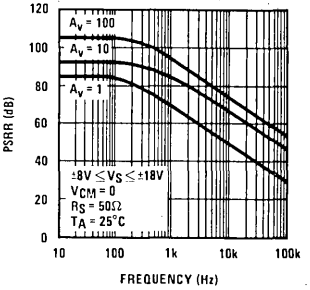
Small Signal Frequency Response



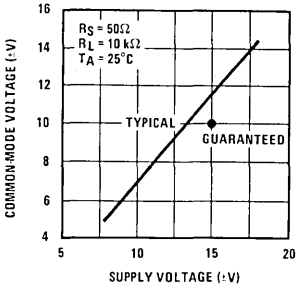
Common-Mode Rejection



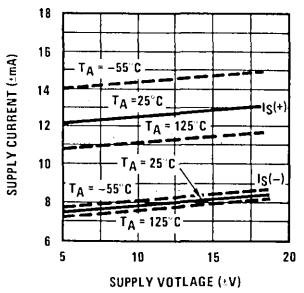
Power Supply Rejection



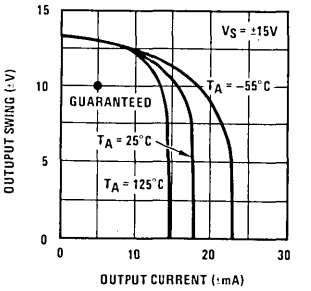
Input Common-Mode Range



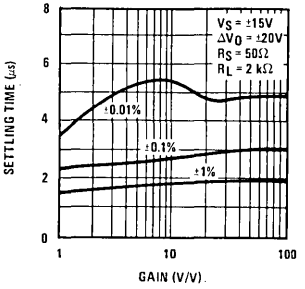
Supply Current



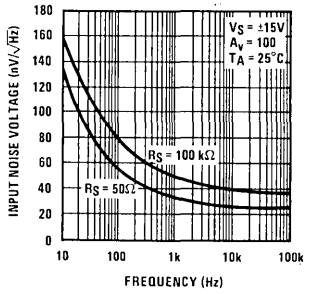
Output Swing



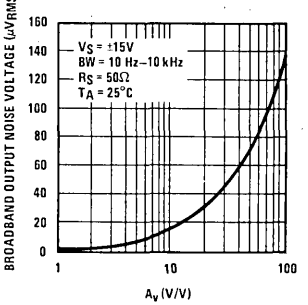
Settling Time



Equivalent Input Noise Voltage (Includes Source-Resistance Noise)



Broadband Output Noise Voltage



AC Test Circuits

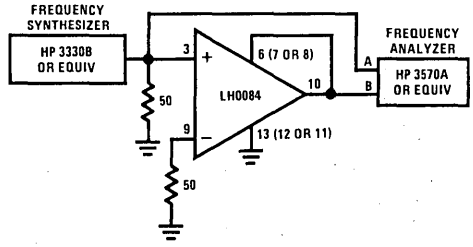


FIGURE 1. Frequency Response Measurement Circuit

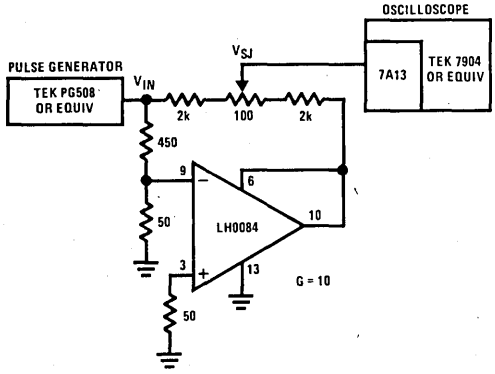
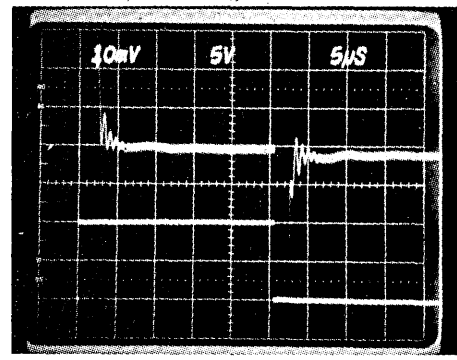


FIGURE 2. Settling Time Measurement Circuit

Settling Time



$A_V = 10$ Input Stage

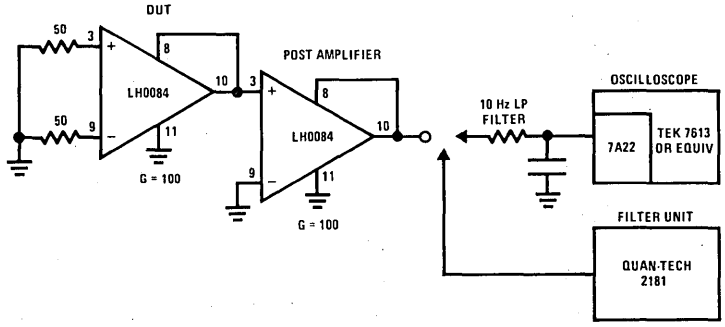
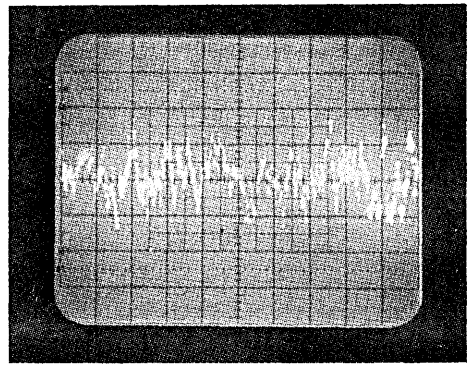


FIGURE 3. Noise Measurement Circuit

Wideband Noise



$R_S = 50\Omega$ Bandwidth 0.1 Hz to 10 Hz
1μV/Division Vertical 5 Seconds/Division Horizontal

Applications Information

THEORY OF OPERATION

The LH0084 is a digitally-programmable-gain true-instrumentation amplifier composed of a variable-gain voltage-follower input stage (A1 and A2), followed by a differential output stage (A3). The schematic is shown in *Figure 4.*

The input stage contains matched high-speed FET-input op amps (A1 and A2). A high-stability temperature-compensated resistor network (R1 through R7) controls feedback ratios at the inverting inputs of op amps A1 and A2 via FET switches S1A-S4A and S1B-S4B. Since the FET switches are in series with the op amp input impedance their resistance match and temperature drift do not degrade the gain accuracy of the instrumentation amplifier. The FET switches are controlled through a 1-of-4 decoder and switch driver, by the logic levels applied at the digital input terminals D1 and D0 and set the gain of the input stage as shown in Table I.

If, for example, D1 is High (≥2.0V) and D0 is Low (≤0.7V), FET switch pair S3A and S3B will be closed (and all remaining switches open). The input stage gain, $A_{V(1)}$, can then be shown to be:

$$A_{V(1)} = \frac{V2 - V1}{V_{IN}(+) - V_{IN}(-)}$$

$$= 1 + \frac{R4 + R5 + R6 + R7}{R1 + R2 + R3} \quad (1)$$

$$= 1 + \frac{6k + 6k + 10k + 10k}{4k + 2k + 2k}$$

$$= 5$$

Schematic Diagram

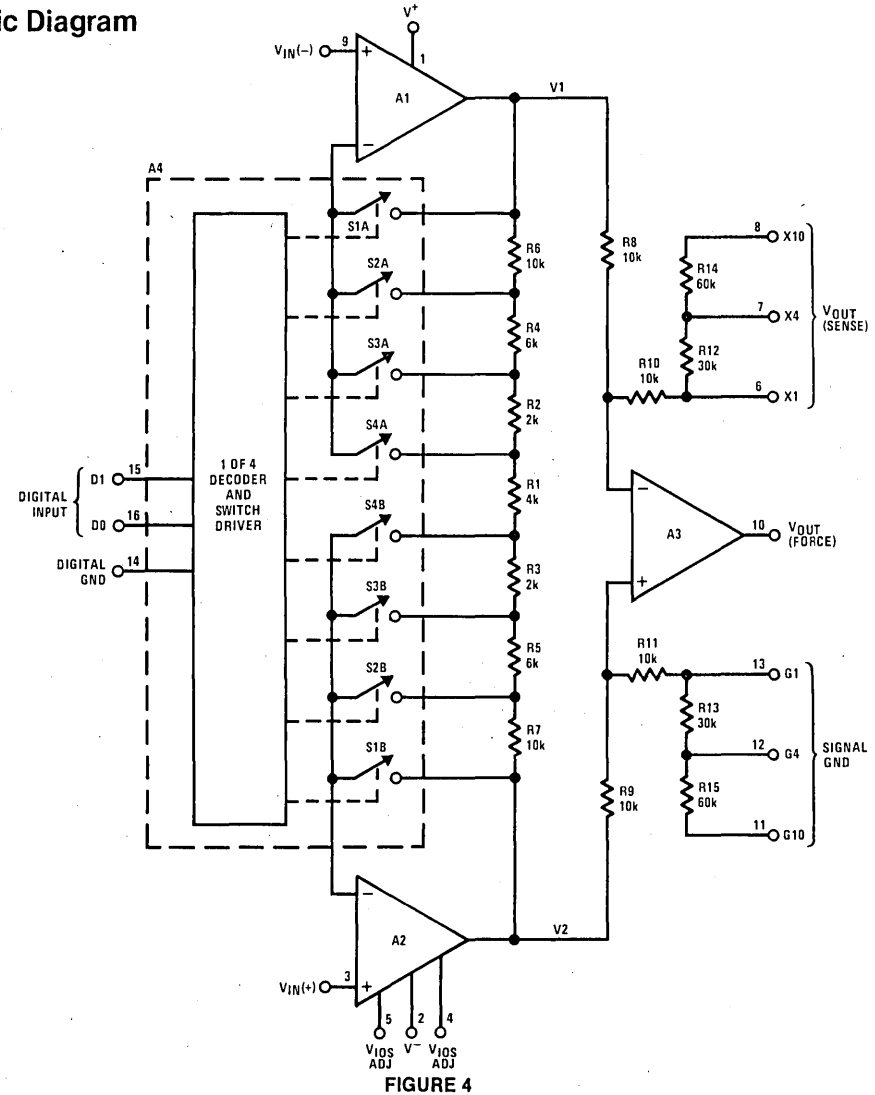


FIGURE 4

Applications Information (Continued)

TABLE I. GAIN TRUTH TABLE AND CONNECTION TABLE

Digital Inputs		1st Stage Gain	Pin Connections	2nd Stage Gain	Overall Gain
D1	D0	$A_{V(1)}$		$A_{V(2)}$	A_V
0	0	1	6-10, 13-GND	1	1
0	1	2			2
1	0	5			5
1	1	10			10
0	0	1	7-10, 12-GND	4	4
0	1	2			8
1	0	5			20
1	1	10			40
0	0	1	8-10, 11-GND	10	10
0	1	2			20
1	0	5			50
1	1	10			100

The output stage, consisting of op amp A3 and resistors R8 through R15, converts the voltage difference at the output of the input stage, V2 minus V1, to a single-ended output. For increased flexibility of the LH0084, the output stage gain is pin-strappable by selecting R10, R10 + R12, or R10 + R12 + R14 as feedback resistor for A3. The ratios of these resistors to the differential stage input resistor R3 are kept very accurate to maintain the excellent overall gain accuracy of the device. The output stage gain, $A_{V(2)}$, is equal to the feedback resistance divided by the input resistance. Thus with, for example, Pin 7 wired to Pin 10, that gain would be:

$$A_{V(2)} = \frac{V_{OUT}}{V2 - V1}$$

$$= \frac{R10 + R12}{R8} \qquad (2)$$

$$= \frac{10k + 30k}{10k}$$

$$= 4$$

To preserve the high common-mode rejection ratio of the output stage, the ground sense resistor, R11, R11 + R13 or R11 + R13 + R15, must match the feedback resistor used.

The overall gain of the LH0084 is therefore:

$$A_V = \frac{V_{OUT}}{V_{IN}(+) - V_{IN}(-)}$$

$$= \frac{V2 - V1}{V_{IN}(+) - V_{IN}(-)} \cdot \frac{V_{OUT}}{V2 - V1} \qquad (3)$$

$$= A_{V(1)} \cdot A_{V(2)}$$

The different gains available are in the range of 1 through 100 and are summarized in Table I.

POWER SUPPLY CONNECTIONS

Proper power supply connections are shown in *Figure 5*. The power supplies should be bypassed to ground as close as possible to device supply pins. For optimum high speed performance V^+ and V^- should be decoupled with a 0.01 μF ceramic disc in parallel with a 1 μF electrolytic capacitor.

The two ground pins, analog and digital grounds, should be connected together as close to the device as possible, preferably with a ground plane underneath the device. If this is not possible, the grounds should be connected together locally with back-to-back diodes and hard-wired together off-board. If a ground reference offset is used, it must be low impedance compared to the ground sense resistance to avoid CMRR degradation.

Care must be taken in the supply power-on sequence. The LH0084 may suffer irreversible damage if the V^+ supply is applied prior to the powering on of the V^- supply. In most applications using dual tracking supplies and with the device supply pins adequately bypassed, this will not present a problem. If this cannot be guaranteed, a germanium or Schottky protection diode should be connected between the digital ground pin and the V^- pin as shown in *Figure 5*.

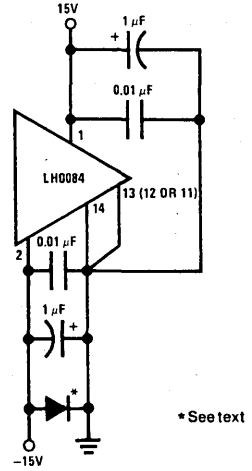


FIGURE 5. Power Supply Connections

Applications Information (Continued)

SIGNAL CONNECTIONS

The input signals should be connected as shown in *Figure 6*. To minimize errors, $R_S(+)$, $R_S(-)$ and R_{CM} should be kept as small as possible.

The output connections are also shown in *Figure 6*. The feedback leads should be kept short as should the ground sense in order to minimize lead resistance and parasitic capacitance.

OFFSET AND GAIN ADJUSTMENTS

Special care must be taken when using external offset adjustment. Since the LH0084 is a 2-stage amplifier with each stage contributing offset errors, and the amplifier presumably is used at several different gains, it is important to realize that the offsets of both the 1st and the 2nd stages must be nulled to maintain zero offset referred to output (RTO) at all gain settings.

In general, it is recommended that the input stage offset (V_{IOS}) be adjusted with a potentiometer as shown in *Figure 7*. The output stage offset (V_{OOS}) is ideally adjusted at a subsequent gain stage (i.e. sample-and-hold or A-to-D converter), but if this is impractical, it may also be done as shown in *Figure 7*.

Recommended offset adjust procedure is as follows: Initially set both pots to center positions and short both inputs of the LH0084 to ground.

a) Set the input stage gain to 1 (pull D1 and D0 low). Measure the output voltage, V_{OUT1}.

b) Set the input stage gain to 10 (pull D1 and D0 high). Measure the new output voltage, V_{OUT2}.

c) Calculate the portion of V_{OUT2} contributed by the output stage offset per the equation:

$$V_{OOS} = \frac{1}{9}(10 \cdot V_{OUT1} - V_{OUT2}) \qquad (4)$$

d) While maintaining an input stage gain of 10, adjust the input offset voltage (V_{IOS}) potentiometer until the output voltage is equal to the voltage calculated in Equation (4).

e) Change the input back to a gain of 1 and adjust the output offset voltage (V_{OOS}) potentiometer until the output voltage is zero.

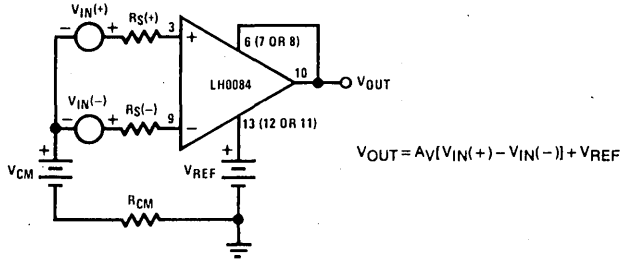


FIGURE 6. Signal Connections

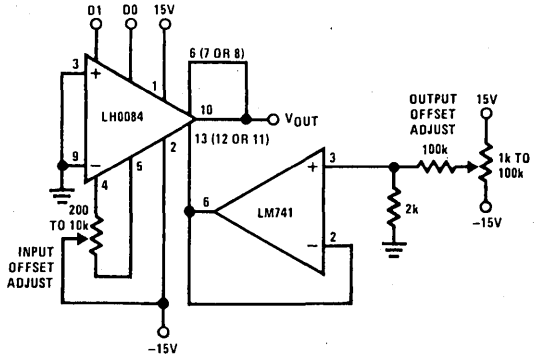


FIGURE 7. Offset Adjust Circuit

Applications Information (Continued)

An alternate offset adjust scheme is shown in *Figure 8*. The offset should be rezeroed after each time the gain is changed or when the op amp integrator drift warrants a new zero pulse. An additional advantage of this adjustment technique is that it can also be used to cancel out offset voltage drift and common-mode voltage error contributions.

External gain adjustment is generally discouraged since gain accuracy can be optimized for one gain setting only. If gain adjustment is required, however, it should be done at a subsequent gain stage.

LOGIC CONNECTIONS

The digital inputs D1 and D0 are referenced to the digital ground. The device interfaces directly to TTL and, with pull-down resistors, to CMOS.

Interfacing with microprocessors will usually require a latch. A circuit using full 6-bit wide address decode and write strobe is shown in *Figure 9*.

REMOTE OUTPUT SENSE

The feedback resistors of the LH0084 can be connected directly at the load in order to eliminate errors due to lead resistance (*Figure 10*).

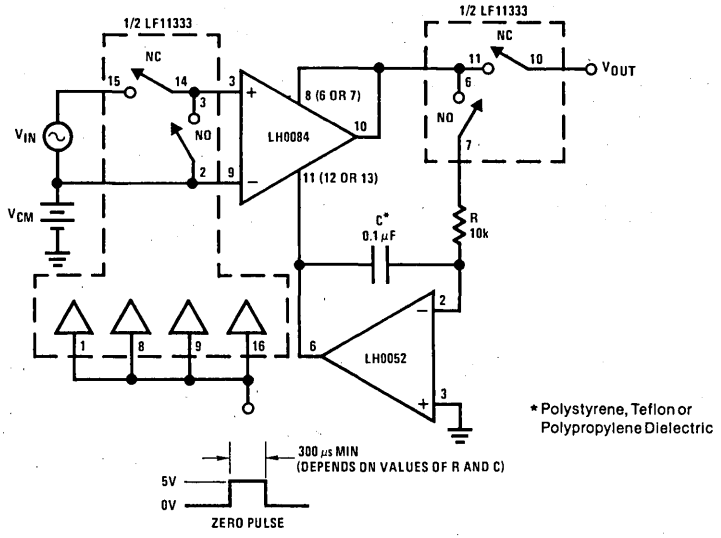


FIGURE 8. Auto Zero Circuit

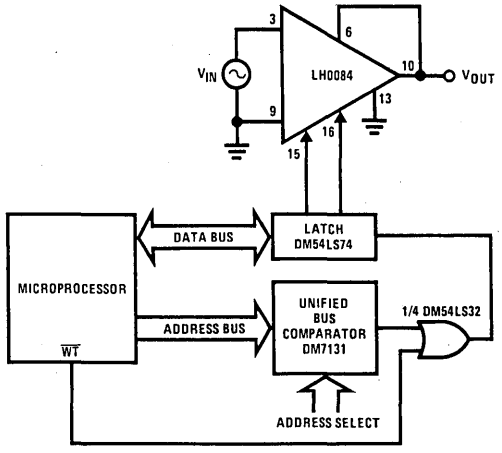


FIGURE 9. Typical Microprocessor Interface

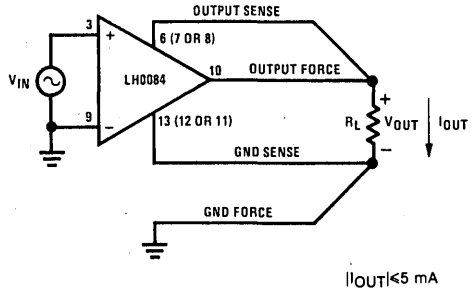


FIGURE 10. Remote Sense Connection

Applications Information (Continued)

Also a unity gain buffer, such as the LH0033, may be included in the feedback loop for increased current drive capability as shown in *Figure 11.*

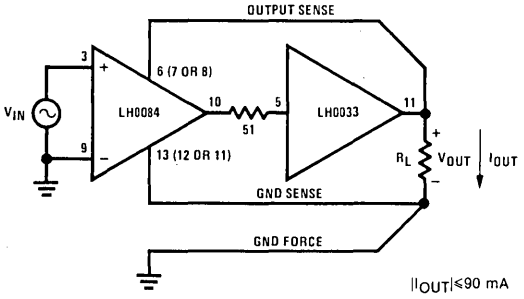


FIGURE 11. Buffered Output Connection

The output sense feature can also be used in other ways such as output offset, *Figure 12*, or current source output, *Figure 13.*

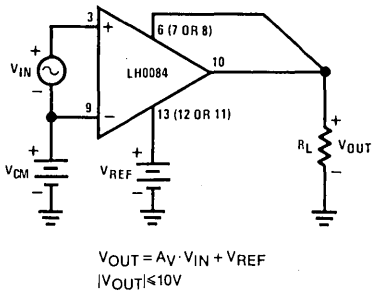


FIGURE 12. Output Offset Connection

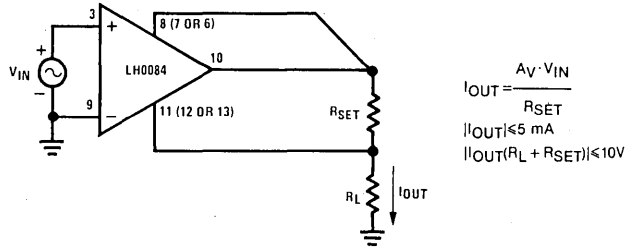


FIGURE 13. Output Current Source Connection

Applications

The LH0084 is ideal for application in increased dynamic range A-to-D converters, test systems, process control, and multi-channel data acquisition systems. *Figure 14* shows the device used in a typical data acquisition-system.

A software offset and gain error correction scheme is shown in *Figure 15.* By first selecting a multiplexer input connected to analog ground, and then selecting a channel connected to a reference of known value, the overall system gain and offset errors can be calculated. For all subsequent readings, offset and gain corrections can be made mathematically by solving a simple first-order equation in software.

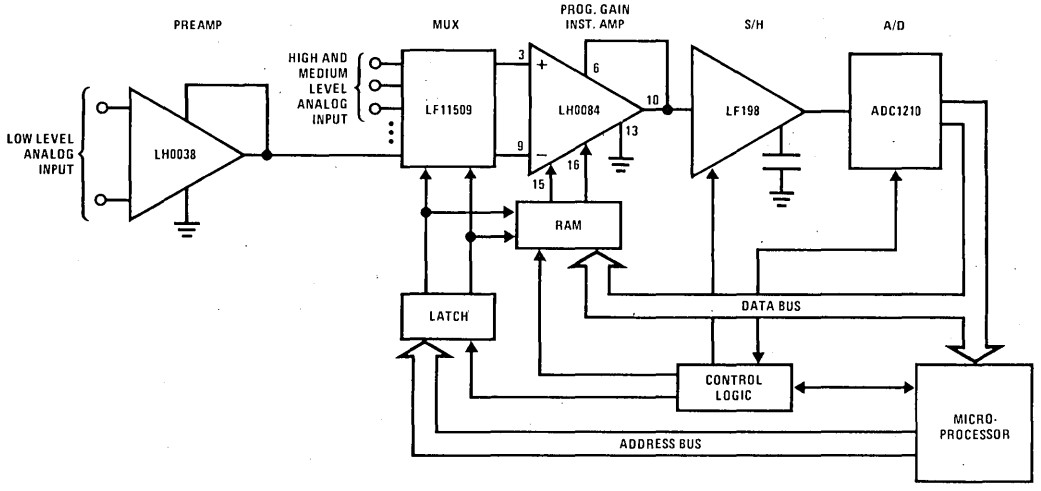


FIGURE 14. Typical Data Acquisition System

Applications (Continued)

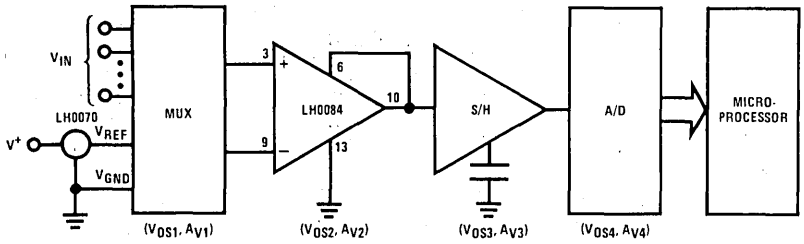


FIGURE 15. Software System Offset and Gain Calibration Circuit

Definition of Terms

Input Offset Voltage, V_{IOS}: The voltage which must be applied to the inputs to force the output of the input stage to 0V. V_{IOS} can be calculated by measuring V_{OS} (RTO) at input stage gains of 1 and 10 and using the following equation:

$$V_{IOS} = \frac{1}{9}\left(V_{OS}\Big|_{A_V=10} - V_{OS}\Big|_{A_V=1}\right)$$

where:

$V_{OS}\Big|_{A_V=10}$ = Overall offset (RTO) for $A_V = 10$

$V_{OS}\Big|_{A_V=1}$ = Overall offset (RTO) for $A_V = 1$

Input Offset Current, I_{OS}: The difference in the currents into the 2 analog input terminals at 0V.

Input Bias Current, I_B: The average of the currents into the 2 analog input terminals at 0V.

Input Resistance, R_{IN}: Common-mode input resistance is the change in input voltage range divided by the change in input bias current with both analog inputs at the same voltage. Differential input resistance is the change in input voltage at one input terminal divided by the change in input current at the other input terminal which is kept still at 0V.

Input Voltage Range, V_{IN}: The voltage range for which the device is operational.

Common-Mode Rejection Ratio, CMRR: The ratio of the input common-mode voltage range to the change in input offset voltage over this range.

Power Supply Rejection Ratio, PSRR: The ratio of the specified change in supply voltage to the change in input offset voltage over this range.

Voltage Gain, A_V: The ratio of output voltage change to the input voltage change producing it.

Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end-points expressed as a percent of full-scale (10V for operation with ±15V supply). For testing purposes it is the difference between positive swing gain (0V to 10V) and average gain (−10V to 10V) or between negative swing gain (0V to −10V) and average gain.

Output Stage Offset Voltage, V_{OOS}: The voltage which must be applied to the input of the output stage for the output to be forced to 0V. V_{OOS} can be calculated by measuring V_{OS} (RTO) at input stage gains of 1 and 10 and applying the following equation:

$$V_{OOS} = \frac{1}{9}\left(10 \cdot V_{OS}\Big|_{A_V=1} - V_{OS}\Big|_{A_V=10}\right)$$

where:

$V_{OS}\Big|_{A_V=1}$ = Overall offset (RTO) for $A_V = 1$

$V_{OS}\Big|_{A_V=10}$ = Overall offset (RTO) for $A_V = 10$

Offset Voltage (Referred to Output), $V_{OS(RTO)}$: The output voltage when both inputs are connected to 0V. V_{OS} is composed of input offset voltage, V_{IOS}, and output offset voltage, V_{OOS}, and is a function of amplifier gain. The overall offset voltage is given by:

$$V_{OS(RTO)} = A_{V(2)}(A_{V(1)}\, V_{IOS} + V_{OOS})$$

where:

V_{IOS} = Input offset voltage

V_{OOS} = Output stage offset voltage

$A_{V(1)}$ = Input stage gain

$A_{V(2)}$ = Output stage gain

Definition of Terms (Continued)

Output Voltage Swing, V_O: The peak output voltage swing referenced to ground into specified load.

Output Short-Circuit Current, I_O: The current supplied by the device with the output connected directly to ground.

Output Resistance, r_o: The ratio of change in output voltage to change in output current around zero output.

Supply Voltage Range, V_S: The supply voltage range for which the device is operational.

Supply Current, I_S: The current required from the supply to operate the device with zero load and with the analog as well as the digital inputs at 0V.

Power Dissipation, P_D: The power dissipated in the device with zero load and with the analog as well as the digital inputs at 0V.

Digital "1" Input Voltage, V_{IH}: Minimum voltage required at the digital input to guarantee a high logic state.

Digital "0" Input Voltage, V_{IL}: Maximum voltage required at the digital input to guarantee a low logic state.

Digital "1" Input Current, I_{IH}: The current into a digital input at specified logic level.

Digital "0" Input Current, I_{IL}: The current into a digital input at specified logic level.

Average Input Offset Voltage Drift, $\Delta V_{IOS}/\Delta T$: The ratio of input offset voltage change from 25°C to either temperature extreme divided by the temperature range.

Average Output Offset Voltage Drift, $\Delta V_{OOS}/\Delta T$: The ratio of output offset voltage change from 25°C to either temperature extreme divided by the temperature range.

Average Gain Temperature Coefficient, $\Delta A_V/\Delta T$: The ratio of change in gain from 25°C to either temperature extreme divided by the temperature range.

Small Signal Bandwidth, BW: The frequency at which the device gain changes from the low frequency gain by a specified amount.

Power Bandwidth, PBW: Maximum frequency for which the output swing is a large signal sinewave without noticeable distortion.

Slew Rate, SR: The internally limited rate of change in output voltage with a large amplitude step function applied at the input.

Settling Time, t_s: The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Gain Switching Time: The time between the initiation of a gain logic change and the time when the final gain switches are closed. It includes overdrive recovery time, but not settling to final value.

Equivalent Input Noise Voltage, E_N: The rms or peak noise voltage referred to the input (RTI) over a specified frequency band.

Equivalent Input Noise Current, I_N: The rms or peak noise current referred to the input (RTI) over a specified frequency band.

National Semiconductor

LH0086/LH0086C Digitally-Programmable-Gain Amplifier

General Description

The LH0086 is a self-contained, high-accuracy, digitally-programmable-gain amplifier. It consists of a FET-input operational amplifier, a precision resistor ladder, and a digitally-programmable switch network. A three-bit TTL-compatible digital input selects accurate gain settings of 1, 2, 5, 10, 20, 50, 100, or 200.

The LH0086 exhibits low offset voltage, high input impedance, fast settling, high power supply rejection ratio, and excellent gain accuracy and gain non-linearity.

The LH0086 is specified for operation from −55°C to +125°C. The LH0086C is specified from −25°C to +85°C. Both devices are hermetically sealed in a 14-lead dual-in-line metal package.

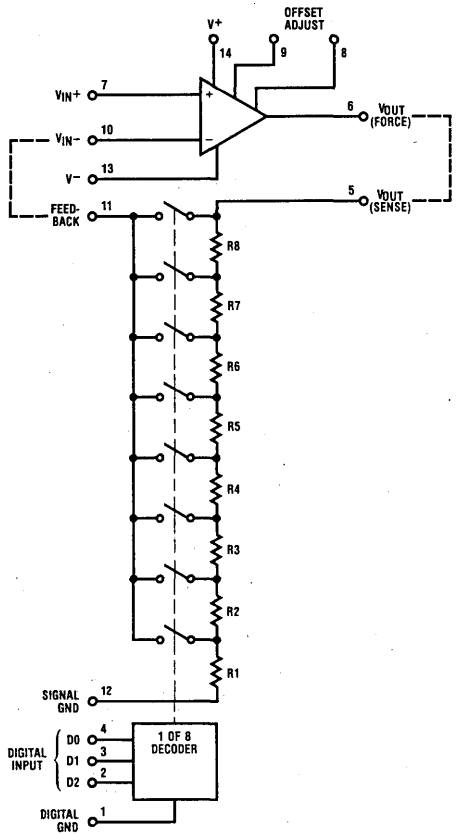
Features

- 0.01% gain accuracy at gain = 1
- 0.005% gain non-linearity
- 1ppm/°C typical gain drift
- $10^{10}\Omega$ input impedance
- 80dB minimum PSRR.
- TTL-compatible digital inputs
- 2μs settling to 0.01%

Applications

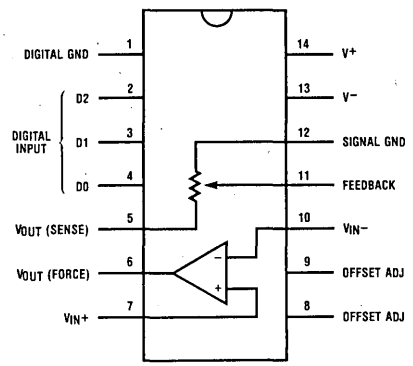
- Data acquisition systems
- Auto range DVMs
- Adaptive servo loops

Simplified Schematic



Connection Diagram

Dual-In-Line Package



CASE IS ELECTRICALLY ISOLATED

Top View

Order Number LH0086D or LH0086CD
See NS Package D14F

Absolute Maximum Ratings

V_S	Supply Voltage (Note 1)	±18V	T_A	Operating Temperature Range:	
V_{IN}	Analog Input Voltage (Note 2)	±15V		LH0086	−55°C to +125°C
$V_{IL(H)}$	Digital Input Voltage	−4V, $+V_S$		LH0086C	−25°C to +85°C
P_D	Power Dissipation	500mW	T_{STG}	Storage Temperature	−65°C to +150°C
	Output Short Circuit Duration	Continuous		Lead Temperature (soldering, 20 seconds)	+300°C

DC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 10k\Omega$, $T_{MIN} \leq T_A \leq T_{MAX}$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting)

Parameter		Conditions		LH0086			LH0086C			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input Offset Voltage		$T_J = 25°C$		0.3	5.0		0.3	10	mV
						7.0			13	
$V_{OS}/\Delta T$	Input Offset Voltage Change with Temperature	$V_{IN} = 0V$			10			10		µV/°C
I_B	Input Bias Current	(Notes 3, 4)	$T_J = 25°C$		100	500		100	500	pA
						500			100	nA
R_{IN}	Input Resistance				10			10		GΩ
V_{IN}	Input Voltage Range			±10	±11.5		±10	±11.5		V
A_V	Voltage Gain	See Table 1, p. 5, for Digital Gain-Control Codes			1.0			1.0		V/V
					2.0			2.0		
					5.0			5.0		
					10			10		
					20			20		
					50			50		
					100			100		
					200			200		
	Gain Error	$A_V = 1$	$T_A = 25°C$		0.003	0.01		0.003	0.03	%
		$A_V = 2,5$			0.03	0.05		0.05	0.1	
		$A_V = 10,20$			0.05	0.1		0.1	0.2	
		$A_V = 50,100,200$			0.1	0.2		0.15	0.3	
		$A_V = 1$			0.003	0.02		0.003	0.06	
		$A_V = 2,5$			0.03	0.1		0.05	0.2	
		$A_V = 10,20$			0.1	0.2		0.1	0.3	
		$A_V = 50,100,200$			0.15	0.3		0.15	0.4	
	Gain Non-Linearity	$A_V = 1$	$T_A = 25°C$		0.002			0.002		%
					0.005			0.005		
$\Delta A_V/\Delta T$	Gain Temperature Coefficient	$A_V = 1$			1.0			1.0		ppm/°C
PSRR	Power Supply Rejection Ratio	$\pm 8V \leq V_S \leq \pm 18V$		80	90		70	90		dB
V_O	Output Voltage Swing	$R_L \geq 10k\Omega$		±10	±12		±10	±12		V

Note 1: Improper supply power-on sequence may damage the device. See Power Supply Connection Section under Applications Information.

Note 2: For supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.

Note 3: Due to short production test time, these parameters are specified at junction temperature, $T_J = 25°C$. In normal operation the junction temperature rises above the ambient temperature, T_A, as a result of the internal power dissipation, PD. $T_J = T_A + \theta_{jA} \times PD$ where θ_{jA} is the thermal resistance from junction to ambient (typically 65°C/W).

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in junction temperature.

DC Electrical Characteristics (cont'd)

$V_S = \pm 15V$, $R_L = 10k\Omega$, $T_{MIN} \leq T_A \leq T_{MAX}$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting).

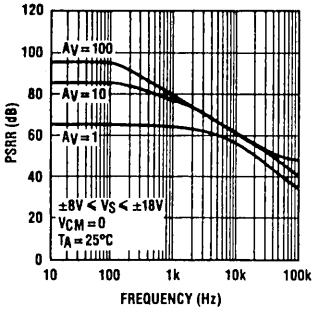
Parameter		Conditions		LH0086			LH0086C			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{SC}	Output Short-Circuit Current		$T_A = 25°C$	±5	±18	±30	±5	±18	±30	mA
				±2		±30	±2		±30	
R_O	Output Resistance	$A_{VCL} = 1$			0.05			0.05		Ω
V_{IL}	Digital "0" Input Voltage					0.7			0.7	V
V_{IH}	Digital "1" Input Voltage			2.0			2.0			
I_{IL}	Digital "0" Input Current	$V_{IN} = 0.4V$			1.5	4.0		1.5	4.0	μA
I_{IH}	Digital "1" Input Current	$V_{IN} = 2.4V$			0.01			0.01		
V_S	Supply Voltage Range			±8.0		±18	±8.0		±18	V
$I_S^{(+)}$	Positive Supply Current	$V_S = \pm 18V$			8.5	15.5		8.5	15.5	mA
$I_S^{(-)}$	Negative Supply Current				−4.5	−8.5		−4.5	−8.5	

AC Electrical Characteristics

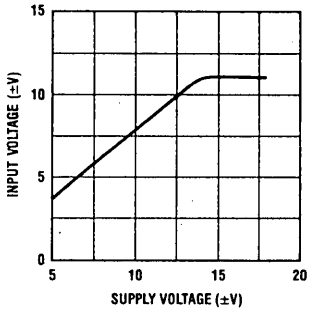
$V_S = \pm 15V$, $T_A = 25°C$, $R_L = 10k\Omega$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting)

Parameter		Conditions		Min.	Typ.	Max.	Units
BW	Small Signal Bandwidth	−3dB	$A_V = 1$		3000		kHz
			$A_V = 50$		60		
			$A_V = 200$		15		
		−1%	$A_V = 1$		425		
			$A_V = 50$		8.5		
			$A_V = 200$		2		
PBW	Power Bandwidth	$V_O = \pm 10V$			159		kHz
SR	Slew Rate				10		V/μs
t_S	Settling Time (Figure 7) 0.01%	$\Delta V_O = 20V$	$A_V = 1$		2.5		μs
			$A_V = 50$		20		μs
			$A_V = 200$		75		
t_S	Settling Time After Gain Change				10		
$\overline{e_N}$	Equivalent Input Noise Voltage (Figure 6)	$R_S = 100\Omega$, $A_V = 100$	BW = 0.1–10Hz		3		μV_{P-P}
			f = 1kHz		25		$nV/\sqrt{Hz}$
$\overline{i_N}$	Equivalent Input Noise Current				0.01		$pA/\sqrt{Hz}$

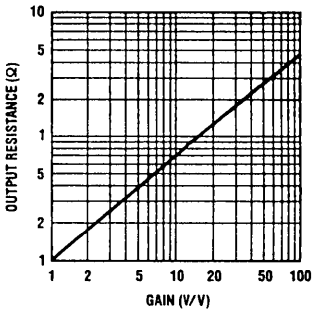
Power Supply Rejection



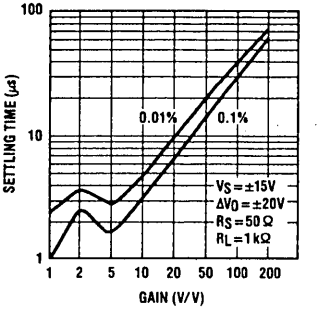
Input Voltage Range



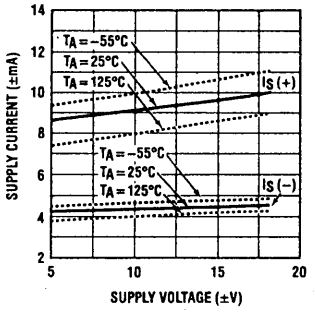
Closed Loop Output Resistance



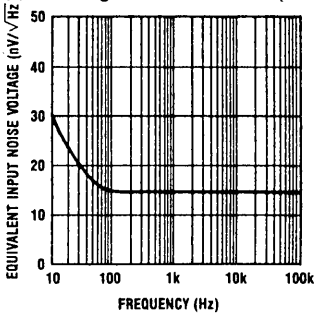
Settling Time



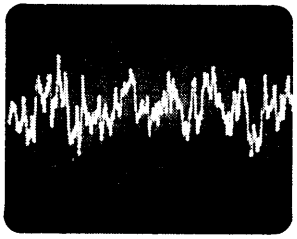
Supply Current



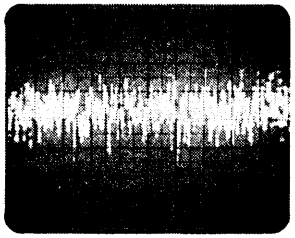
Equivalent Input Noise Voltage



Wideband Noise



$R_S = 50\Omega$. Bandwidth = 0.1 Hz to 10 Hz
1 μV/division Vertical, 5 seconds/division Horizontal



$R_S = 50\Omega$. Bandwidth = 10 Hz to 10 kHz
5 μV/division Vertical, 1 ms/division Horizontal

Applications Information

Theory of Operation

The LH0086 is a digitally programmable gain amplifier with 3-bit digital gain control. It contains a FET-input operational amplifier, a precision resistor ladder, and a digitally programmable switch network.

The LH0086 was designed for use in a non-inverting configuration, thus the following discussion covers the LH0086 as used as a non-inverting amplifier. The gain of the LH0086 is given by the familiar gain equation of a non-inverting amplifier.

$$A_V = 1 + \frac{R_F}{R_S}$$

Each gain step is set by the ratio of the ladder resistors. The resistor ladder is constructed with high stability, low temperature-coefficient resistors precision laser-trimmed to the required values. FET switches are used to select the desired ratio. Since the FET switches are in series with the operational amplifier input, their "on resistance" and temperature drift do not degrade amplifier accuracy. The FET switches are selected by a 1 of 8 decoder, by applying the proper logic levels at digital inputs D0, D1, and D2. The gains are set as given in Table 1.

Table 1. Gain-Control Codes

Gain	D2	D1	D0
1	0	0	0
2	0	0	1
5	0	1	0
10	0	1	1
20	1	0	0
50	1	0	1
100	1	1	0
200	1	1	1

Power Supply Connection

Proper power supply connections are shown in Figure 1. The power supplies should be bypassed to ground as close as possible to device supply pins. For most applications, the bypass capacitor should be 0.1μF.

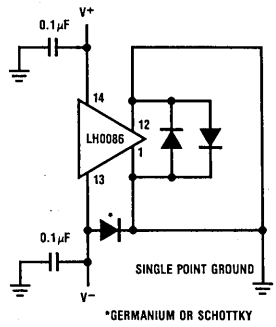


Figure 1. Power Supply and Ground Connections

Care must be taken in the power-on sequence. The LH0086 may suffer irreversible damage if the V^+ supply is applied prior to the powering on of the V^- supply. In most applications using dual-tracking supplies and with the device supply pins adequately bypassed, this will not present a problem. If this cannot be guaranteed, a germanium or Schottky protection diode should be connected between the digital ground pin and the V^- pin as shown in Figure 1.

Grounding Considerations

Care should be taken in the connection of digital and analog grounds. Digital switching currents can introduce noise on the analog ground pin. If possible, both grounds should go to a ground plane beneath the device, otherwise each ground should be run separately to a single point ground. The idea is to keep digital current from passing through the analog ground line. If long ground leads are used, diode clamps should be placed as close to the device as possible (Figure 1).

Programmable Attenuator

The LH0086 may be used as a programmable attenuator when connected as in Figure 2. The accuracy of this attenuator will be typically 0.1%.

Note: Max. $V_{IN} = \pm 11$ Volts.

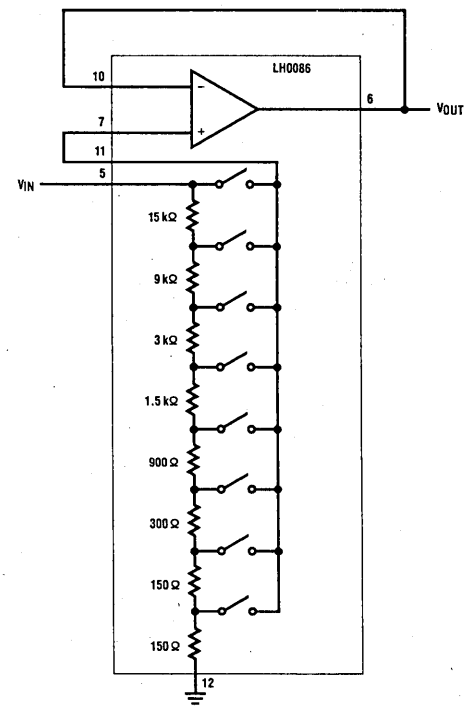


Figure 2. Programmable Attenuator

Table 2. Attenuator Codes

D2	D1	D0	Attenuation
0	0	0	1
0	0	1	2
0	1	0	5
0	1	1	10
1	0	0	20
1	0	1	50
1	1	0	100
1	1	1	200

Table 3. Inverting Gain Chart

D2	D1	D0	Gain	R_{IN} (Ω)
0	0	0	$A_V = 0$	30k
0	0	1	$A_V = 1$	15k
0	1	0	$A_V = 4$	6k
0	1	1	$A_V = 9$	3k
1	0	0	$A_V = 19$	1.5k
1	0	1	$A_V = 49$	600
1	1	0	$A_V = 99$	300
1	1	1	$A_V = 199$	150

Inverting Mode

The LH0086 may be used in the inverting mode, however, there are several design considerations.

1. Input resistance is low at high gains (see gain chart for input resistance at each gain).
2. Each gain step gets a one subtracted from the non-inverting gain. (See inverting gain chart for available gains.)
3. The first gain step (digital code of 000) cannot be used because the output will remain at virtual ground regardless of the input.

Remote Output Sense

The V_{OUT} sense pin of the LH0086 should be connected at the load in order to eliminate errors due to lead resistance. In any case the output sense and output force must be tied together at some point. See Figure 4.

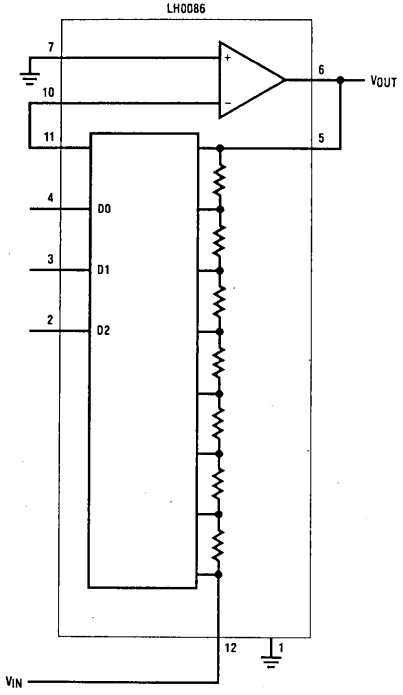


Figure 3. LH0086 Inverting Gain Configuration

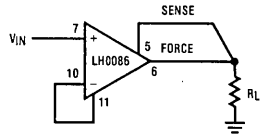


Figure 4. Remote Output Sense

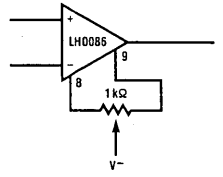


Figure 5. Offset Adjustment

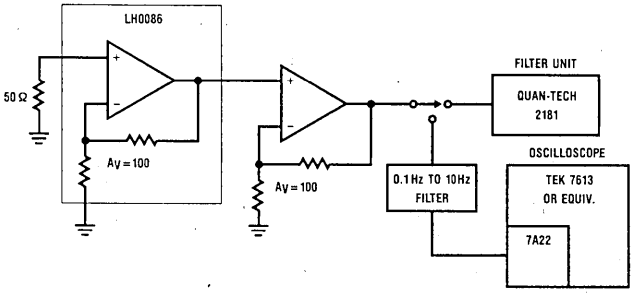


Figure 6. Noise Measurement Circuit

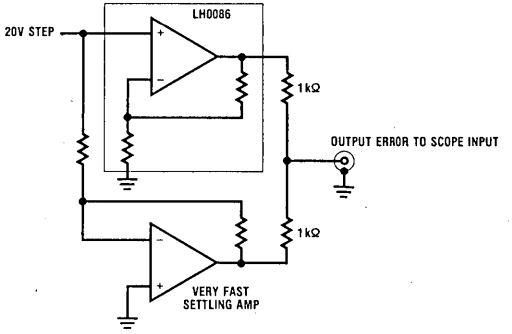


Figure 7. Settling Time Test Circuit

Definition of Terms

V_{OS} **Offset Voltage:** The voltage that must be applied to force the output to 0 volts.

I_B **Input Bias Current:** The current into Pin 7 with the device connected in the non-inverting configuration.

R_{IN} **Input Resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

V_{IN} **Input Voltage Range:** The voltage range for which the device is operational.

PSRR **Power Supply Rejection Ratio:** The ratio of the specified change in supply voltage to the change in input offset voltage over this range.

A_V **Voltage Gain:** The ratio of output voltage change to the input voltage change producing it.

Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the endpoints expressed as a percent of full scale (10V for operation with ±15V supplies). For testing purposes it is the difference between positive swing gain (0V to 10V) and average gain (−10V to 10V) or between negative swing gain (0V to −10V) and average gain.

V_O **Output Voltage Swing:** The peak output voltage swing referenced to ground into specified load.

$I_{O(SC)}$ **Output Short-Circuit Current:** The current supplied by the device with the output connected directly to ground.

R_O **Closed Loop Output Resistance:** The ratio of change in output voltage to change to output current at a specific gain.

V_S **Supply Voltage Range:** The supply voltage range for which the device is operational.

I_S **Supply Current:** The current required from the supply to operate the device with no load and with the analog as well as the digital inputs at 0V.

P_D **Power Dissipation:** The power dissipated in the device with no load and with the analog as well as the digital inputs at 0V.

V_{IH} **Digital "1" Input Voltage:** Minimum voltage required at the digital input to guarantee a high logic state.

V_{IL} **Digital "0" Input Voltage:** The current into a digital input at specified logic level.

$\Delta V_{OS}/\Delta T$ **Average Input Offset Voltage Drift:** The ratio of input offset voltage change from 25°C to either temperature extreme divided by the temperature range.

$\Delta A_V/\Delta T$ **Average Gain Temperature Coefficient:** The ratio in gain from 25°C to either temperature extreme divided by the temperature range.

BW **Bandwidth:** The frequency at which the voltage gain is reduced to 3 dB below the low frequency value.

PBW **Power Bandwidth:** Maximum frequency for which the output swing is a large signal sinewave without noticeable distortion.

SR **Slew Rate:** The internally limited rate of change in output voltage with a large amplitude step function applied at the input.

t_S **Settling Time:** The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Gain Switching Time: The time between the initiation of a gain logic change and the time when the final gain switches are closed. It includes overdrive recovery time, but not settling to final value.

e_N **Equivalent Input Noise Voltage:** The rms or peak noise voltage referred to the input (RTI) over a specified frequency band.

i_N **Equivalent Input Noise Current:** The rms or peak noise current referred to the input (RTI) over a specified frequency band.

Section 4

Sample & Hold Amplifiers

4

Section 4. Sample & Hold Amplifiers

Each of these circuits includes input and output buffer amplifiers and analog switches for a complete sample and hold function.

Features	Accuracy (Max)	Drift Rate ($T_A = 25°C$)	Acquisition Time	Aperture Time	Part Number		Page Number
					−55°C to 125°C	−25°C to 85°C	
Monolithic	±0.02%	30 mV/s (Note 1)	4 μs (Note 1) 20 μs (Note 2)	25 ns	LF198	LF298	4-18
Low Drift	±0.01% ±0.02%	2 mV/s (Note 2)	50 μs (Note 2)	150 ns	LH0023G	LH0023CG	4-4
Medium Speed	±0.1% ±0.3%	25 mV/s (Note 1)	10 μs (Note 1)	20 ns	LH0043G	LH0043CG	4-4
High Speed	±0.2% ±0.3%	30 mV/s (Note 1)	5 μs (Note 1)	25 ns	LH0053G	LH0053CG	4-12

Note 1: $C_S = 1000\,pF$.
Note 2: $C_S = 0.01\,\mu F$.

National Semiconductor

LH0023/LH0023C, LH0043/LH0043C Sample and Hold Circuits

General Description

The LH0023/LH0023C and LH0043/LH0043C are complete sample and hold circuits including input buffer amplifier, FET output amplifier, analog signal sampling gate, TTL compatible logic circuitry and level shifting. They are designed to operate from standard ±15V DC supplies, but provision is made on the LH0023/LH0023C for connection of a separate +5V logic supply in minimum noise applications. The principal difference between the LH0023/LH0023C and the LH0043/LH0043C is a 10:1 trade-off in performance on sample accuracy vs sample acquisition time. Devices are pin compatible except that TTL logic is inverted between the two types.

The LH0023/LH0023C and LH0043/LH0043C are ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup. They offer significant cost and size reduction over equivalent module or discrete designs. Each device is available in a hermetic TO-8 package and are completely specified over both full military and instrument temperature ranges.

The LH0023 and LH0043 are specified for operation over the −55°C to +125°C military temperature range. The LH0023C and LH0043C are specified for operation over the −25°C to +85°C temperature range.

Features

LH0023/LH0023C

- Sample accuracy—0.01% max
- Hold drift rate—0.5 mV/sec typ
- Sample acquisition time—100 μs max for 20V
- Aperture time—150 ns typ
- Wide analog range—±10V min
- Logic input—TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

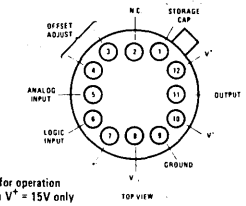
Features

LH0043/LH0043C

- Sample acquisition time—15 μs max for 20V
  4 μs typ for 5V
- Aperture time—20 nS typ
- Hold drift rate—1 mV/sec typ
- Sample accuracy—0.1% max
- Wide analog range—±10V min
- Logic input—TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

Block and Connection Diagrams

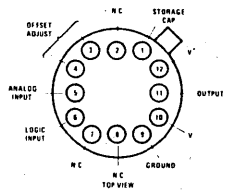
LH0023/LH0023C

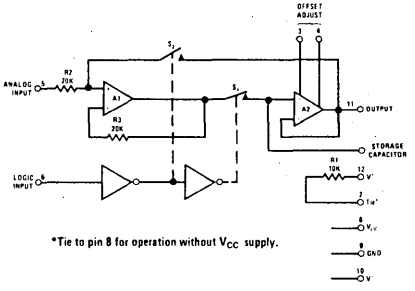


*Tie for operation with V^+ = 15V only

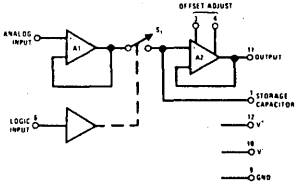
Order Number LH0023G or LH0023CG or LH0043G or LH0043CG
See Package H12B

LH0043/LH0043C





*Tie to pin 8 for operation without V_{CC} supply.



Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)		±20V
Logic Supply Voltage (V_{CC})	LH0023, LH0023C	+7.0V
Logic Input Voltage (V_6)		+5.5V
Analog Input Voltage (V_5)		±15V
Power Dissipation		See graph
Output Short Circuit Duration		Continuous
Operating Temperature Range	LH0023, LH0043	−55°C to +125°C
	LH0023C, LH0043C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Soldering (10 sec)		300°C

Electrical Characteristics LH0023/LH0023C (Note 1)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0023			LH0023C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Sample (Logic "1") Input Voltage	V_{CC} = 4.5V	2.0			2.0			V
Sample (Logic "1") Input Current	V_6 = 2.4V, V_{CC} = 5.5V			5.0			5.0	μA
Hold (Logic "0") Input Voltage	V_{CC} = 4.5V			0.8			0.8	V
Hold (Logic "0") Input Current	V_6 = 0.4V, V_{CC} = 5.5V			0.5			0.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current – I_{10}	V_5 = 0V, V_6 = 2V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current – I_{12}	V_5 = 0V, V_6 = 0.4V, V_{11} = 0V		4.5	6		4.5	6	mA
Supply Current – I_8	V_8 = 5.0V, V_5 = 0		1.0	1.6		1.0	1.6	mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)		0.002	0.01		0.002	0.02	%
DC Input Resistance	Sample Mode	500	1000		300	1000		kΩ
	Hold Mode	20	25		20	25		kΩ
Input Current – I_5	Sample Mode		0.2	1.0		0.3	1.5	μA
Input Capacitance			3.0			3.0		pF
Leakage Current – pin 1	V_5 = ±10V; V_{11} = ±10V, T_A = 25°C		10.0	200		20.0	500	pA
	V_5 = ±10V; V_{11} = ±10V			2.5			2	nA
Drift Rate	V_{OUT} = ±5V, C_S = 0.01 μF, T_A = 25°C		0.5			0.5		mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF, T_A = 25°C		1.0	20		2.0	50	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF			0.50			0.2	mV/ms
Aperture Time			150			150		ns
Sample Acquisition Time	ΔV_{OUT} = 20V, C_S = 0.01 μF		50	100		50	100	μs
Output Amplifier Slew Rate		1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	$R_S \leq$ 10k, V_5 = 0V, V_6 = 2.0V			±20			±20	mV
Analog Voltage Output Range	$R_L \geq$ 1k, T_A = 25°C	±10	±11		±10	±11		V
	$R_L \geq$ 2k	±10	±12		±10	±12		V

Note 1: Unless otherwise noted, these specifications apply for V^+ = +15V, V_{CC} = +5V, V^- = −15V, pin 9 grounded, a 0.01μF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0023, and −25°C to +85°C for the LH0023C. All typical values are for T_A = 25°C.

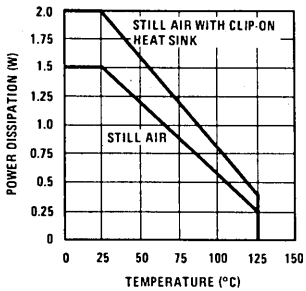
Electrical Characteristics LH0043/LH0043C: (Note 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0043			LH0043C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Hold (Logic "1") Input Voltage		2.0			2.0			V
Hold (Logic "1") Input Current	V_6 = 2.4V			5.0			5.0	μA
Sample (Logic "0") Input Voltage				0.8			0.8	V
Sample (Logic "0") Input Current	V_6 = 0.4V			1.5			1.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	V_5 = 0V, V_6 = 2V, V_{11} = 0V V_5 = 0V, V_6 = 0.4V, V_{11} = 0V		20 14	22 18		20 14	22 18	mA mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)		0.02	0.1		0.02	0.3	%
DC Input Resistance	T_C = 25°C	10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Current – I_5			1.0	5.0		2.0	10.0	nA
Input Capacitance			1.5			1.5		pF
Leakage Current–pin 1	V_5 = ±10V; V_{11} = ±10, T_C = 25°C		10	25		20	50	pA
	V_5 = ±10V; V_{11} = ±10V		10	25		2	5	nA
Drift Rate	V_{OUT} = ±10V, C_S = 0.001 μF, T_C = 25°C		10	25		20	50	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.001 μF		10	25		2	5	mV/ms
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF, T_C = 25°C		1	2.5		2	5	mV/s
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF		1	2.5		0.2	0.5	mV/ms
Aperture Time			20	60		20	60	ns
Sample Acquisition Time	ΔV_{OUT} = 20V, C_S = 0.001 μF ΔV_{OUT} = 20V, C_S = 0.01 μF ΔV_{OUT} = 5V, C_S = 0.001 μF		10 30 4	15 50		10 30 4	15 50	μs μs μs
Output Amplifier Slew Rate	V_{OUT} = 5V, C_S = 0.001 μF	1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	$R_S \leq$ 10k, V_5 = 0V, V_6 = 0V			±40			±40	mV
Analog Voltage Output Range	$R_L \geq$ 1k, T_A = 25°C $R_L \geq$ 2k	±10 ±10	±11 ±12		±10 ±10	±11 ±12		V V

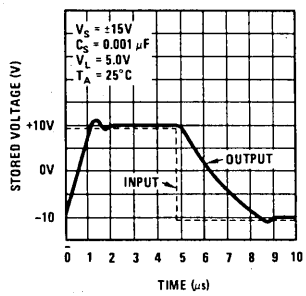
Note 2: Unless otherwise noted, these specifications apply for V^+ = +15V, V^- = −15V, pin 9 grounded, a 5000 pF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0043, and −25°C to +85°C for the LH0043C. All typical values are for T_C = 25°C.

Typical Performance Characteristics

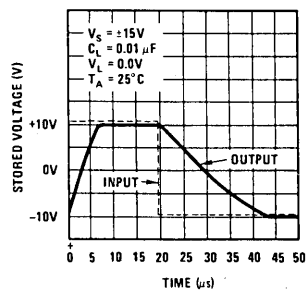
Power Dissipation



Sample Acquisition Time–LH0043

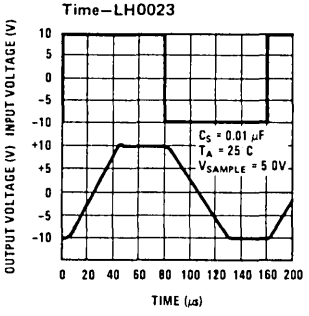


Sample Acquisition Time–LH0043

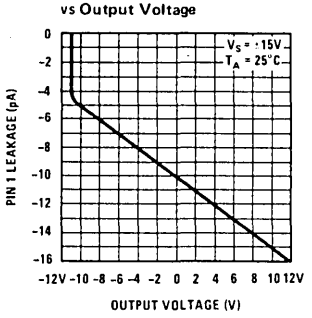


Typical Performance Characteristics (Continued)

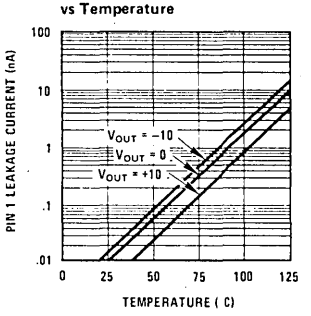
Sample Acquisition Time—LH0023



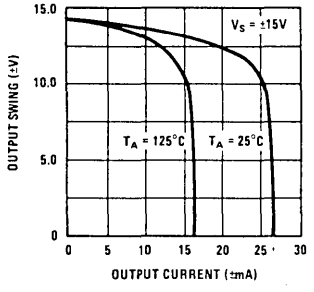
Pin 1 Leakage Current vs Output Voltage



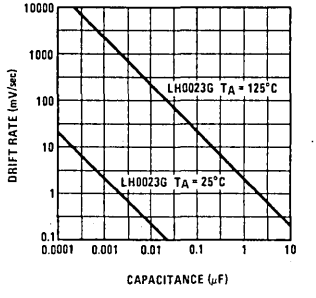
Pin 1 Leakage Current vs Temperature



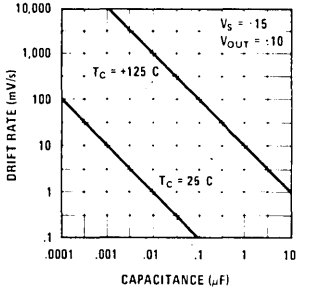
Output Current Limiting



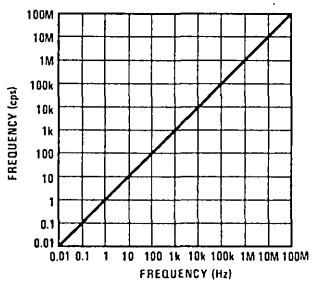
Drift vs Capacitance (LH0023)



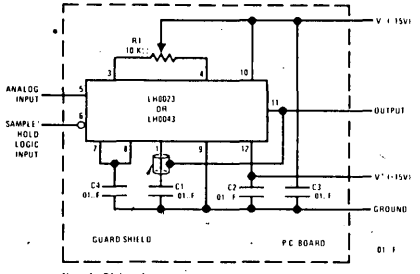
Drift vs Capacitance (LH0043)



(LH0023)



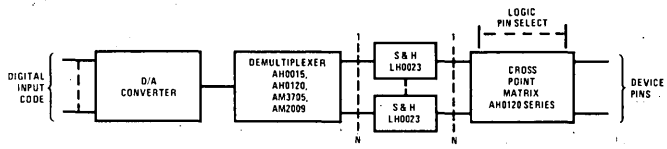
Typical Applications



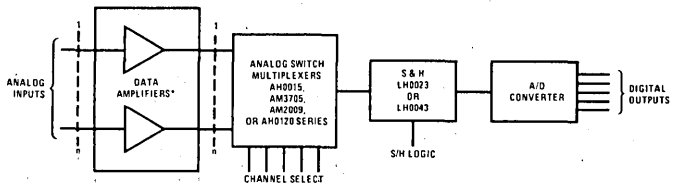
Note 1: C1 is polystyrene.
Note 2: C2, C3, C4 are ceramic disc.
Note 3: Jumper 7–8 and C4 not required for LH0043.
Note 4: R1 optional if zero trim is required.

How to Build a Sample and Hold Module

Typical Applications (Continued)

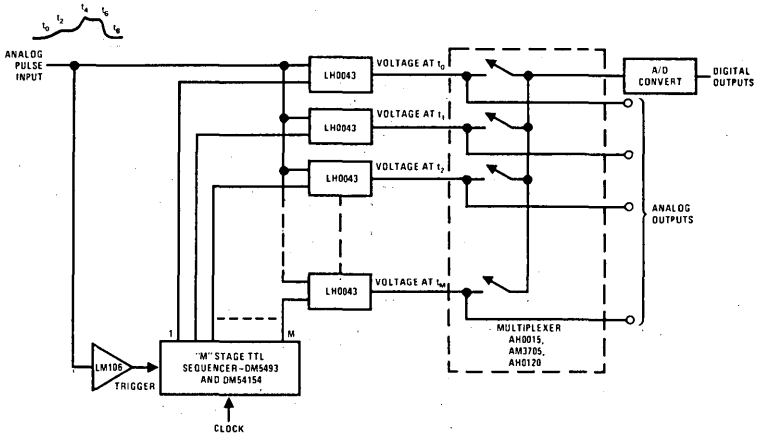


Forcing Function Setup for Automatic Test Gear

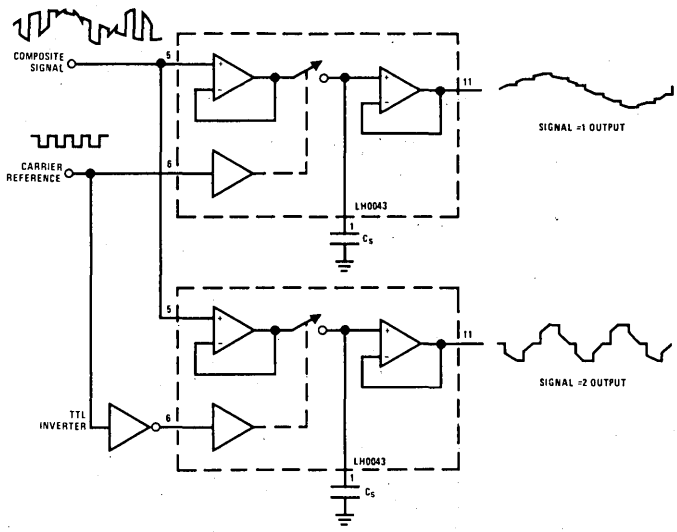


*See op amp selection guide for details. Most popular types include LH0052, LM108, LM112, LH0044, LH0036, and LH0038.

Data Acquisition System



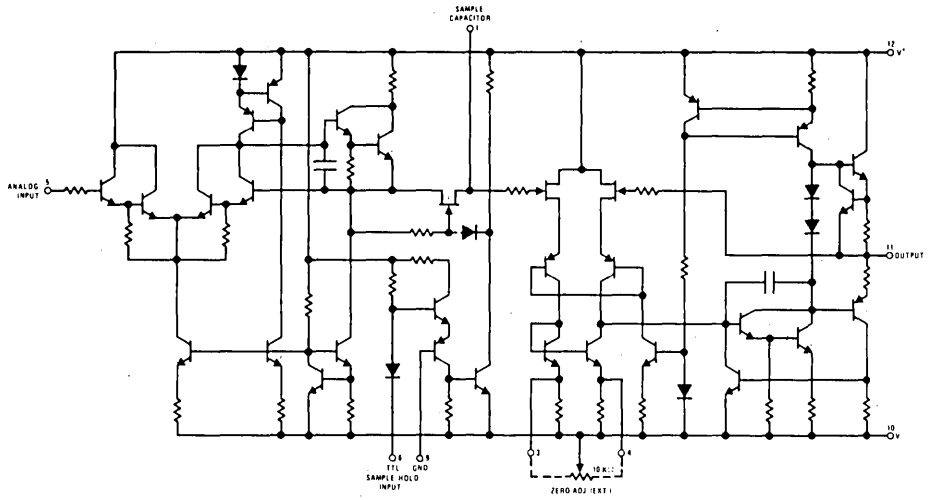
Single Pulse Sampler



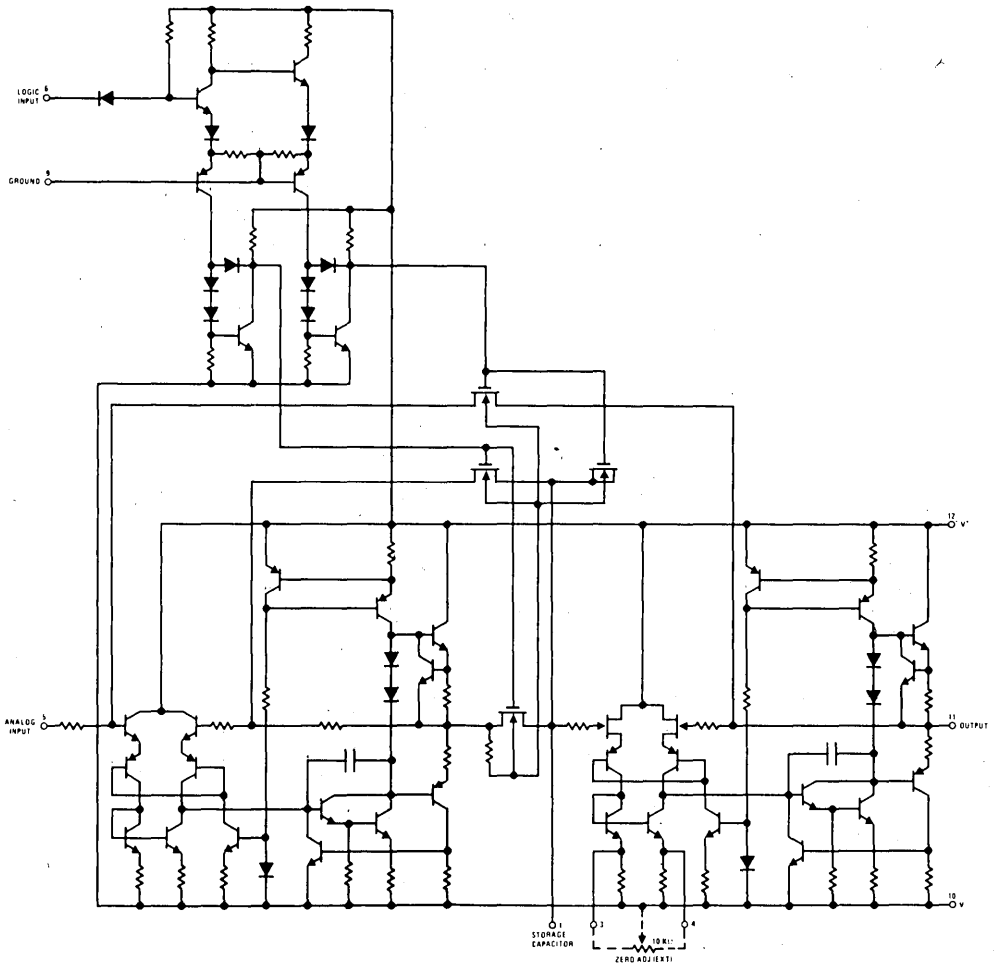
Two Channel Double Sideband Demodulator

Schematic Diagrams

LH0043/LH0043C



LH0023/LH0023C



Applications Information

1.0 Drift Error Minimization

In order to minimize drift error, care in selection of C_S and layout of the printed circuit board is required. The capacitor should be of high quality Teflon, polycarbonate, or polystyrene construction. Board cleanliness and layout are critical particularly at elevated temperatures. See AN-63 for detailed recommendations. A guard conductor connected to the output surrounding the storage node (pin 1) will be helpful in meeting severe environmental conditions which would otherwise cause leakage across the printed circuit board.

2.0 Capacitor Selection

The size of the capacitor is dictated by the required drift rate and acquisition time. The drift is determined by the leakage current at pin 1 and may be calculated by $\frac{dV}{dt} = \frac{I_L}{C_S}$, where I_L is the total leakage current at pin 1 of the device, and C_S is the value of the storage capacitor.

2.1 Capacitor Selection – LH0023

At room temperature leakage current for the LH0023 is approximately 100 pA. A drift rate of 10 mV/sec would require a 0.01 μF capacitor.

For values of C_S up to 0.01 μF the acquisition time is limited by the slew rate of the input buffer amplifier, A1, typically 0.5 V/μs. Beyond this point, current availability to charge C_S also enters the picture. The acquisition time is given by:

$$t_A \cong \sqrt{\frac{2\Delta e_O RC_S}{0.5 \times 10^6}} = 2 \times 10^{-3}\sqrt{\Delta e_O RC_S}$$

where: R = the internal resistance in series with C_S

Δe_O = change in voltage sampled

An average value for R is approximately 600 ohms. The expression for t_A reduces to:

$$t_A \cong \frac{\sqrt{\Delta e_O C_S}}{20}$$

For a –10V to +10V change and C_S = .05 μF, acquisition time is typically 50 μs.

2.2 Capacitor Selection–LH0043

At 25°C case temperature, the leakage current for the LH0043G is approximately 10 pA, so a drift rate of 5 mV/s would require a capacitor of $C_S = 10 \cdot 10^{-12}/5 \cdot 10^{-3} = 2000$ pF or larger.

For values of C_S below about 5000 pF, the acquisition time of the LH0043G will be limited by the slew rate of the output amplifier (the signal will be acquired, in the sense that the voltage will be stored on the capacitor, in much less time as dictated by the slew rate and current capacity of the input amplifier, but it will not be available at the output). For larger values of storage capacitance, the limitation is the current sinking capability of the input amplifier, typically 10 mA. With $C_S = 0.01$ μF, the slew rate can be estimated by $\frac{dV}{dt} = \frac{10 \cdot 10^{-3}}{0.01 \cdot 10^{-6}} = 1$V/$\mu$s or a slewing time for a 5 volt signal change of 5μs.

3.0 Offset Null

Provision is made to null both the LH0023 and LH0043 by use of a 10k pot between pins 3 and 4. Offset null should be accomplished in the sample mode at one half the input voltage range for minimum average error.

4.0 Switching Spike Minimization–LH0043

A capacitive divider is formed by the storage capacitor and the capacitance of the internal FET switch which causes a small error current to be injected into the storage capacitor at the termination of the sample interval. This can be considered a negative DC offset and nulled out as described in (3.0), or the transient may be nulled by coupling an equal but opposite signal to the storage capacitor. This may be accomplished by connecting a capacitor of about 30 pF (or a trimmer) between the logic input (pin 6) and the storage capacitor (pin 1). Note that this capacitor must be chosen as carefully as the storage capacitor itself with respect to leakage. The LH0023 has switch spike minimization circuitry built into the device.

5.0 Elimination of the 5V Logic Supply–LH0023

The 5V logic supply may be eliminated by shorting pin 7 to pin 8 which connects a 10k dropping resistor between the +15V and V_C. Decoupling pin 8 to ground through 0.1 μF disc capacitor is recommended in order to minimize transients in the output.

6.0 Heat Sinking

The LH0023 and LH0043G may be operated without damage throughout the military temperature range of –55 to +125°C (–25 to +85°C for the LH0023CG and LH0043CG) with no explicit heat sink, however power dissipation will cause the internal temperature to rise above ambient. A simple clip-on heat sink such as Wakefield #215–1.9 or equivalent will reduce the internal temperature about 20°C thereby cutting the leakage current and drift rate by one fourth at max. ambient. There is no internal electrical connection to the case, so it may be mounted directly to a grounded heat sink.

7.0 Theory of Operation–LH0023

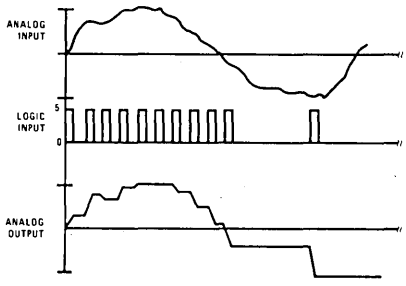
The LH0023/LH0023C is comprised of input buffer amplifier, A1, analog switches, S1 and S2, a

Applications Information (Continued)

TTL to MOS level translator, and output buffer amplifier, A2. In the "sample" mode, the logic input is raised to logic "1" ($V_6 \leq 2.0V$) which closes S1 and opens S2. Storage capacitor, C_S, is charged to the input voltage through S1 and the output slews to the input voltage. In the "hold" mode, the logic input is lowered to logic "0" ($V_6 \leq 0.8V$) opening S1 and closing S2. C_S retains the sample voltage which is applied to the output via A2. Since S1 is open, the input signal is overridden, and leakage across the MOS switch is therefore minimized. With S1 open, drift is primarily determined by input bias current of A2, typically 100 pA at 25°C.

7.1 Theory of Operation—LH0043

The LH0043/LH0043C is comprised of input buffer amplifier A1, FET switch S1 operated by a TTL compatible level translator, and output buffer amplifier A2. To enter the "sample" mode, the logic input is taken to the TTL logic "0" state (V_6 = 0.8V) which commands the switch S1 closed and allows A1 to make the storage capacitor voltage equal to the analog input voltage. In the "hold" mode (V_6 = 2.0V), S1 is opened isolating the storage capacitor from the input and leaving it charged to a voltage equal to the last analog input voltage before entering the hold mode. The storage capacitor voltage is brought to the output by low leakage amplifier A2.



8.0 Definitions

V_5: The voltage at pin 5, e.g., the analog input voltage.

V_6: The voltage at pin 6, e.g., the logic control input signal.

V_{11}: The voltage at pin 11, e.g., the output signal.

T_A: The temperature of the ambient air.

T_C: The temperature of the device case at the center of the bottom of the header.

Acquisition Time:
The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to the input (pin 5) with the logic input (pin 6) in the low state.

Aperture Time:
The time indeterminacy when switching from sample mode to hold including the delay from the time the mode control signal (pin 6) passes through its threshold (1.4 volts) to the time the circuit actually enters the hold mode.

Output Offset Voltage:
The voltage at the output terminal (pin 11) with the analog input (pin 5) at ground and logic input (pin 6) in the "sample" mode. This will always be adjustable to zero using a 10k pot between pins 3 and 4 with the wiper arm returned to V^-.

National Semiconductor

LH0053/LH0053C High Speed Sample and Hold Amplifier

General Description

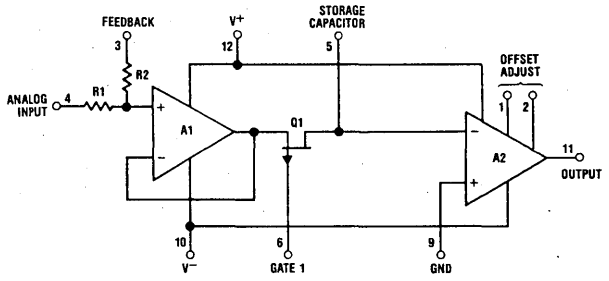
The LH0053/LH0053C is a high speed sample and hold circuit capable of acquiring a 20V step signal in under 5.0μs.

The device is ideally suited for a variety of high speed data acquisition applications including analog buffer memories for A to D conversion and synchronous demodulation.

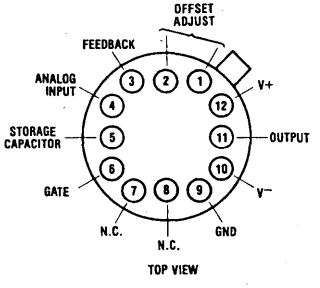
Features

- Sample acquisition time 10μs max. for 20V signal
- FET switch for preset or reset function
- Sample accuracy null
- Offset adjust to 0V
- DTL/TTL compatible FET gate
- Single storage capacitor

Schematic and Connection Diagrams

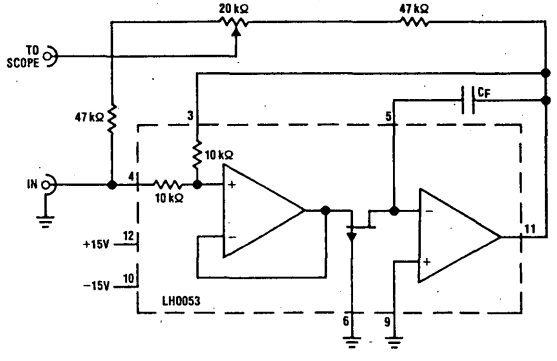


Metal Can Package



Order Number LH0053G or LH0053CG
See Package H12B

AC Test Circuit



Acquisition Time Test Circuit

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	±18V
Gate Input Voltage (V_6)	±20V
Analog Input Voltage (V_4)	±15V
Input Current (I_8 and I_5)	±10mA
Power Dissipation	1.5W
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH0053	−55°C to +125°C
LH0053C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

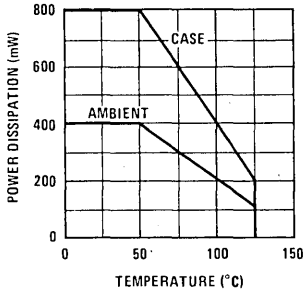
Parameter	Conditions	Limits						Units
		LH0053			LH0053C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Sample (Gate "0") Input Voltage				0.5			0.5	V
Sample (Gate "0") Input Current	$V_6 = 0.5V$, $T_A = 25°C$			−5.0			−5.0	μA
	$V_6 = 0.5V$			−100			−100	μA
Hold (Gate "1") Input Voltage		4.5			4.5			V
Hold (Gate "1") Input Current	$V_6 = 4.5V$, $T_A = 25°C$			1.0				nA
	$V_6 = 4.5V$			1.0				μA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	$V_4 = 0V$, $V_6 = 0.5V$		13	18		13	18	mA
Input Bias Current (I_4)	$V_4 = 0V$, $T_A = 25°C$		120	250		150	500	nA
Input Resistance		5.0	10	15	5.0	10	15	kΩ
Analog Output Voltage Range	$R_L = 2.0kΩ$	±10	±12		±10	±12		V
Output Offset Voltage	$V_4 = 0V$, $V_6 = 0.5V$, $T_A = 25°C$		5.0	7.0		5.0	10	mV
	$V_4 = 0V$, $V_6 = 0.5V$			10			15	mV
Sample Accuracy (Note 2)	$V_4 = ±10V$, $V_6 = 0.5V$, $T_A = 25°C$		0.1	0.2		0.1	0.3	%
Aperture Time	$ΔV_6 = 4.5V$, $T_A = 25°C$		10	25		10	25	ns
Sample Acquisition Time	$V_4 = ±10V$, $T_A = 25°C$, $C_F = 1000pF$, $V_6 = 0V$		5.0	10		8.0	15	μs
Sample Acquisition Time	$V_4 = ±10V$, $T_A = 25°C$, $C_F = 100pF$, $V_6 = 0V$		4.0			4.0		μs
Output Slew Rate	$ΔV_{IN} = ±10V$, $T_A = 25°C$, $C_F = 100pF$, $V_6 = 0V$		20			20		V/μs
Large Signal Bandwidth	$V_4 = ±10V$, $T_A = 25°C$, $C_F = 1000pF$		200			200		kHz
Leakage Current (Pin 5)	$V_4 = ±10V$, $T_A = 25°C$,		6.0	50		10	100	pA
	$V_4 = ±10V$			30			30	nA
Drift Rate	$V_4 = ±10V$, $T_A = 25°C$, $C_F = 1000pF$		6.0	50		10	100	mV/s
Drift Rate	$V_4 = ±10V$, $C_F = 1000pF$			30			30	V/s

Note 1: Unless otherwise noted, these specifications apply for $V_S = ±15V$, pin 9 grounded, a 1000pF capacitor between pin 5 and pin 11, pin 3 shorted to pin 11, over the temperture range −55°C to +125°C for the LH0053 and −25°C to +85°C for the LH0053C. All typical values are for $T_A = 25°C$.

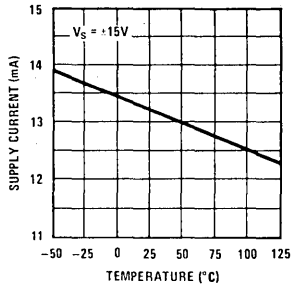
Note 2: Sample accuracy may be nulled by inserting a potentiometer in the feedback loop. This compensates for source impedance and feedback resistor tolerances.

Typical Performance Characteristics

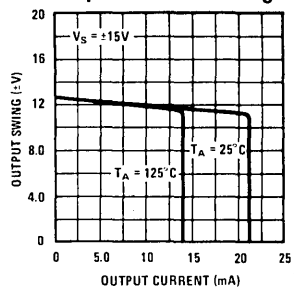
Power Dissipation



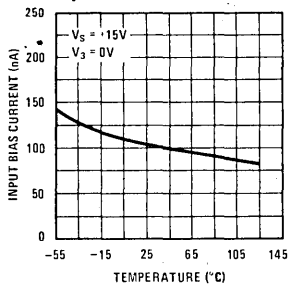
Supply Current vs. Temperature



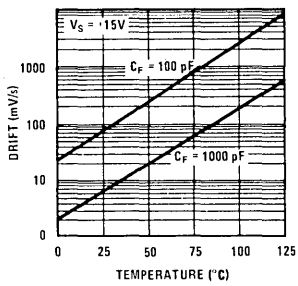
Output Current Limiting



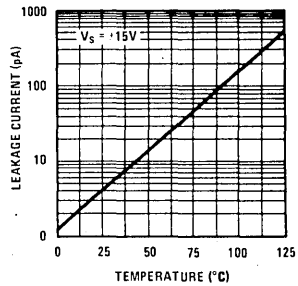
Input Bias Current



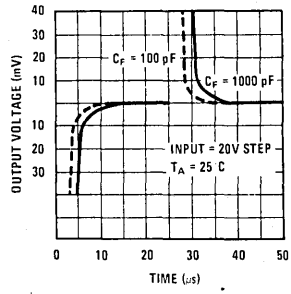
Drift



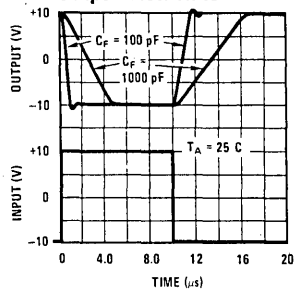
Leakage Current at Pin 5



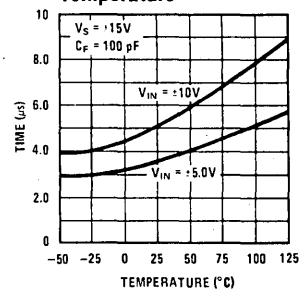
Sample Acquisition Time



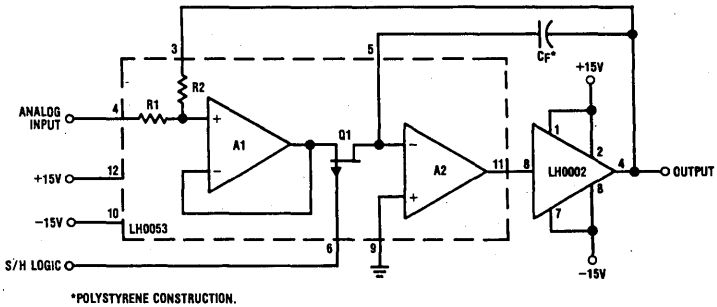
Output Slew Rate



Acquisition Time vs. Temperature

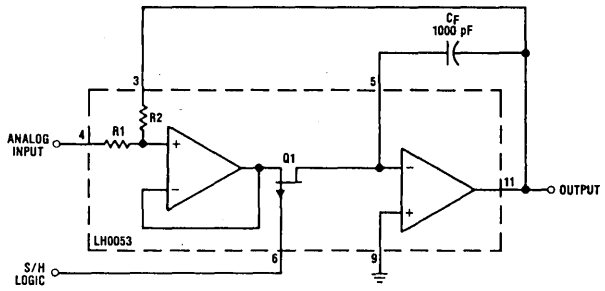


Typical Applications



Increasing Output Drive Capability

Typical Applications (Continued)



Sample and Hold

Applications Information

Source Impedance Compensation

The gain accuracy (linearity) of the LH0053/LH0053C is set by two internal precision resistors. Circuit applications in which the source impedance is non-zero will result in a closed loop gain error, e.g. if $R_S = 10\,\Omega$, a gain error of 0.1% results. Figures 1 and 2 show methods for accomodating non-zero source impedance.

Drift Error Minimization

In order to minimize drift error, care in selecting C_F and layout of the printed circuit board are required. The capacitor should be of high quality teflon, polycarbonate, or polystyrene construction. Board layout and clean lines are critical particularly at elevated temperature.

A ground guard (shield) surrounding pin 5 will minimize leakage currents to and from the summing junction, arising from extraneous signals. See AN-63 for detailed recommendations.

Capacitor Selection

The size of the capacitor is determined by the required drift rate usually at the expense of acquisition time.

The drift is dictated by leakage current at pin 5 and is given by:

$$\frac{dv}{dt} = \frac{I_L}{C_F}$$

Where I_L is the leakage current at pin 5 and C_F is the value of the capacitance. The room temperature leakage of the LH0053 is typically 6.0 pA, and a 1000 pF capacitor will yield a drift rate of 6.0 mV per second.

For values of C_F below 1000 pF acquisition for the LH0053 is primarily governed by the slew rate of the input amplifier (20 V/μs) and the setting time of the output amplifier ($\cong$1.0 μs). For values above $C_F = 1000$ pF, acquisition time is given by:

$$t_a = \frac{C_F\,\Delta V}{I_{DSS}} + t_{S2}$$

Where:

C_F = The value of the capacitor

ΔV = The magnitude of the input step, e.g. 20V

I_{DSS} = The ON current of switch Q1 $\cong$ 5.0 mA

t_{S2} = The setting time of output amplifier $\cong$ 1.0 μs

Applications Information (Continued)

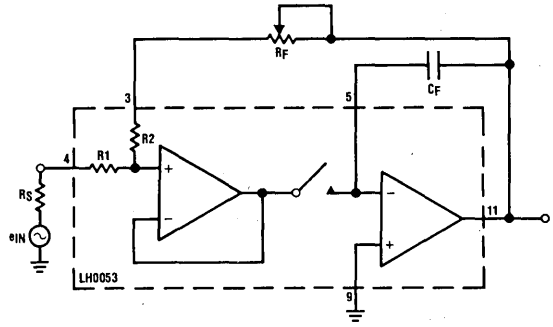


Figure 1. Non-Zero Source Impedance Compensation

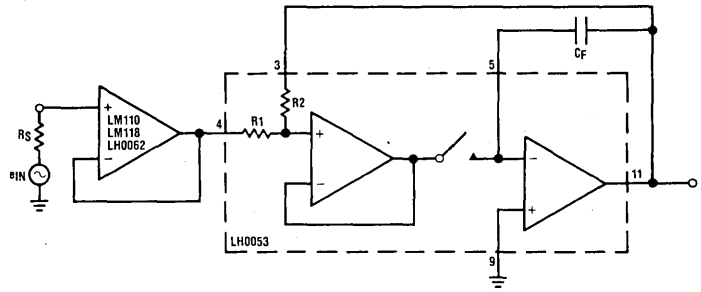


Figure 2. Non-Zero Source Impedance Buffering

Gate Input Considerations

5.0V TTL Applications

The LH0053 Gate input (pin 6) will interface directly with 5.0V TTL. However, TTL gates typically pull up to 2.5V in the logic "1" state. It is therefore advisable to use a 10kΩ pull-up resistor between the 5.0V, V_{CC}, and the output of the gate as shown in Figure 3.

To obtain the highest speed and fastest acquisition time, the gate drive shown in Figure 6 is recommended.

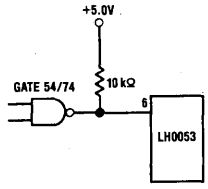


Figure 3. TTL Logic Compatibility

CMOS Applications

The LH0053 gate input may be interfaced directly with 74C, CMOS operating off of V_{CC}'s from 5.0V to 15V. However, transient currents of several milliamps can flow on the rising and falling edges of the input signal. It is, therefore, advisable to parallel the outputs of two 54C/74C gates as shown in Figure 4.

It should be noted that leakage at pin 5 in the hold mode will be increased by a factor of 2 to 3 when operating into 15V logic levels.

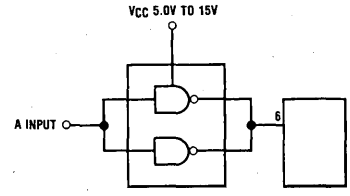


Figure 4. CMOS Logic Compatibility

Heat Sinking

The LH0053 may be operated over the military temperature range, −55°C to +125°C, without incurring damage to the device. However, a clip on heat sink such as the Wakefield 215 Series or Thermalloy 2240 will reduce the internal temperature rise by about 20°C. The result is a two-fold improvement in drift rate at temperature.

Applications Information (Continued)

Since the case of the device is electrically isolated from the circuit, the LH0053 may be mounted directly to a grounded heat sink.

Power Supply Decoupling

Amplifiers A1 and A2 within the LH0053 are very wide band devices and are sensitive to power supply inductance. It is advisable to bypass V^+ (pin 12) and V^- (pin 10) to ground with 0.1μF disc capacitors in order to prevent oscillation. Should this procedure prove inadequate, the disc capacitors should be paralleled with 4.7μF solid tantalum electrolytic capacitors.

DC Offset Adjust

Output offset error may be adjusted to zero using the circuit shown in Figure 5. Offset null should be accomplished in the sample mode ($V_6 \leq 0.5V$) and analog input (pin 4) equal to zero volts.

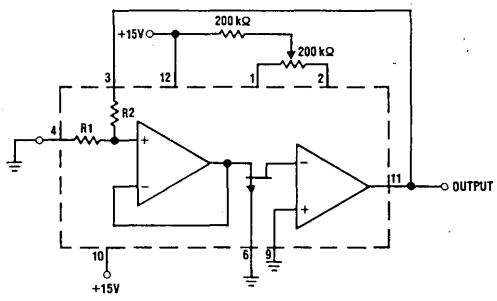


Figure 5. Offset Null Circuit

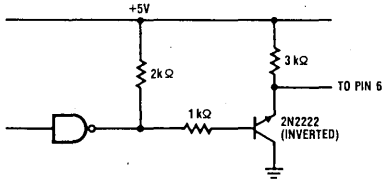


Figure 6. High Speed Gate Drive Circuit

Definition of Terms

Voltage, V_4: The voltage at pin 4, i.e., the analog input voltage.

Voltage, V_6: The voltage at pin 6, i.e., the logic control signal. A logic "1" input, $V_6 \leq 4.5V$, places the LH0053 in the HOLD mode; a logic "0" input ($V_6 \leq 0.5V$) places the device in sample mode.

Acquisition Time: The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to Analog Input 1 (pin 4) with logic input, (pin 6) in the logic "0" state.

Aperture Time: The time indeterminacy when switching from the "sample" mode to the HOLD mode measured from the time the logic input passes through its threshold (2.0V) to the time the device actually enters the HOLD mode.

Sample Accuracy: Difference between input voltage and output voltage while in the sample mode, expressed as a percent of the input voltage.

National Semiconductor

Sample and Hold Amplifiers

LF198/LF298/LF398 Monolithic Sample and Hold Circuits

General Description

The LF198/LF298/LF398 are monolithic sample and hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

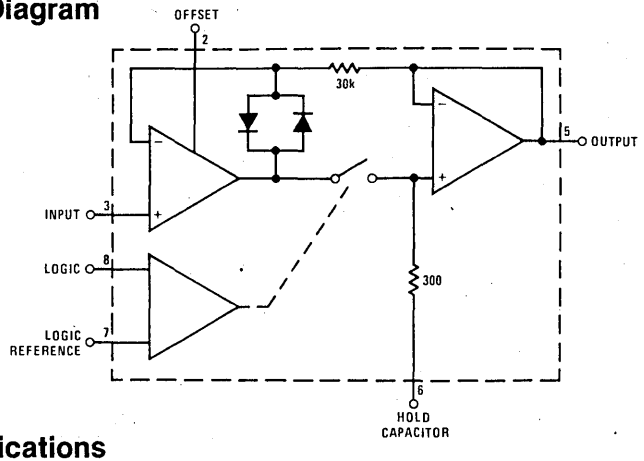
P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

Features

- Operates from ±5V to ±18V supplies
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

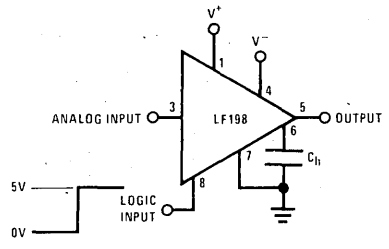
Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package.

Functional Diagram

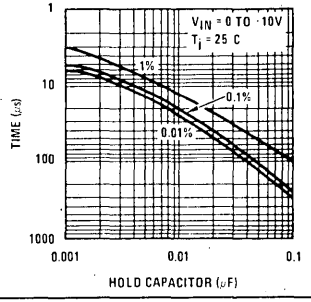


Typical Applications

Typical Connection



Acquisition Time



Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 1)	500 mW
Operating Ambient Temperature Range	
LF198	−55°C to +125°C
LF298	−25°C to +85°C
LF398	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 2)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LF198/LF298			LF398			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage, (Note 6)	$T_j = 25°C$		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 6)	$T_j = 25°C$		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF		4			4		μs
	$C_h = 0.01\mu F$		20			20		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: The maximum junction temperature of the LF198 is 150°C, for the LF298, 115°C, and for the LF398, 100°C. When operating at elevated ambient temperature, the TO-5 package must be derated based on a thermal resistance (Θ_{jA}) of 150°C/W.

Note 2: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 3: Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10\ k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

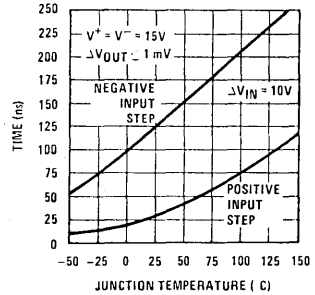
Note 4: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters guaranteed over a supply voltage range of ±5 to ±18V.

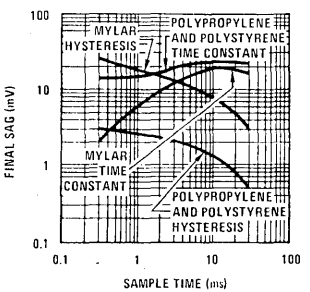
Typical Performance Characteristics

Aperture Time*

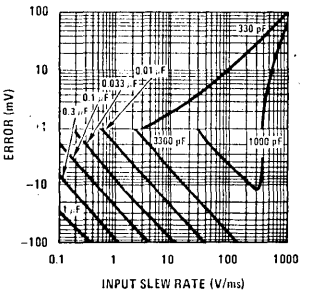


*See definition

Capacitor Hysteresis

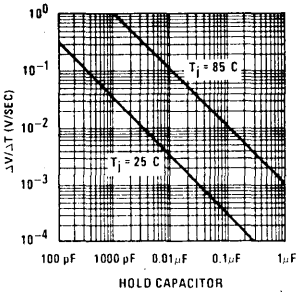


Dynamic Sampling Error

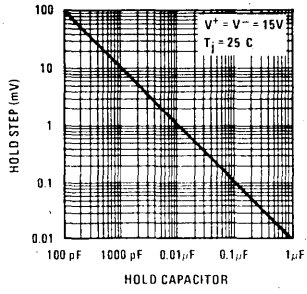


Typical Performance Characteristics (Cont'd)

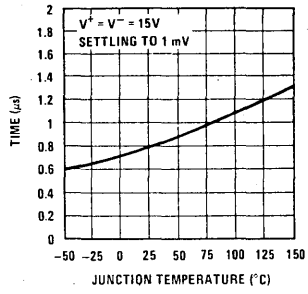
Output Droop Rate



Hold Step

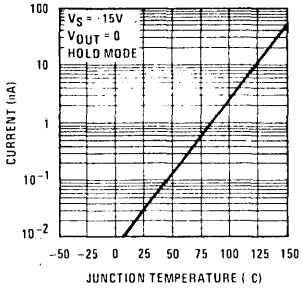


"Hold" Settling Time*

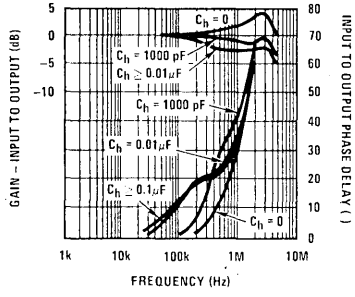


*See definition

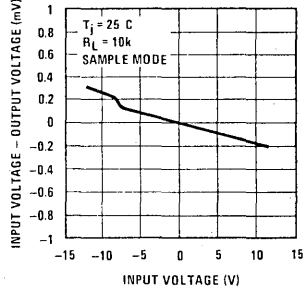
Leakage Current into Hold Capacitor



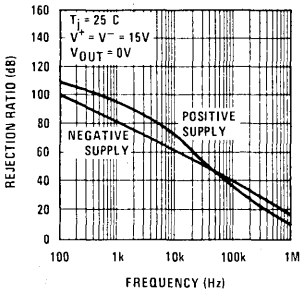
Phase and Gain (Input to Output, Small Signal)



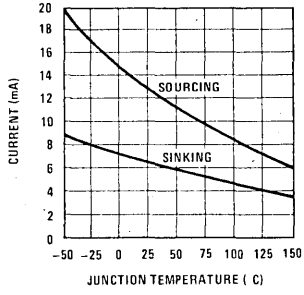
Gain Error



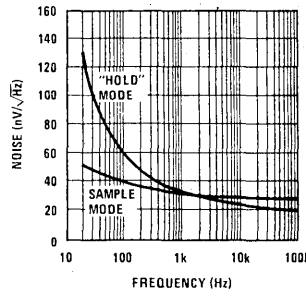
Power Supply Rejection



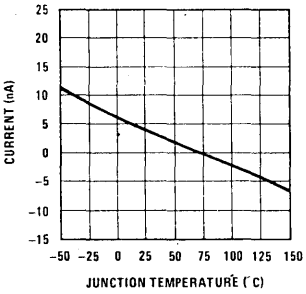
Output Short Circuit Current



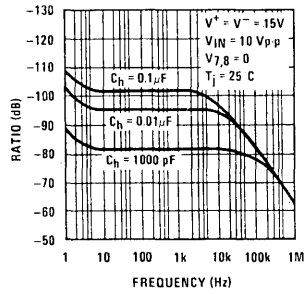
Output Noise



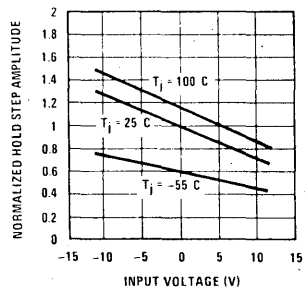
Input Bias Current



Feedthrough Rejection Ratio (Hold Mode)



Hold Step vs Input Voltage



Application Hints

Hold Capacitor

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with $> 1\%$ hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. For more exact data, see the curve labeled dielectric absorption error vs sample time. The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10–50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC and AC Zeroing

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01μF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

Logic Rise Time

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 0.2 V/μs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 0.2 V/μs.

Sampling Dynamic Signals

Sample error due to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/μs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1μs)(0.6V/μs) = 60 mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive-going input would give a ±60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs)(0.6 V/μs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analog) for a total of −36 mV. To add to the confusion, analog delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

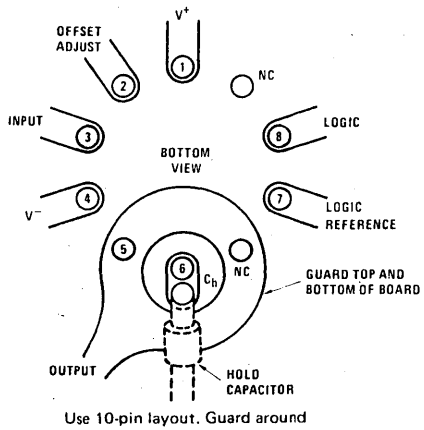
A curve labeled Aperture Time has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1 mV error fed into the output.

A second curve, Hold Settling Time indicates the time required for the output to settle to 1 mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

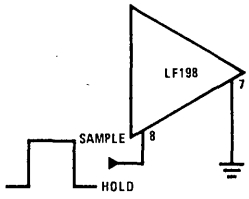
Guarding Technique



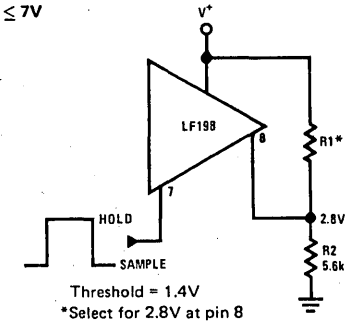
Use 10-pin layout. Guard around C_h is tied to output.

Logic Input Configurations

TTL & CMOS
$3V \leq V_L$ (Hi State) $\leq 7V$

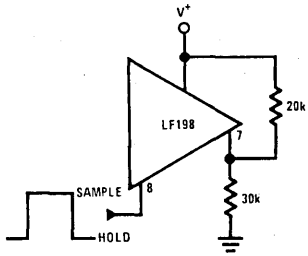


Threshold = 1.4V

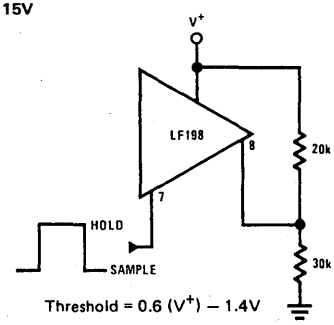


Threshold = 1.4V
*Select for 2.8V at pin 8

CMOS
$7V \leq V_L$ (Hi State) $\leq 15V$

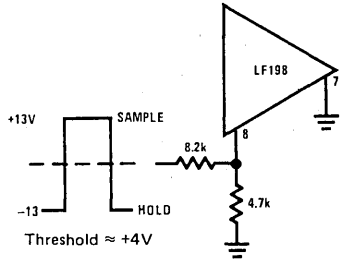


Threshold = 0.6 (V^+) + 1.4V

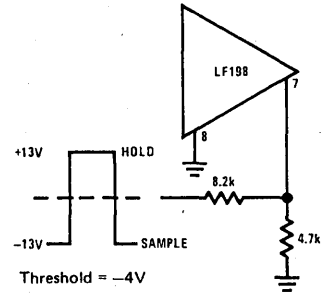


Threshold = 0.6 (V^+) − 1.4V

Op Amp Drive



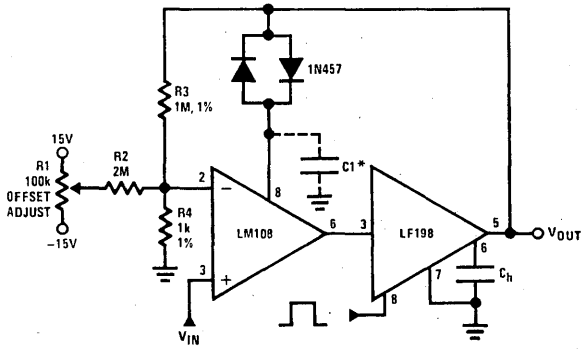
Threshold ≈ +4V



Threshold = −4V

Typical Applications (Cont'd)

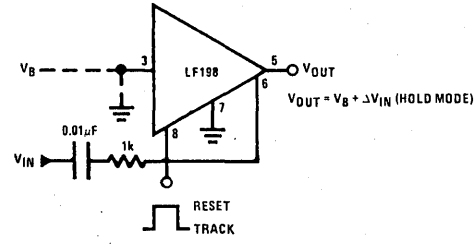
X1000 Sample & Hold



*For lower gains, the LM108 must be frequency compensated

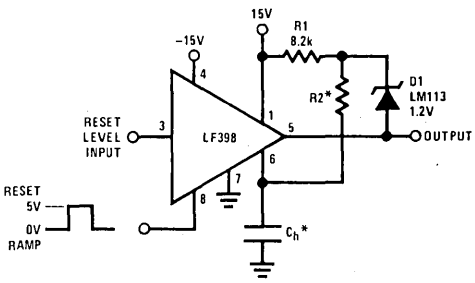
Use $\approx \frac{100}{A_V}$ pF from comp 2 to ground

Sample and Difference Circuit
(Output Follows Input in Hold Mode)



Typical Applications (Cont'd)

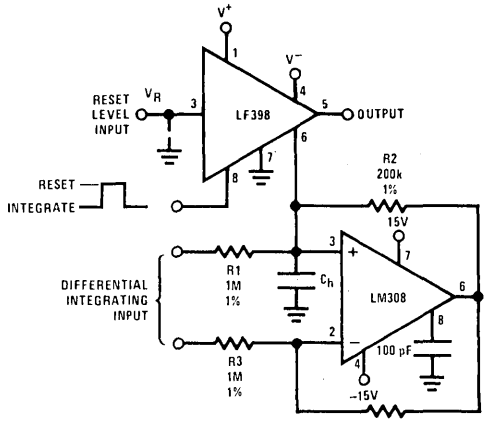
Ramp Generator with Variable Reset Level



*Select for ramp rate $R \geq 10k$

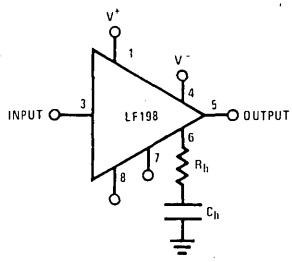
$$\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)(C_h)}$$

Integrator with Programmable Reset Level



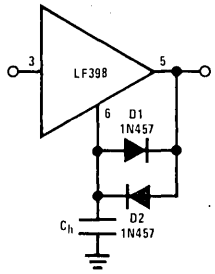
$$V_{OUT}\ (\text{Hold Mode}) = \left[\frac{1}{(R1)(C_h)}\int_0^t V_{IN}\,dt\right] + \left[V_R\right]$$

Output Holds at Average of Sampled Input

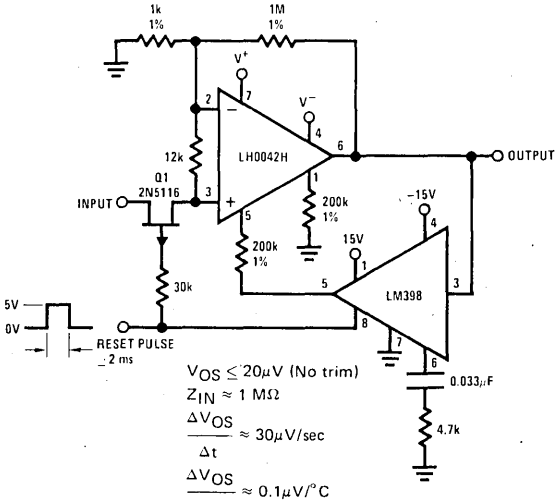


$$\text{Select } (R_h)(C_h) >> \frac{1}{2\pi f_{IN}\ (\text{Min})}$$

Increased Slew Current



Reset Stabilized Amplifier (Gain of 1000)



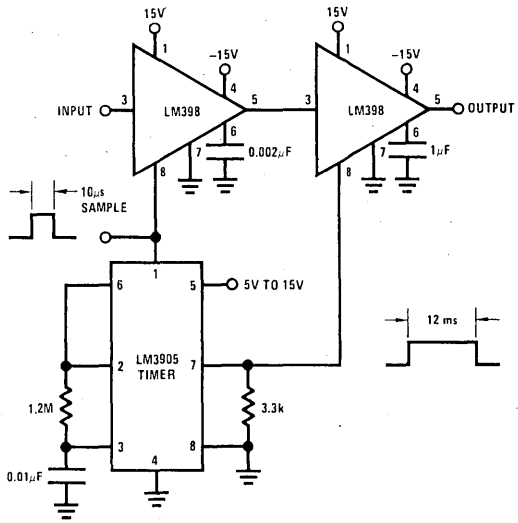
$V_{OS} \leq 20\mu V$ (No trim)

$Z_{IN} \approx 1\ M\Omega$

$$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V/\text{sec}$$

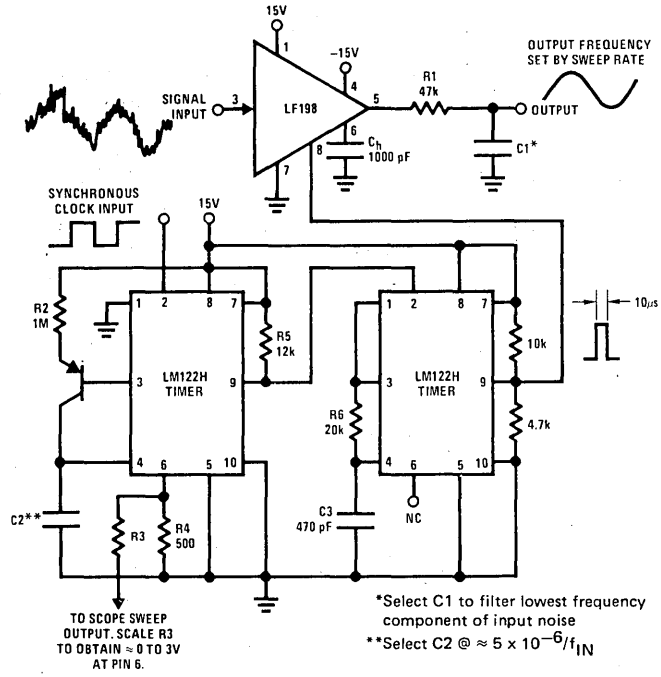
$$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/^\circ C$$

Fast Acquisition, Low Droop Sample & Hold



Typical Applications (Cont'd)

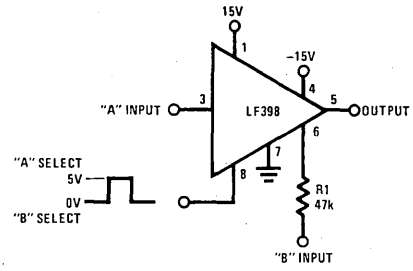
Synchronous Correlator for Recovering Signals Below Noise Level



*Select C1 to filter lowest frequency component of input noise

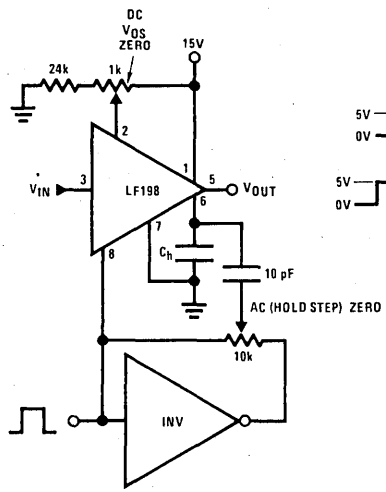
**Select C2 @ $\approx 5 \times 10^{-6}/f_{IN}$

2-Channel Switch

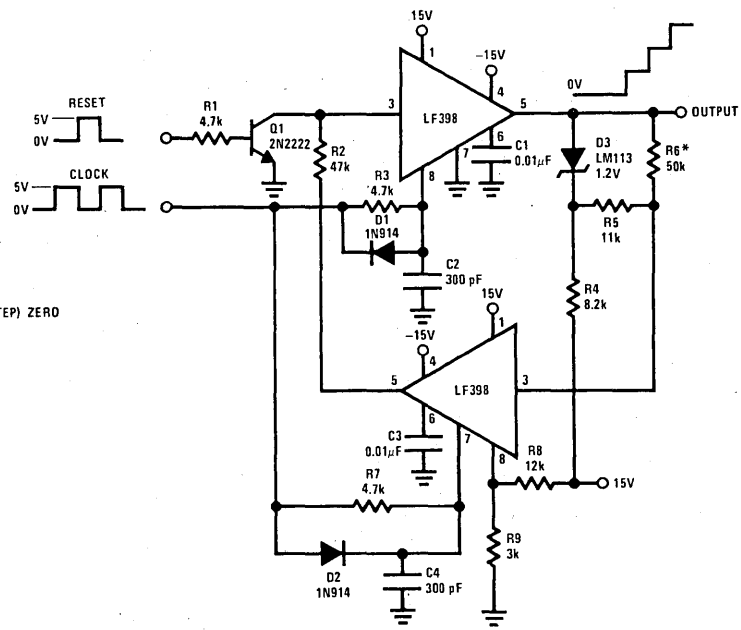


	A	B
Gain	1 ±0.02%	1 ±0.2%
Z_{IN}	$10^{10}\Omega$	47 kΩ
BW	≈1 MHz	≈400 kHz
Crosstalk @ 1 kHz	–90 dB	–90 dB
Offset	≤ 6 mV	≤ 75 mV

DC & AC Zeroing



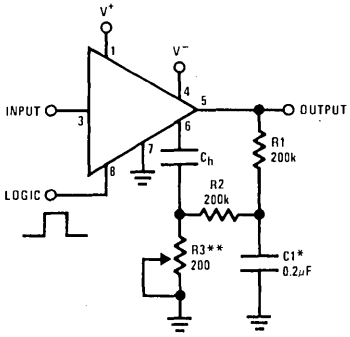
Staircase Generator



*Select for step height
50k → ≈ 1V Step

Typical Applications (Cont'd)

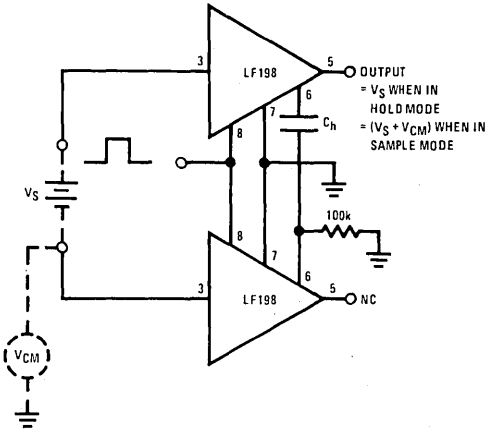
Capacitor Hysteresis Compensation



*Select for time constant C1 = $\frac{\tau}{100k}$

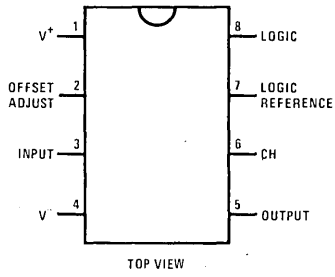
**Adjust for amplitude

Differential Hold



Connection Diagram

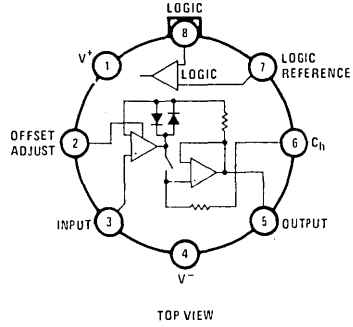
Dual-In-Line Package



Order Number LF198J, LF298J or LF398J
See NS Package J08A

Order Number LF398N
See NS Package N08B

Metal Can Package



Order Number LF198H, LF298H or LF398H
See NS Package H08C

Section 5

Comparators

5

National Semiconductor

LH2111/LH2211/LH2311 Dual Voltage Comparator

General Description

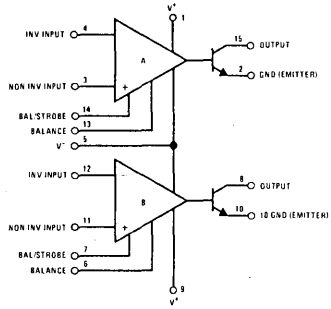
The LH2111 series of dual voltage comparators are two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information see the LM111 data sheet and National's Linear Application Handbook.

The LH2111 is specified for operation over the -55°C to +125°C military temperature range. The LH2211 is specified for operation over the -25°C to +85°C temperature range. The LH2311 is specified for operation over the 0°C to 70°C temperature range.

Features

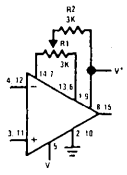
- Wide operating supply range — ±15V to a single +5V
- Low input currents — 6 nA
- High sensitivity — 10 μV
- Wide differential input range — ±30V
- High output drive — 50 mA, 50V

Connection Diagram

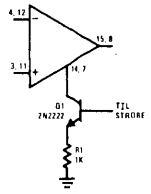


Order Number LH2111D or LH2211D or LH2311D
See Package D16C
LH2111F or LH2211F or LH2311F,
See Package F16B
LH2111J or LH2211J or LH2311J,
See Package J16A

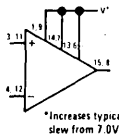
Auxiliary Circuits



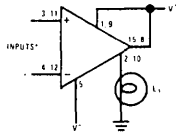
Offset Balancing



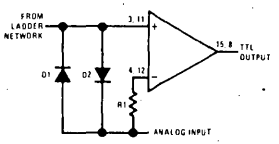
Strobing



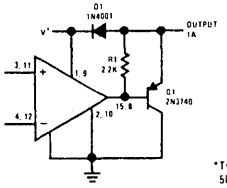
Increasing Input Stage Current*



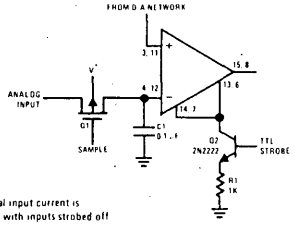
Driving Ground-Referred Load



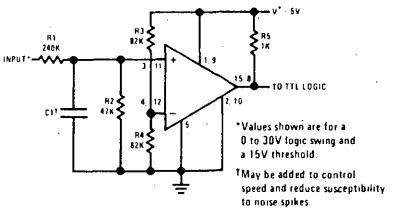
Using Clamp Diodes to Improve Responses



Comparator and Solenoid Driver



Strobing off Both Input* and Output Stages



TTL Interface with High Level Logic

Absolute Maximum Ratings

Total Supply Voltage ($V^+ - V^-$)	36V	Output Short Circuit Duration	10 sec
Output to Negative Supply Voltage ($V_{OUT} - V^-$)	50V	Operating Temperature Range LH2111	-55°C to 125°C
Ground to Negative Supply Voltage (GND - V^-)	30V	LH2211	-25°C to 85°C
Differential Input Voltage	±30V	LH2311	0°C to 70°C
Input Voltage (Note 1)	±15V	Storage Temperature Range	-65°C to 150°C
Power Dissipation (Note 2)	500 mW	Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics Each Side (Note 3)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2111	LH2211	LH2311	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$	3.0	3.0	7.5	mV Max
Input Offset Current (Note 4)	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	100	100	250	nA Max
Voltage Gain	$T_A = 25°C$	200	200	200	V/mV Typ
Response Time (Note 5)	$T_A = 25°C$	200	200	200	ns Typ
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$	1.5	1.5	1.5	V Max
Strobe On Current	$T_A = 25°C$	3.0	3.0	3.0	mA Typ
Output Leakage Current	$V_{IN} > 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$	10	10	50	nA Max
Input Offset Voltage (Note 4)	$R_S \leq 50k$	4.0	4.0	10	mV Max
Input Offset Current (Note 4)		20	20	70	nA Max
Input Bias Current		150	150	300	nA Max
Input Voltage Range		±14	±14	±14	V Typ
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -5$ mV, $I_{SINK} \leq 8$ mA	0.4	0.4	0.4	V Max
Positive Supply Current	$T_A = 25°C$	6.0	6.0	7.5	mA Max
Negative Supply Current	$T_A = 25°C$	5.0	5.0	5.0	mA Max

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature is 150°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2 ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$ for the LH2111, $-25°C \leq T_A \leq 85°C$ for the LH2211, and $0°C \leq T_A \leq 70°C$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. For the LH2311, $V_{IN} = \pm 10$ mV.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Section 6

Non-Linear Functions

Section 6. Non-Linear Functions

Function	Characteristics	Transfer Characteristics	Part Number		Page Number
			−55°C to 125°C	−25°C to 85°C	
True RMS to DC Converter	0.05% accuracy, 100 KHz bandwidth, crest factor 5 minimum	$E_{OUT} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)dt}$	LH0091D	LH0091CD	6-4
Multifunction Converter	0.05% accuracy, device multiplies, divides, square roots, raises to fractional powers	$E_{OUT} = V_Y\left(\frac{V_Z}{V_X}\right)^m$	LH0094D	LH0094CD	6-9

National Semiconductor

LH0091 True RMS to DC Converter

General Description

The LH0091, rms to dc converter, generates a dc output equal to the rms value of any input per the transfer function:

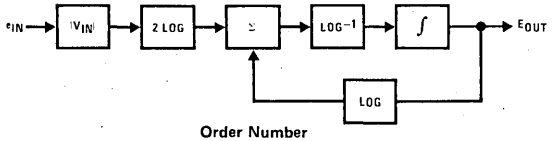
$$E_{OUT(DC)} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2\,(t)\,dt}$$

The device provides rms conversion to an accuracy of 0.1% of reading using the external trim procedure. It is possible to trim for maximum accuracy (0.5 mV ±0.05% typ) for decade ranges i.e., 10 mV → 100 mV, 0.7V → 7V, etc.

Features

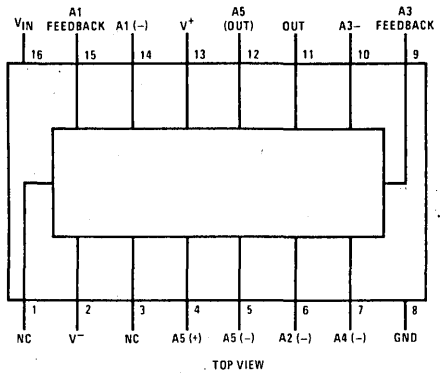
- Low cost
- True rms conversion
- 0.5% of reading accuracy untrimmed
- 0.05% of reading accuracy with external trim
- Minimum component count
- Input voltage to ±15V peak for V_S = ±15V
- Uncommitted amplifier for filtering, gain, or high crest factor configuration
- Military or commercial temperature range.

Block and Connection Diagrams



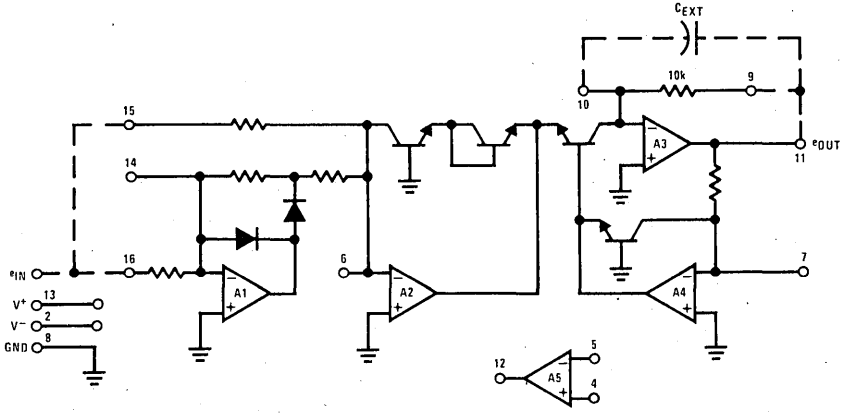
Order Number
LH0091D
LH0091CD
See Package D16D

Dual-In-Line Package



TOP VIEW

Simplified Schematic



Note: Dotted lines denote external connections.

Absolute Maximum Ratings

Supply Voltage		±22V
Input Voltage		±15V peak
Output Short Circuit Duration		Continuous
Operating Temperature Range	T_{MIN}	T_{MAX}
LH0091	−55°C	125°C
LH0091C	−25°C	85°C
Storage Temperature Range		
LH0091		−65°C to +150°C
LH0091C		−25°C to +85°C
Lead Temperature (Soldering, 10 seconds)		300°C

Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise notes

Transfer Function = $E_{O(DC)} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2\,(t)\,dt}$

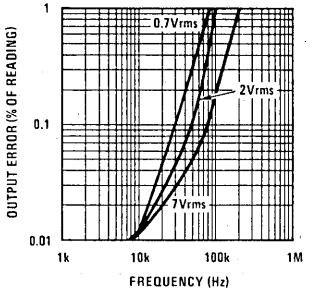
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (See Definition of Terms)					
Total Unadjusted Error	50 mVrms ≤ V_{IN} ≤ 7Vrms *(Figure 1)*		20, ±0.5	40, ±1.0	mV, %
Total Adjusted Error	50 mVrms ≤ V_{IN} ≤ 7Vrms *(Figure 3)*		0.5, ±0.05	1, ±0.2	mV, %
Total Unadjusted Error vs Temperature	−25°C ≤ T_A ≤ +70°C		0.25, ±0.02%		mV, %/°C
Total Unadjusted Error vs Supply Voltage			1		mV/V
AC PERFORMANCE					
Frequency for Specified Adjusted Error	Input = 7Vrms, Sinewave *(Figure 3)*	30	70		kHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		40		kHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		20		kHz
Frequency for 1% Additional Error	Input = 7Vrms, Sinewave *(Figure 3)*	100	200		kHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		75		kHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		50		kHz
Bandwidth (3 dB)	Input = 7Vrms, Sinewave *(Figure 3)*		2		MHz
	Input = 0.7Vrms, Sinewave *(Figure 3)*		1.5		MHz
	Input = 0.1Vrms, Sinewave *(Figure 3)*		0.8		MHz
Crest Factor	Rated Adjusted Accuracy Using the High Crest Factor Circuit *(Figure 5)*	5	10		
INPUT CHARACTERISTICS					
Input Voltage Range	For Rated Performance	±0.05		±11	Vpeak
Input Impedance		4.5	5		kΩ
OUTPUT CHARACTERISTICS					
Rated Output Voltage	$R_L \geq 2.5$ kΩ	10			V
Output Short Circuit Current			22		mA
Output Impedance			1		Ω
POWER SUPPLY REQUIREMENTS					
Operating Range		±5		±20	V
Quiescent Current	V_S = ±15V		14	18	mA

Op Amp Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise notes

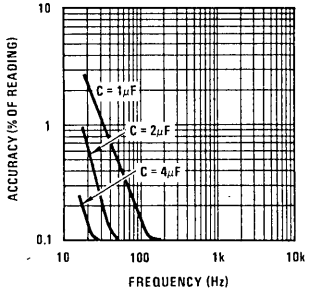
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	10	mV
I_{OS}	Input Offset Current			4.0	200	nA
I_B	Input Bias Current			30	500	nA
R_{IN}	Input Resistance			2.5		MΩ
A_{OL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	15	160		V/mV
V_O	Output Voltage Swing	$R_L = 10\ k\Omega$	±10	±13		V
V_I	Input Voltage Range		±10			V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$		90		dB
PSRR	Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		96		dB
I_{SC}	Output Short-Circuit Current			25		mA
S_r	Slew Rate (Unity Gain)			0.5		V/μs
BW	Small Signal Bandwidth			1.0		MHz

Typical Performance Characteristics

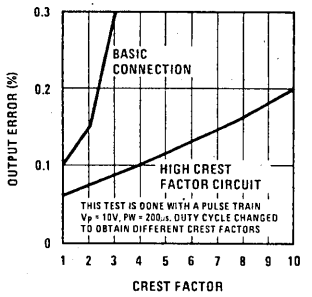
Error vs Frequency



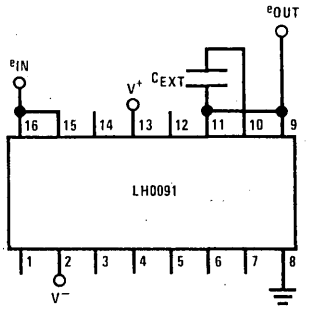
Error vs Frequency



Error vs Crest Factor



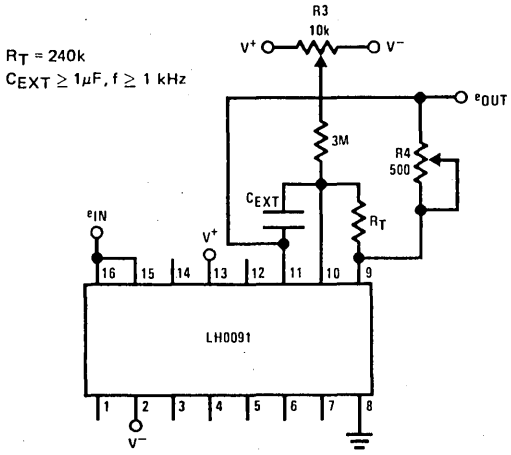
Typical Applications (All applications require power supply by-pass capacitors.)



$C_{EXT} \geq 1\mu F$; frequency ≥ 1 kHz

FIGURE 1. LH0091 Basic Connection (No Trim)

Typical Applications (Cont'd)

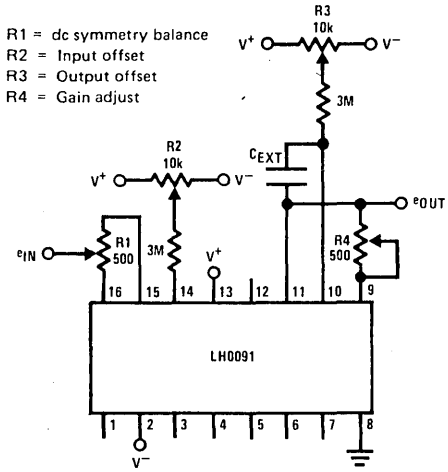


Note. The easy trim procedure is used for ac coupled input signals. It involves two trims and can achieve accuracies of 2 mV offset ±0.1% reading.

Procedure:

1. Apply 100 mV rms (sine wave) to input, adjust R3 until the output reads 100 mV_{DC}.
2. Apply 5 V_{rms} (sine wave) to input, adjust R4 until the output reads 5 V_{DC}.
3. Repeat steps 1 and 2 until the desired initial accuracy is achieved.

FIGURE 2. LH0091 "Easy Trim" (For ac Inputs Only)

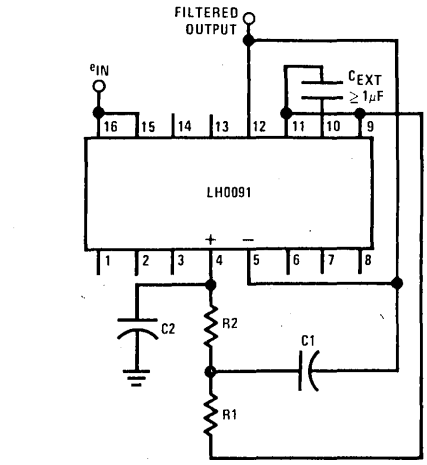


Note. This procedure will give accuracies of 0.5 mV offset ±0.05% reading for inputs from 0.05V peak to 10V peak.

Procedure:

1. Apply 50 mV_{DC} to the input. Read and record the output.
2. Apply −50 mV_{DC} to the input. Use R2 to adjust for an output of the same magnitude as in step 1.
3. Apply 50 mV to the input. Use R3 to adjust the output for 50 mV.
4. Apply −50 mV to input. Use R2 to adjust the output for 50 mV.
5. Apply ±10V alternately to the input. Adjust R1 until the output readings for both polarities are equal (not necessary that they be exactly 10V).
6. Apply 10V to the input. Use R4 to adjust for 10V at the output.
7. Repeat this procedure to obtain the desired accuracy.

FIGURE 3. LH0091 Standard dc Trim Procedure



Note. The additional op amp in the LH0091 may be used as a low pass filter as shown in *Figure 4*.

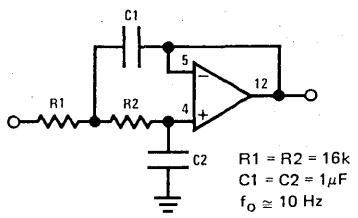
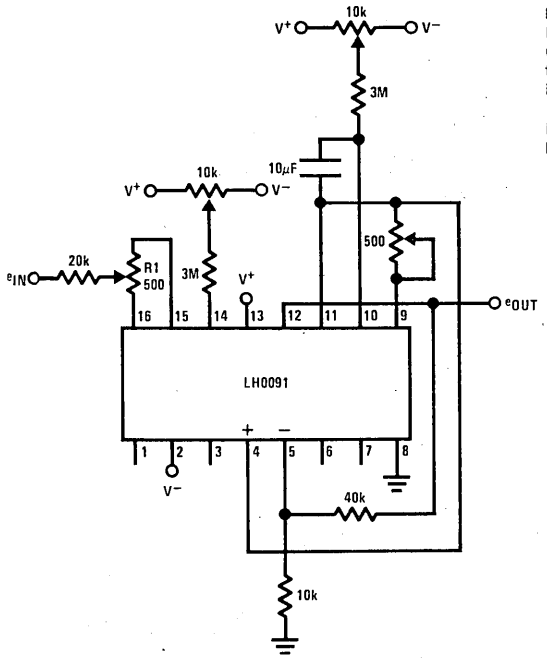


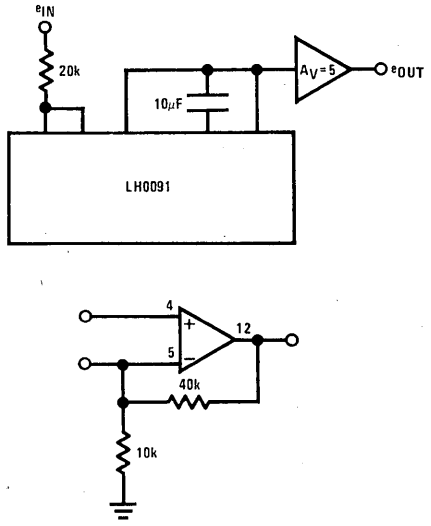
FIGURE 4. Output Filter Connection Using the Internal Op Amp

Typical Applications (Cont'd)



Note. When converting signals with a crest factor ≥ 2, the LH0091 should be connected as shown. Note that this circuit utilizes a 20k resistor to drop the input current by a factor of five. The frequency response will correspond to a voltage which is 1/5 e_{IN}.

Note that the extra op amp in the LH0091 may be used to build a gain of 5 amplifier to restore the output voltage.



Note. Response time of the dc output voltage is dominated by the RC time constant consisting of the total resistance between pins 9 and 10 and the external capacitor, C_{EX}.

FIGURE 5. High Crest Factor Circuit

Definition of Terms

True rms to dc Converter: A device which converts any signal (ac, dc, ac + dc) to the dc equivalent of the rms value.

Error: is the amount by which the actual output differs from the theoretical value. Error is defined as a sum of a fixed term and a percent of reading term. The fixed term remains constant, regardless of input while the percent of reading term varies with the input.

Total Unadjusted Error: The total error of the device without any external adjustments.

Bandwidth: The frequency at which the output dc voltage drops to 0.707 of the dc value at low frequency.

Frequency for Specified Error: The error at low frequency is governed by the size of the external averaging capacitor. At high frequencies, error is dependent on the frequency response of the internal circuitry. The frequency for specified error is the maximum input frequency for which the output will be within the specified error band (i.e., frequency for 1% error means the input frequency must be less than 200 kHz to maintain an output with an error of less than 1% of the initial reading.

Crest Factor: is the peak value of a waveform divided by the rms value of the same waveform. For high crest factor signals, the performance of the LH0091 can be improved by using the high crest factor connection.

National Semiconductor

LH0094 Multifunction Converter

General Description

The LH0094 multifunction converter generates an output voltage per the transfer function:

$$E_O = V_Y \left(\frac{V_Z}{V_X}\right)^m, \quad 0.1 \leq m \leq 10, \text{ m continuously adjustable}$$

m is set by 2 resistors.

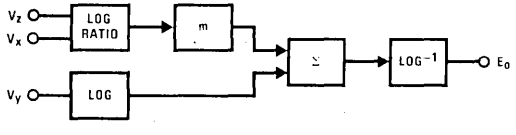
Features

- Low cost
- Versatile
- High accuracy—0.05%
- Wide supply range—±5V to ±22V
- Minimum component count
- Internal matched resistor pair for setting m = 2 and m = 0.5

Applications

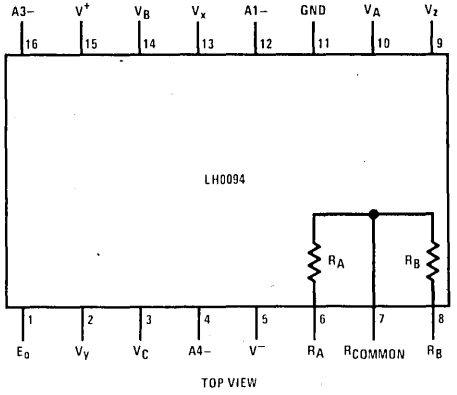
- Precision divider, multiplier
- Square root
- Square
- Trigonometric function generator
- Companding
- Linearization
- Control systems
- Log amp

Block and Connection Diagrams



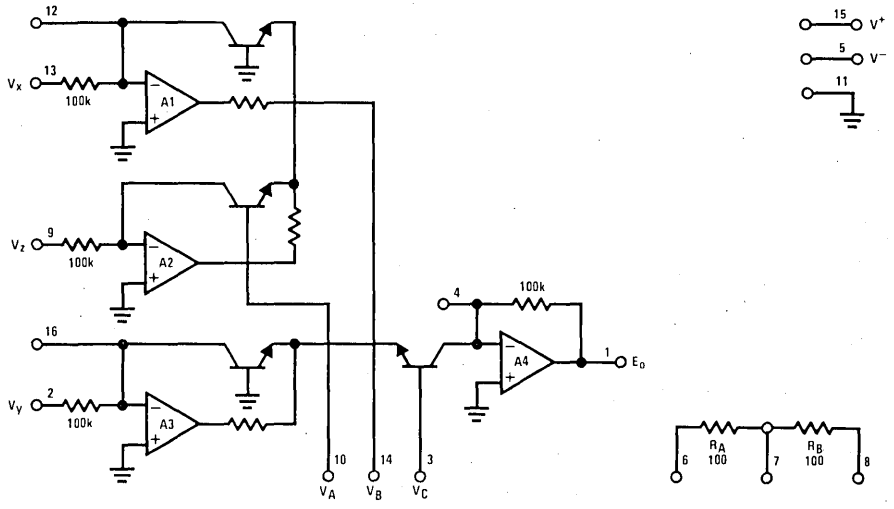
Order Number
LH0094D
LH0094CD
See Package D16D

Dual-In-Line Package



TOP VIEW

Simplified Schematic



Absolute Maximum Ratings

Supply Voltage	±22V
Input Voltage	±22V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LH0094CD	−25°C to +85°C
LH0094D	−55°C to +125°C
Storage Temperature Range	
LH0094D	−65°C to +150°C
LH0094CD	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified. Transfer function: $E_O = V_y \frac{V_z}{V_x}^m$; $0.1 \leq m \leq 10$; $0V \leq V_x, V_y, V_z \leq 10V$

Parameter	Conditions	LH0094			LH0094C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Accuracy								
Multiply	$E_O = \frac{V_z V_y}{10}$ ($0.03 \leq V_y \leq 10V$; $0.01 \leq V_z \leq 10V$)							% F.S.
Untrimmed	(Figure 2)		0.25	0.45		0.45	0.9	(10V)
External Trim	(Figure 3)		0.10			0.1		% F.S.
	vs. Temperature		0.2			0.2		mV/°C
Divide	$E_O = 10V_z/V_x$							
Untrimmed	(Figure 4) $0.5 \leq V_x \leq 10$; $0.01 \leq V_z \leq 10$)		0.25	0.45		0.45	0.9	% F.S.
External Trim	(Figure 5), ($0.1 \leq V_x \leq 10$; $0.01 \leq V_z \leq 10$)		0.10			0.1		% F.S.
	vs. Temperature		0.2			0.2		mV/°C
Square Root	$E_O = 10\sqrt{V_z/10}$							
Untrimmed	(Figure 8), ($0.03 \leq V_z \leq 10$		0.25	0.45		0.45	0.9	% F.S.
External Trim	(Figure 9), ($0.01 \leq V_z \leq 10$		0.15			0.15		% F.S.
Square	$E_O = 10\,(V_z/10)^2$ ($0.1 \leq V_z \leq 10$)							
Untrimmed	(Figure 6)	0.5	1.0		1.0	2.0	% F.S.	
External Trim	(Figure 7)	0.15			0.15		% F.S.	
Low Level Square Root	$E_O = \sqrt{10V_z}$; 5.0mV ≤ $V_z \leq 10V$ (Figure 10)		0.05			0.05		% F.S.
Exponential	$m = 0.2$, $E_O = 10\,(V_z/10)^2$ (Figure 11), ($0.1 \leq V_z \leq 10$)		0.05			0.08		% F.S.
Circuits	$m = 5.0$, $E_O = 10\,(V_z/10)^5$ (Figure 11), ($1.0 \leq V_z \leq 10$)		0.05			0.08		% F.S.
Output Offset								
	$V_x = 10V$, $V_y = V_z = 0$		2.0	5.0		5.0	10	mV
AC Characteristics								
3dB Bandwidth	$m = 1.0$, $V_x = 10V$, $V_y = 0.1V_{rms}$		10			10		kHz
Noise	10Hz to 1.0kHz, $m = 1.0$, $V_y = V_z = 0V$							
	$V_x = 10V$		100			100		μV/rms
	$V_x = 0.1V$		300			300		μV/rms
Exponents								
m		0.2 to 5.0	0.1 to 10		0.2 to 5.0	0.1 to 10		
Input Characteristics								
Input Voltage	(For Rated Performance)	0		10	0		10	V
Input Impedance	(All Inputs)	98	100		98	100		kΩ
Output Characteristics								
Output Swing	($R_L \leq 10k$)	10	12		10	12		V
Output Impedance			1.0			1.0		Ω
Supply Current	($V_S = \pm 15V$), Note 1		3.0	5.0		3.0	5.0	mA

Applications Information

GENERAL INFORMATION

Power supply bypass capacitors (0.1 μF) are recommended for all applications.

The LH0094 series is designed for positive input signals only. However, negative input up to the supply voltage will not damage the device.

A clamp diode *(Figure 1)* is recommended for those applications in which the inputs may be subjected to open circuit or negative input signals.

For basic applications (multiply, divide, square, square root) it is possible to use the device without any external adjustments or components. Two matched resistors are provided internally to set m for square or square root.

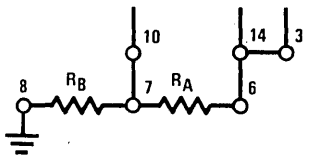
When using external resistors to set m, such resistors should be as close to the device as possible.

SELECTION OF RESISTORS TO SET m

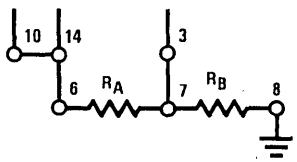
Internal Matched Resistors

R_A and R_B are matched internal resistors. They are 100Ω ±10%, but matched to 0.1%.

(a) m = 2*



(b) m = 0.5*

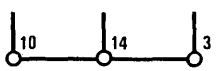


*No external resistors required, strap as indicated

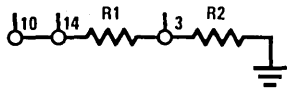
External Resistors

The exponent is set by 2 external resistors or it may be continuously varied by a single trim pot. (R1 + R2 ≤ 500Ω.

(a) m = 1

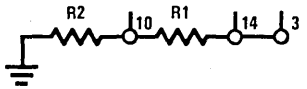


(b) m < 1



$$m = \frac{R2}{R1 + R2} \qquad R1 + R2 \approx 200\Omega$$

(c) m > 1



$$m = \frac{R1 + R2}{R2}$$

ACCURACY (ERROR)

The accuracy of the LH0094 is specified for both externally adjusted and unadjusted cases.

Although it is customary to specify the errors in percent of full-scale (10V), it is seen from the typical performance curves that the actual errors are in percent of reading. Thus, the specified errors are overly conservative for small input voltages. An example of this is the LH0094 used in the multiplication mode. The specified typical error is 0.25% of full-scale (25 mV). As seen from the curve, the unadjusted error is ≈ 25 mV at 10V input, but the error is less than 10 mV for inputs up to 1V. Note also that if either the multiplicand or the multiplier is at less than 10V, (5V for example) the unadjusted error is less. Thus, the errors specified are at full-scale—the worst case.

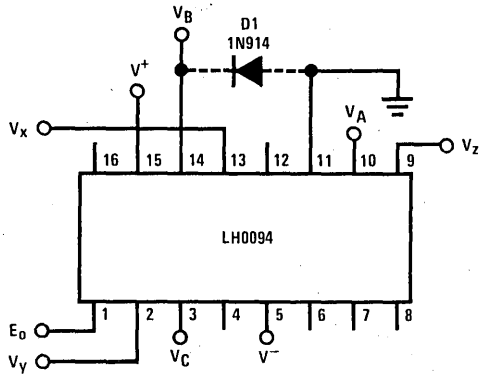
The LH0094 is designed such that the user is able to externally adjust the gain and offset of the device—thus trim out all of the errors of conversion. In most applications, the gain adjustment is the only external trim needed for super accuracy—except in division mode, where a denominator offset adjust is needed for small denominator voltages.

EXPONENTS

The LH0094 is capable of performing roots to 0.1 and powers up to 10. However, care should be taken when applying these exponents—otherwise, results may be misinterpreted. For example, consider the 1/10th power of a number: i.e., 0.001 raised to 0.1 power is 0.5011; 0.1 raised to the 0.1 power is 0.7943; and 10 raised to the 0.1 power is 1.2589. Thus, it is seen that while the input has changed 4 decades, the output has only changed a little more than a factor of 2. It is also seen that with as little as 1 mV of offset, the output will also be greater than zero with zero input.

Applications Information (Continued)

1. CLAMP DIODE CONNECTION



$$E_o = V_y \left(\frac{V_z}{V_x}\right)^m$$

$0.1 \leq m \leq 10$

Note. This clamp diode connection is recommended for those applications in which the inputs may be subject to open circuit or negative signals.

FIGURE 1. Clamp Diode Connection

2. MULTIPLY

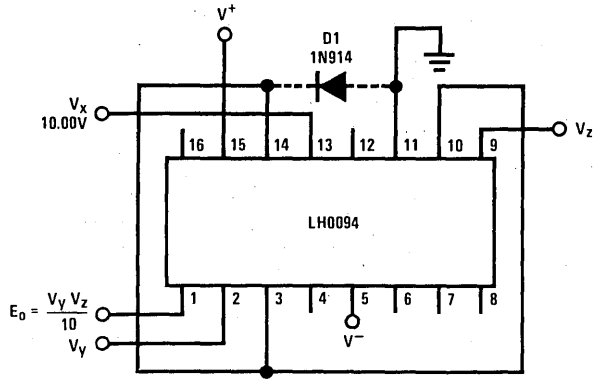


FIGURE 2a. LH0094 Used to Multiply (No External Adjustment)

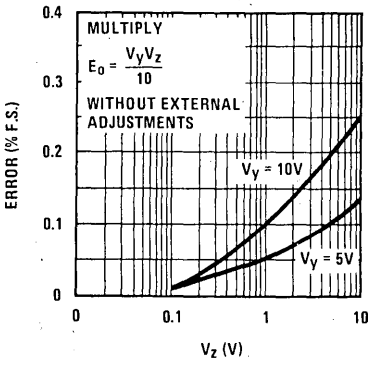


FIGURE 2b. Typical Performance of LH0094 in Multiply Mode Without External Adjustment

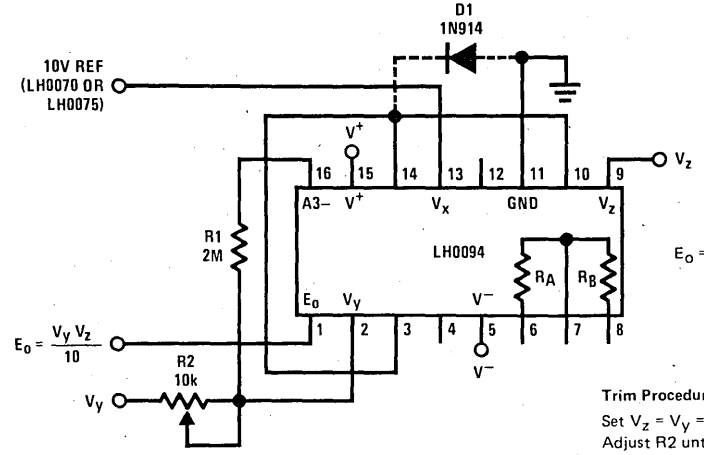


FIGURE 3. Precision Multiplier (0.02% Typ) with 1 External Adjustment

Applications Information (Continued)

3. DIVIDE

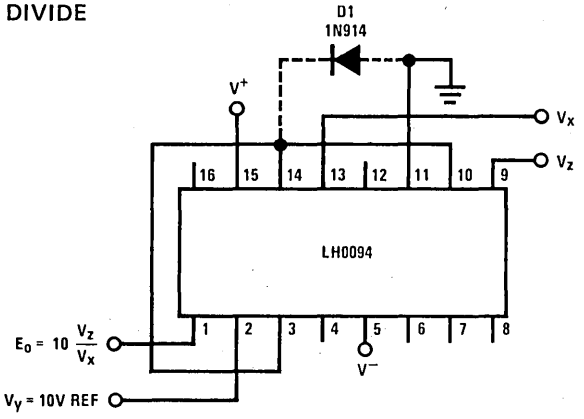


FIGURE 4a. LH0094 Used to Divide (No External Adjustment)

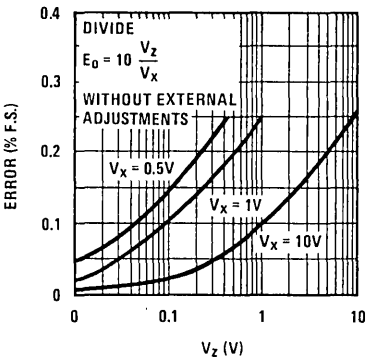


FIGURE 4b. Typical Performance, Divide Mode, Without External Adjustments

Trim Procedures

Apply 10V to V_Y, 0.1V to V_X and V_Z.
Adjust R3 until E_O = 10.000V.

Apply 10.000V to all inputs.
Adjust R2 until E_O = 10.000V

Repeat procedure.

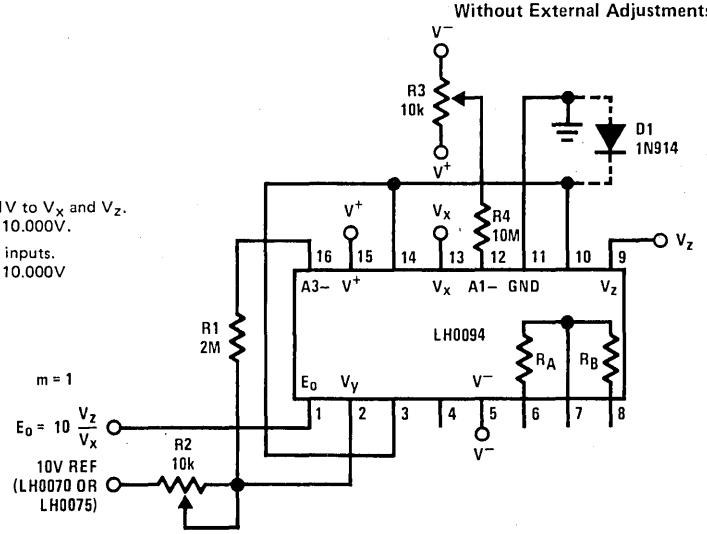


FIGURE 5. Precision Divider (0.05% Typ)

4. SQUARE

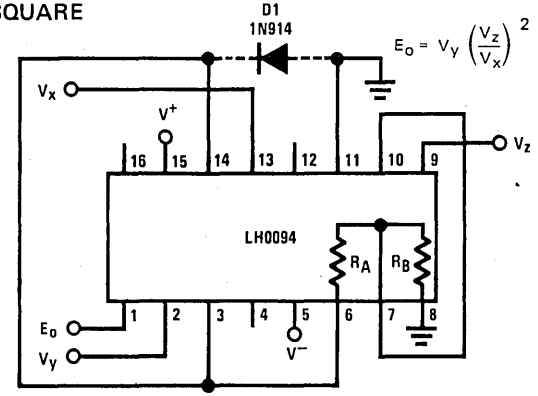


FIGURE 6a. Basic Connection of LH0094 (m = 2) without External Adjustment Using Internal Resistors to Set m

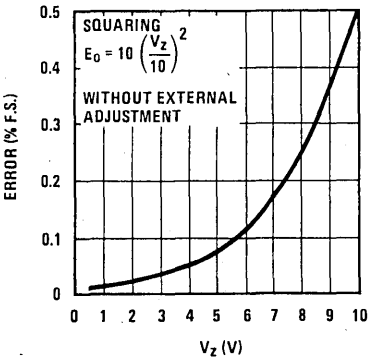


FIGURE 6b. Squaring Mode without External Adjustment

Applications Information (Continued)

4. SQUARE (Continued)

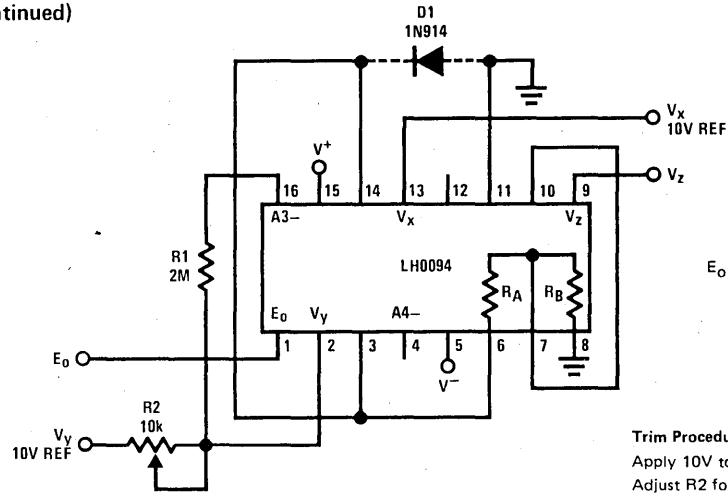


FIGURE 7. Precision Squaring Circuit (0.15% Typ)

5. SQUARE ROOT

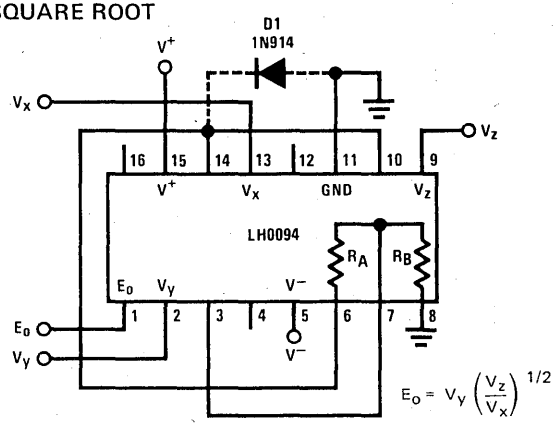


FIGURE 8a. Basic Connection of LH0094 (m = 0.5) without External Adjustment Using Internal Resistors to Set m

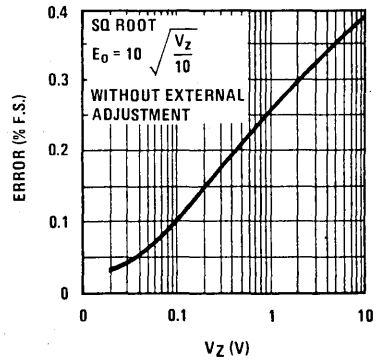


FIGURE 8b. Typical Performance Curve Square Root, No External Adjustment

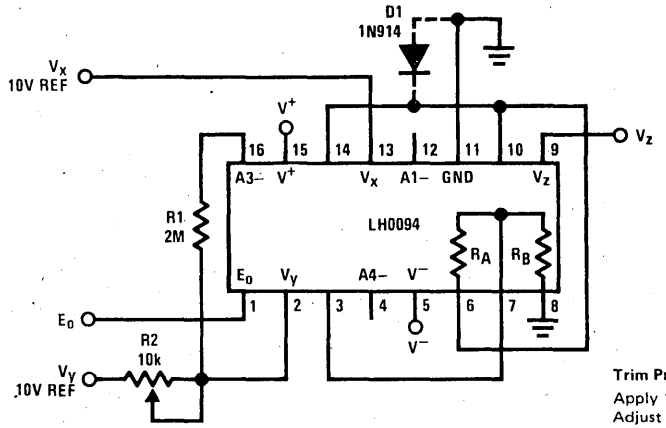


FIGURE 9. Precision Square Rooter (0.15% Typ)

Applications Information (Continued)

6. LOW LEVEL SQUARE ROOT

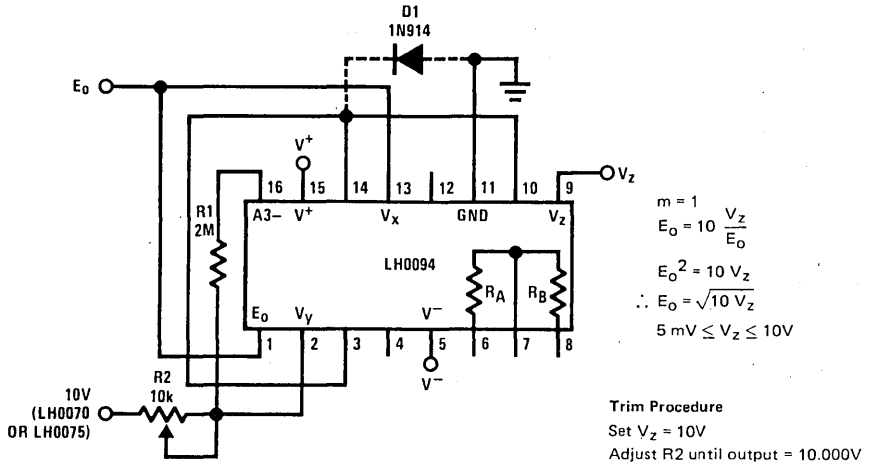


FIGURE 10. 3-Decade Precision Square Root Circuit Using the LH0094 with m = 1

Typical Applications

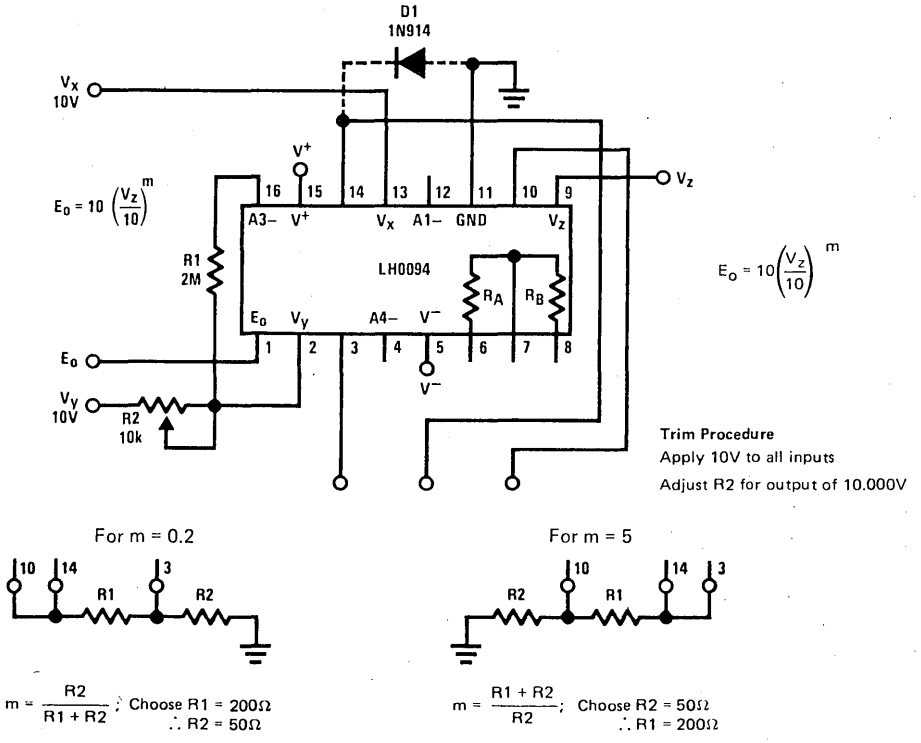
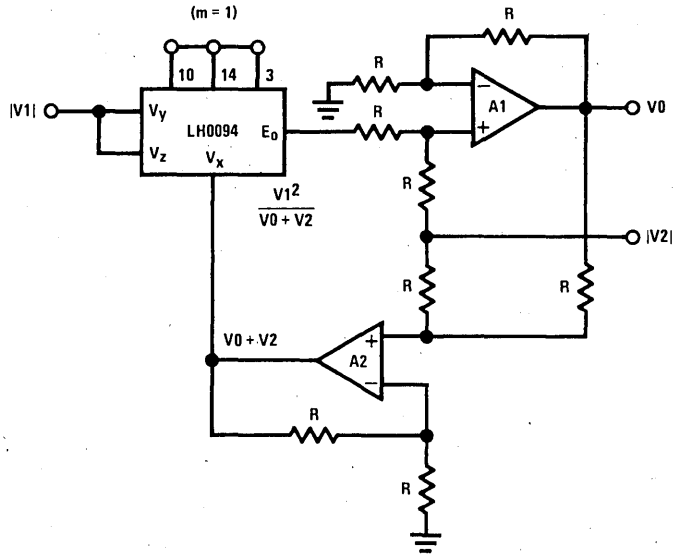


FIGURE 11. Precision Exponentiator (m = 0.2 to 5)

Typical Applications (Continued)



Note. The LH0094 may be used to generate a voltage equivalent to:

$$V0 = \sqrt{V1^2 + V2^2}$$

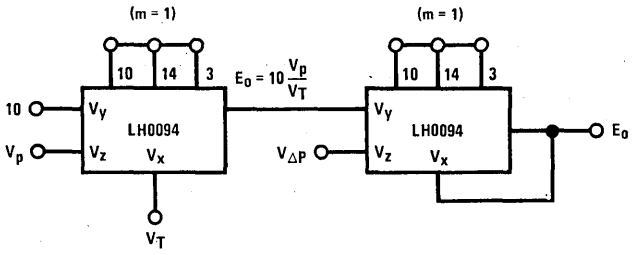
$$V0 = V2 + \frac{V1^2}{V0 + V2}$$

$$V0^2 + V0\,V2 = V2\,V0 + V2^2 + V1^2$$
$$V0^2 = V1^2 + V2^2$$

$$\therefore\ V0 = \sqrt{V1^2 + V2^2} \qquad V1, V2\ 0 \rightarrow 10V$$

$R \approx 10k$
National Semiconductor resistor array RA08–10k is recommended

FIGURE 12. Vector Magnitude Function



Note. The LH0094 may be used in direct measurement of gas flow.

$$\text{Flow} = k\sqrt{\frac{P\Delta P}{T}}$$

$$E_o = 10\,\frac{V_P}{V_T} \times \frac{V_{\Delta P}}{E_o}$$

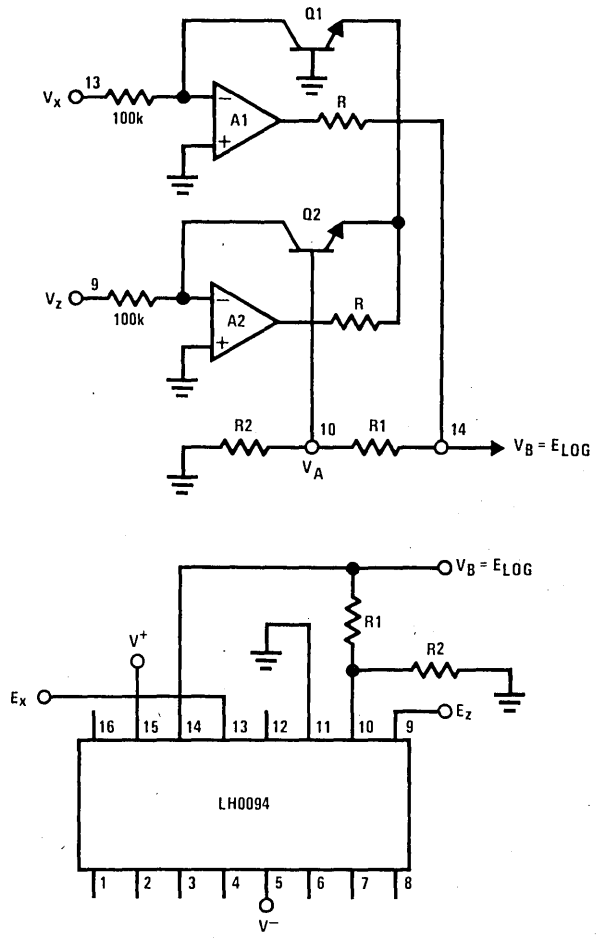
$$E_o^2 = 10\,\frac{V_P\,V_{\Delta P}}{V_T}$$

$$E_o = \sqrt{10\,\frac{V_P\,V_{\Delta P}}{V_T}}$$

P = Absolute pressure
T = Absolute temperature
ΔP = Pressure drop

FIGURE 13. Mass Gas Flow Circuit

Typical Applications (Continued)



Note. The LH0094 may also be used to generate the Log of a ratio of 2 voltages. The output is taken from pin 14 of the LH0094 for the Log application.

$$E_{LOG} = K1 \frac{KT}{q} \ln \frac{V_z}{V_x}$$

where $K1 = \frac{R1 + R2}{R2}$

If $K1 = \frac{1}{KT/q \ln 10}$

then $E_{LOG} = \text{Log}_{10} \frac{V_z}{V_x}$

$R1 = 15.9\ R2$
$R2 \approx 400\Omega$

R2 must be a thermistor with a tempco of $\approx$ 0.33%/°C to be compensated over temperature.

FIGURE 14. Log Amp Application

Section 7

Precision Voltage Regulators and References

Section 7. Precision References and Regulators

Function	Features	Line Reg.	Load Reg.	I_{OUT} (mA)	V_{OUT} Toler. @25°C (Max.)	Drift (Max.)	Part Number −55°C to 125°C	Part Number −25°C to 85°C	Page Number
Positive Programmable Voltage Regulator	Internal programming resistors, adustable current limit V_{OUT} = 5, 6, 8, 10, 12, 15, 18V	0.008%	0.055%	0.1-200	0.5% 1.0%		LH0075	LH0075C	7-8
Negative Programmable Voltage Regulator					0.5% 1.0%		LH0076	LH0076C	7-13
10.000V Precision BCD Reference	Three-terminal buffered zener reference, 0.1Ω output 12.5 to 40V input, 20μV p − p noise	0.02% 0.02% 0.02%	0.01% 0.02% 0.02%	0-5	0.1% 0.1% 0.05%	20mV* 10mV 4.0mV	LH0070-0 LH0070-1 LH0070-2		7-4
10.024V Precision Binary Reference		0.02% 0.02% 0.02%	0.01% 0.02% 0.02%	0-5	0.1% 0.1% 0.05%	20mV* 10mV 4.0mV	LH0071-0 LH0071-1 LH0071-2		7-4
6.95V Temperature Stabilized Reference	Thermostated two-terminal zener, 0.5Ω low noise		0.1%	0.5-10	+1.0% −2.0%	15mV 1.0mV	LM199A	LM299A	7-23
6.9V Reference	Low noise subsurface zener 0.8Ω			6-15	5.0%	7.0 to 35mV	LM129		7-18
Switching Regulator 100kHz Rate 10-35V Input	5A output at 75% efficiency V_{OUT} = 3.0 to 30V	0.05%		5A			LH1605	LH1605C	7-35

*These specifications apply for −25°C to +85°C.

Note: Refer to the *Linear Databook* for information on other regulators and references.

National Semiconductor

LH0070 Series Precision BCD Buffered Reference
LH0071 Series Precision Binary Buffered Reference

General Description

The LH0070 and LH0071 are precision, three terminal, voltage references consisting of a temperature compensated zener diode driven by a current regulator and a buffer amplifier. The devices provide an accurate reference that is virtually independent of input voltage, load current, temperature and time. The LH0070 has a 10.000V nominal output to provide equal step sizes in BCD applications. The LH0071 has a 10.240V nominal output to provide equal step sizes in binary applications.

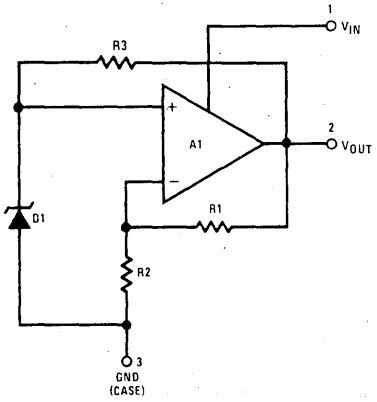
The output voltage is established by trimming ultra-stable, low temperature drift, thin film resistors under actual operating circuit conditions. The devices are short-circuit proof in both the current sourcing and sinking directions.

The LH0070 and LH0071 series combine excellent long term stability, ease of application, and low cost, making them ideal choices as reference voltages in precision D to A and A to D systems.

Features

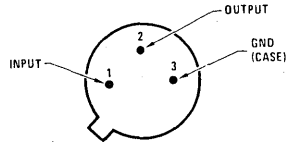
- Accurate output voltage
  - LH0070 — 10V ±0.02%
  - LH0071 — 10.24V ±0.02%
- Single supply operation — 11.4V to 40V
- Low output impedance — 0.2Ω
- Excellent line regulation — 0.1 mV/V
- Low zener noise — 20 μVp-p
- 3-lead TO-5 (pin compatible with the LM109)
- Short circuit proof
- Low standby current — 3 mA

Equivalent Schematic



Connection Diagram

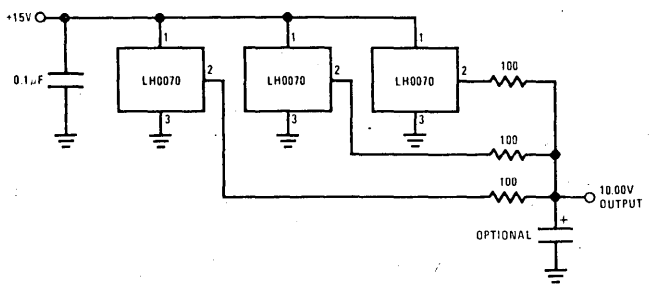
TO-5 Metal Can Package



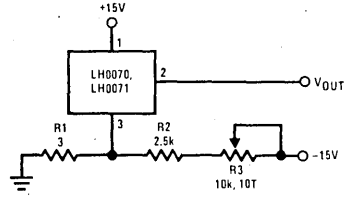
BOTTOM VIEW

Order Number LH0070-0H, LH0071-0H, LH0070-1H, LH0071-1H, LH0070-2H or LH0071-2H
See NS Package H03B

Typical Applications



Statistical Voltage Standard



*Note. The output of the LH0070 and LH0071 may be adjusted to a precise voltage by using the above circuit since the supply current of the devices is relatively small and constant with temperature and input voltage. For the circuit shown, supply sensitivities are degraded slightly to 0.01%/V change in V_{OUT} for changes in V_{IN} and V^-

An additional temperature drift of 0.0001%/°C is added due to the variation of supply current with temperature of the LH0070 and LH0071. Sensitivity to the value of R1, R2 and R3 is less than 0.001%/%.

*Output Voltage Fine Adjustment

Absolute Maximum Ratings

Supply Voltage	40V
Power Dissipation (See Curve)	600 mW
Short Circuit Duration	Continuous
Output Current	±20 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_A = 25°C$				
LH0070			10.000		V
LH0071			10.240		V
Output Accuracy	$T_A = 25°C$				
−0, −1			±0.03	±0.1	%
−2			±0.02	±0.05	%
Output Accuracy	T_A = -55°C, 125°C				
−0, −1				±0.3	%
−2				±0.2	%
Output Voltage Change With Temperature	(Note 2)				
−0				± 0.2	%
−1			±0.02	± 0.1	%
−2			±0.01	±0.04	%
Line Regulation	$13V \leq V_{IN} \leq 33V$, $T_C = 25°C$				
−0, −1			0.02	0.1	%
−2			0.01	0.03	%
Input Voltage Range		11.4		40	V
Load Regulation	$0\ mA \leq I_{OUT} \leq 5\ mA$		0.01	0.03	%
Quiescent Current	$13V \leq V_{IN} \leq 33V$, $I_{OUT} = 0\ mA$	1	3	5	mA
Change In Quiescent Current	ΔV_{IN} = 20V From 13V To 33V		0.75	1.5	mA
Output Noise Voltage	BW = 0.1 Hz To 10 Hz, $T_A = 25°C$		20		μVp-p
Ripple Rejection	f = 120 Hz		0.01		%/Vp-p
Output Resistance			0.2	0.6	Ω
Long Term Stability	$T_A = 25°C$, (Note 3)				
−0, −1				±0.2	%/yr.
−2				±0.05	%/yr.

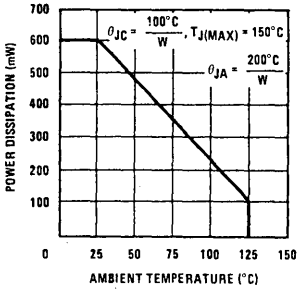
Note 1: Unless otherwise specified, these specifications apply for V_{IN} = 15.0V, R_L = 10 kΩ, and over the temperature range of $-55°C \leq T_A \leq +125°C$.

Note 2: This specification is the difference in output voltage measured at $T_A = 85°C$ and $T_A = 25°C$ or $T_A = 25°C$ and $T_A = -25°C$ with readings taken after test chamber and device-under-test stabilization at temperature using a suitable precision voltmeter.

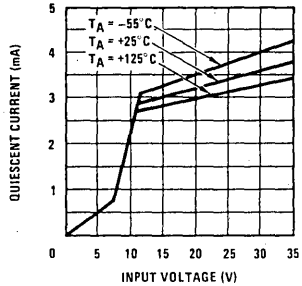
Note 3: This parameter is guaranteed by design and not tested.

Typical Performance Characteristics

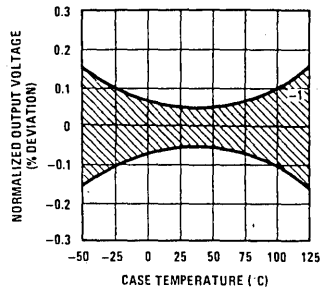
Maximum Power Dissipation



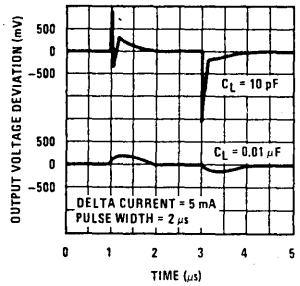
Quiescent Current vs Input Voltage



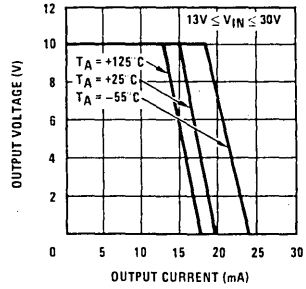
Normalized Output Voltage vs Temperature



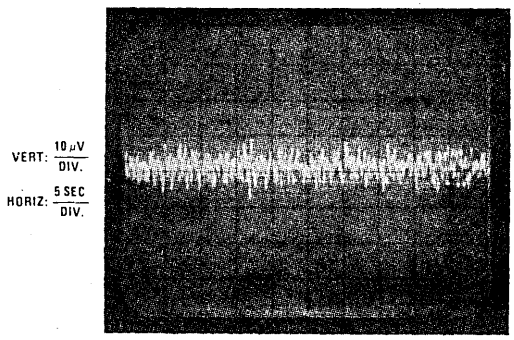
Step Load Response



Output Short Circuit Characteristics

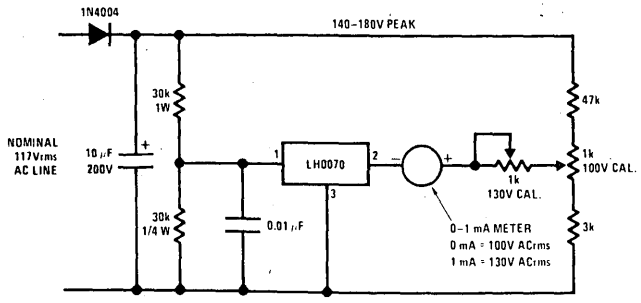


Noise Voltage



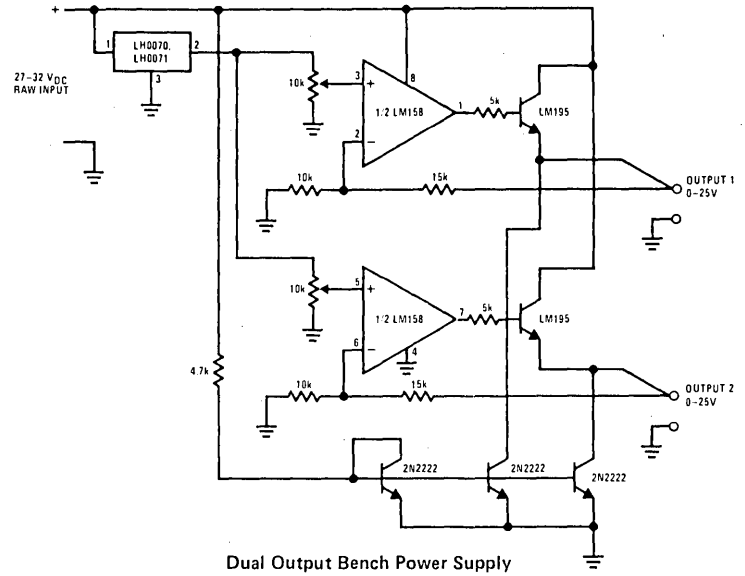
BW = 0.1 Hz TO 10 Hz

Typical Applications (Continued)

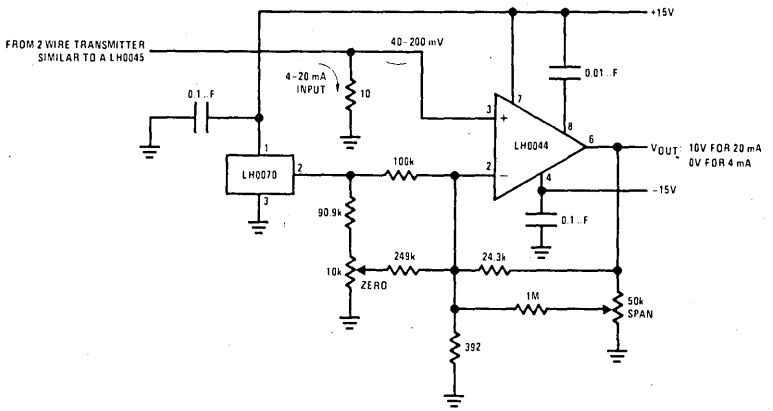


Expanded Scale AC Voltmeter

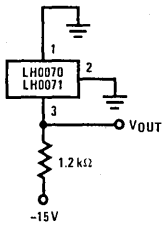
Typical Applications (Continued)



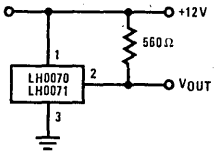
Dual Output Bench Power Supply



Precision Process Control Interface



Negative 10V Reference



Boosted Reference For
Low Input Voltages

National Semiconductor

Voltage References and Regulators

LH0075 Positive Precision Programmable Regulator

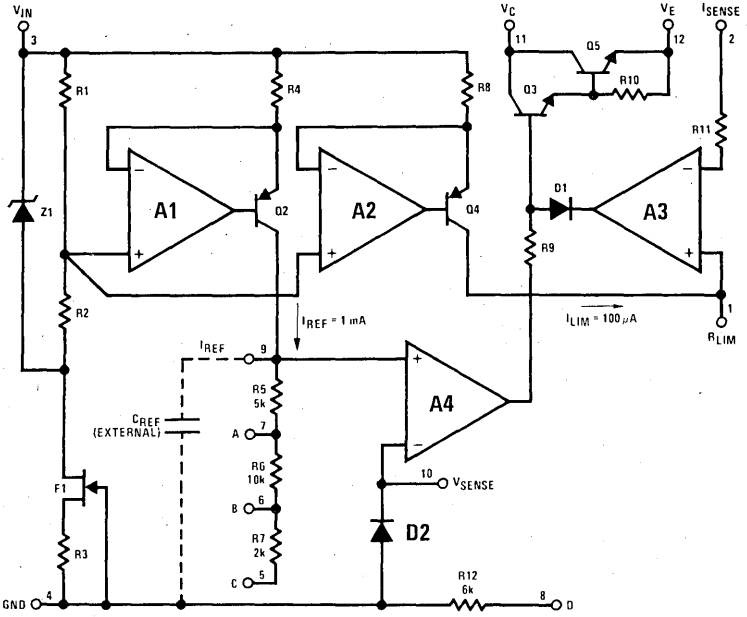
General Description

The LH0075 is a precision programmable regulator for positive voltages. Regulated output voltages from 0 to 27V may be obtained using one external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (5V, 6V, 10V, 12V and 15V). The output current limit is adjustable from 0 to 200 mA using two external resistors. These features provide an inventory of precision regulated values in one package.

Features

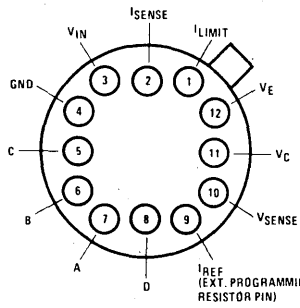
- Output adjustable to 0V
- Line regulation typically 0.008%/V
- Load regulation typically 0.075%
- Remote voltage sensing
- Ripple rejection of 80 dB
- Adjustable precision current limit
- Output currents to 200 mA
- Popular voltages available without external resistors

Schematic Diagram



Connection Diagram

TO-8 Metal Can Package



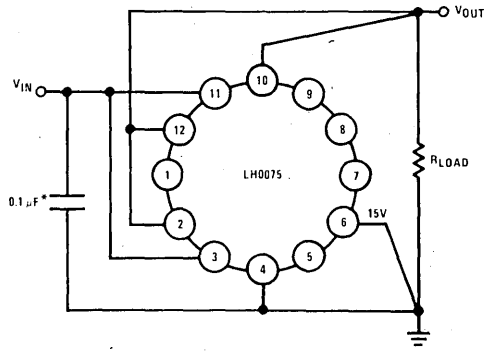
TOP VIEW

Case is electrically isolated

Order Number
LH0075G
LH0075CG
See Package H12B

Typical Applications

Precision 15V Reference Supply without Current Limit



*Needed if device is far from filter capacitors

Absolute Maximum Ratings

Input Voltage	32 V
Output Voltage	27 V
Output Current	200 mA
Power Dissipation	See Curve
Operating Temperature Range	T_{MIN} T_{MAX}
LH0075	−55°C to +125°C
LH0075C	0° to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Conditions for $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted

Parameter	Conditions	LH0075			LH0075C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Line Regulation	$T_A = 25°C$		0.008	0.02		0.008	0.04	%/V
Load Regulation	$T_A = 25°C$, 1 mA < I_{LOAD} < 200 mA							
	$V_{OUT} \leq 5.0$ V		2.5	7.5		2.5	15	mV
	$V_{OUT} \geq 5.0$ V		0.055	0.15		0.055	0.3	%
Reference Current (I_{REF})	$T_A = 25°C$, $V_{IN} = 15$ V	0.998	1.000	1.002	0.995	1.00	1.005	mA
Load Regulation	1 mA < I_{LOAD} < 200 mA							
	$V_{OUT} \leq 5.0$ V		4.0	15		4.0	25	mV
	$V_{OUT} \geq 5.0$ V		0.075	0.3		0.075	0.5	%
Reference Current Drift ($\Delta I_{REF}/\Delta$Temp.)	$V_{IN} = 15$ V		−0.0065			−0.0065		%/°C
Minimum Load Current (I_{LIM})	(Note 1)	98	100	102	95	100	105	μA
Output Voltage Range		0		27	0		27	V
Minimum Input Voltage		10			10			V
Input-Output Differential Voltage	$T_A = 25°C$, 1 mA < I_{LOAD} < 200 mA		3.0	3.2		3.0	3.5	V
Quiescent Supply Current	$V_{IN} = 15$ V		6.0	8.0		6.5	10	mA
Ripple Rejection	$V_{OUT} = 5.0$ V, f = 120 Hz		65			65		dB
	$C_{REF} = 2.2$ μF		80			80		dB
Output Voltage Tolerance	$T_A = 25°C$, (Note 2)		±0.1	±0.5		±0.1	±1.0	%
Output Voltage Change with Temperature ($\Delta V_{OUT}/\Delta$Temp.)	(Note 3)		0.003			0.003		%/°C

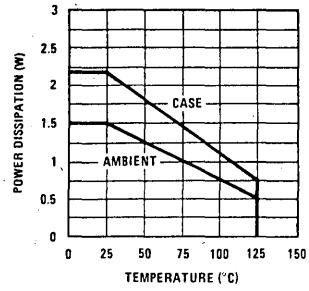
Note 1: Minimum load current is established by I_{LIM}, the current from Q4 (see schematic). I_{LIM} goes directly to the output if the current limit feature is used.

Note 2: For $V_{IN} = 15$ V and V_{OUT} obtained by using R5, R6, R7, and R12 individually.

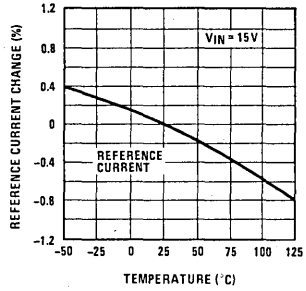
Note 3: Total change over specified temperature range.

Typical Performance Characteristics

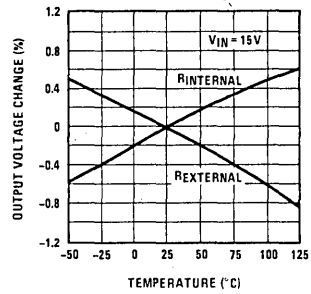
Maximum Power Dissipation



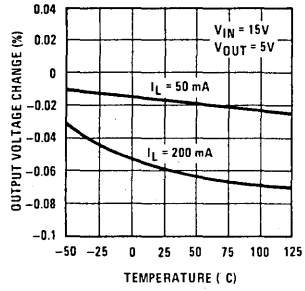
Reference Current Change with Temperature (Normalized)



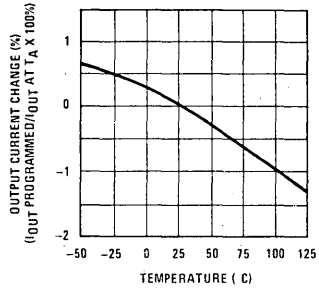
Temperature Stability



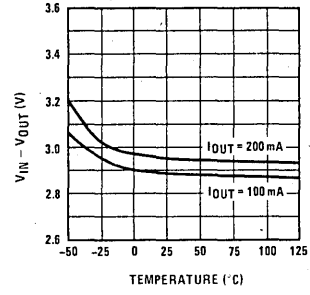
Output Voltage Change with Temperature (Normalized)



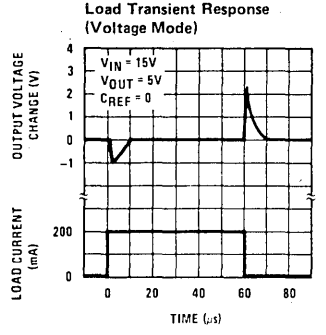
Current Limit



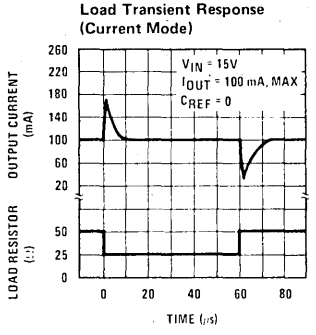
Input–Output Differential Voltage



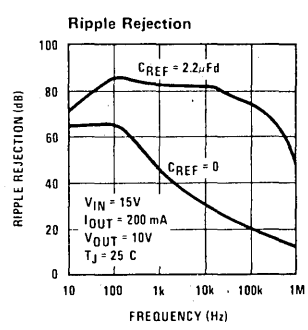
Load Transient Response (Voltage Mode)



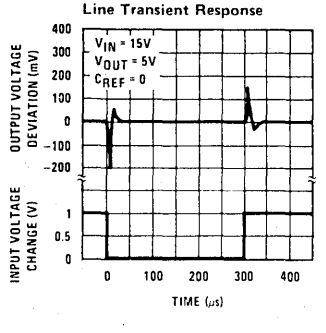
Load Transient Response (Current Mode)



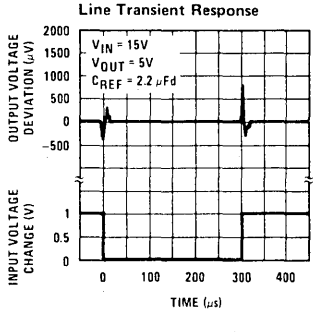
Ripple Rejection



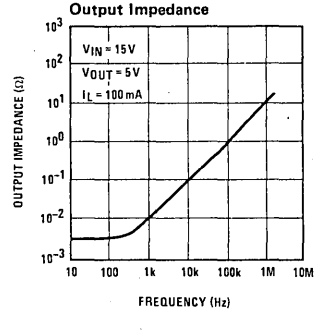
Line Transient Response



Line Transient Response

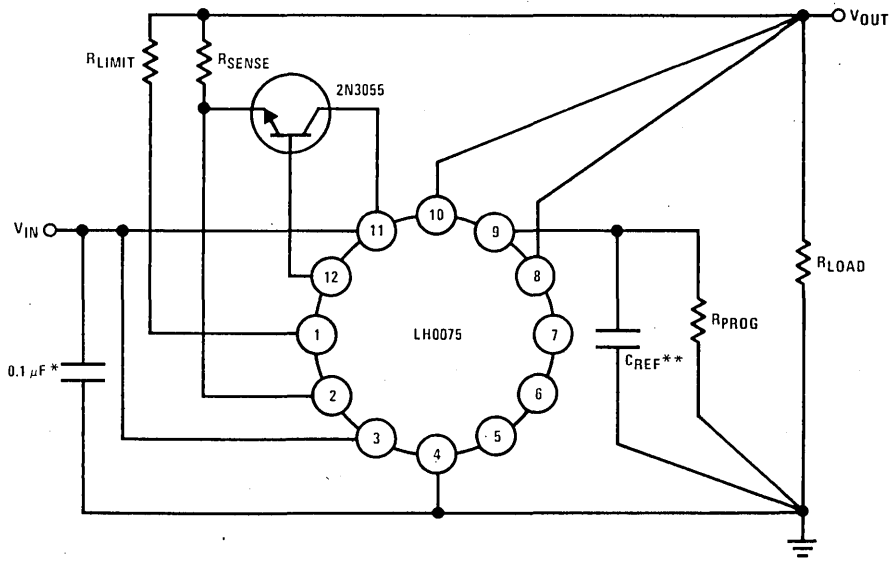


Output Impedance

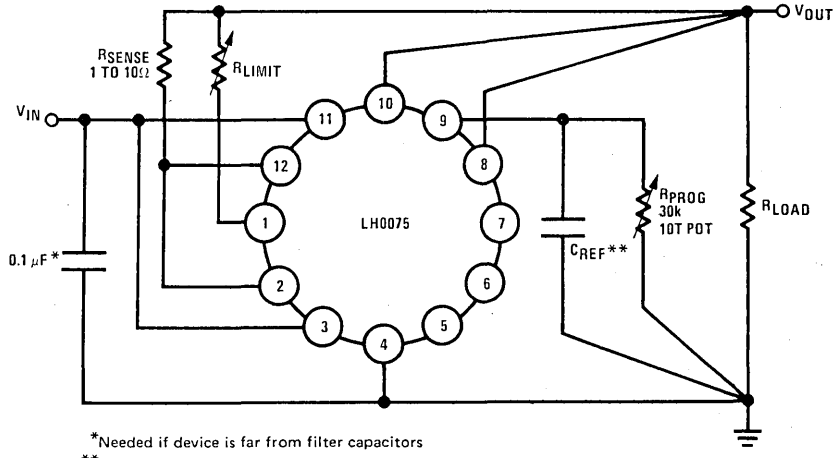


Typical Applications (Cont'd)

2A Regulator with Current Limit



Variable Voltage Reference with Current Limit



*Needed if device is far from filter capacitors
**Optional—improves transient response

$$R_{PROG} = \frac{V_{OUT}\ Desired}{1\ mA} \qquad I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\,\mu A$$

$I_{OUT} \leq 200$ mA

Applications Information

The LH0075 does not require capacitors for stable operation, but an input bypass is recommended if device is far from filter capacitors. A 0.1 μF for input bypassing should be adequate for almost all applications.

Applications Information (Cont'd)

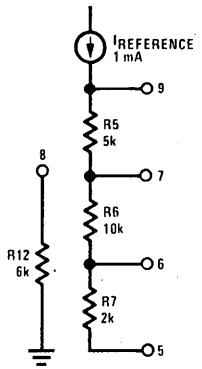
DESCRIPTION OF OPTIONS

Ripple Rejection Compensation. (Increases Ripple Rejection Typically to 80 dB)

The ripple rejection may be improved by connecting an external capacitor between pin 9 and ground. (The typical performance curves show the rejection with a capacitance of 2.2 μFd.)

Internal Voltage Programming

The LH0075 provides various precision output voltages simply by using one or more of the internal resistors. A particular voltage may be obtained by external connections as shown in Table I.



R5, R6, R7 and R12 are precision-trimmed to 0.1%.

FIGURE 1

External Voltage Programming

An external resistance can be connected between pin 9 and ground to obtain any voltage from 0 to 27V using the following equation:

$$R_{EXT} = \frac{V_{OUT}\ \text{Desired}}{1\ \text{mA}}$$

The reference current (I_{REF}) has a typical temperature coefficient of −65 ppm/°C. Choosing a resistive material with a temperature coefficient of 65 ppm/°C will compensate the negative temperature coefficient, resulting in an output voltage with minimal change over the operating temperature range. Example of a good resistive material is Nichrome, which has a typical temperature coefficient of 80 ppm/°C.

Since a current source is used as a reference, this makes remote voltage programming possible.

Current Limit Programming

The maximum current output of the device may be limited by adding two external resistors as shown below. The resistor values are easily calculated with the following equation:

$$I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\,\mu A$$

where R_{SENSE} = 1 to 10Ω

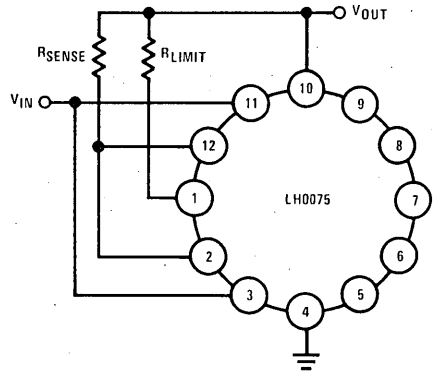


FIGURE 2. Current Limit Programming

This programmable current limit feature can be extended to make the LH0075 a programmable constant current source. This can be done by leaving pin 9 open and setting R_{LIMIT} and R_{SENSE} as desired.

For applications where the current limit is used, a minimum load current of 100 μA is established at the output. This arises from the fact that the constant current used in setting maximum output current is 100 μA, and it goes directly to the output of the LH0075. If the total current drawn from the output is less than the minimum, the output will rise.

As in the remote voltage adjustment application, remote current sensing can be applied similarly. R_{SENSE} must be placed as close to the output of the LH0075 as possible, but R_{LIMIT} can be a fixed resistor or potentiometer located remotely from the device.

TABLE I. Connection Scheme for Internal Available Output Voltages

OUTPUT VOLTAGE (V)	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9
5			Gnd		
6				•	•
8	•	•		•	•
10		Gnd		•	•
12	Gnd			•	•
15		Gnd			
18	•			•	•

National Semiconductor

Voltage References and Regulators

LH0076 Negative Precision Programmable Regulator

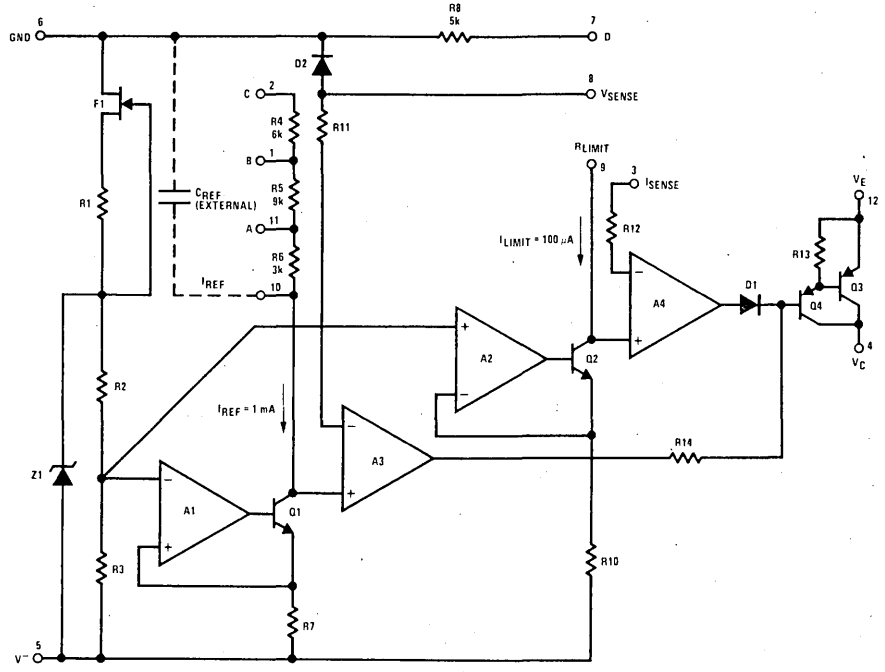
General Description

The LH0076 is a precision programmable regulator for negative voltages. Regulated output voltages from 0 to −27V may be obtained by using 1 external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (−3V, −5V, −6V, −8V, −9V, −12V, −15V and −18V). The output current limit is adjustable from 0 to 200 mA using 2 external resistors. These features provide an inventory of precision regulated values in 1 package.

Features

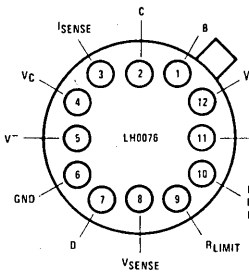
- Line regulation typically 0.005%/V
- Load regulation typically 0.02%
- Remote voltage sensing
- Ripple rejection−70 dB
- Output Adjustable to 0V
- Adjustable precision current limit
- Output current to 200 mA

Schematic Diagram



Connection Diagram

Metal Can Package

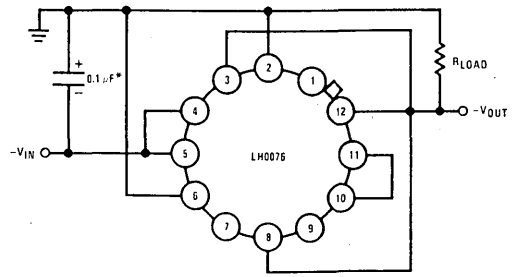


Order Number
LH0076G
LH0076CG
See Package H12B

Case is electrically isolated

Typical Application

Precision − 15V Reference Supply without Current Limit



*Recommended if device is far from filter capacitors

Absolute Maximum Ratings

Input Voltage	−32 V
Output Voltage	−27 V
Output Current	200 mA
Power Dissipation	See Curve
Operating Temperature Range	
LH0076	−55°C to +125°C
LH0076C	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Conditions are for $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted

Parameter	Conditions	LH0076			LH0076C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Line Regulation	$T_A = 25°C$		0.005	0.02		0.005	0.04	%/V
Load Regulation	$T_A = 25°C$, $1mA < I_{LOAD} < 200mA$							
	$V_{OUT} \geq -5.0V$			7.5			15	mV
	$V_{OUT} \leq -5.0V$		0.02	0.15		0.02	0.3	%
Reference Current (I_{REF})	$T_A = 25°C$, $V_{IN} = -15V$	0.998	1.000	1.002	0.995	1.000	1.005	mA
Reference Current Drift ($\Delta I_{REF}/\Delta Temp.$)	$V_{IN} = -15V$		−0.0065			−0.0065		%/°C
Minimum Load Current (I_{LIM})	(Note 1)	98	100	102	95	100	105	μA
Output Voltage Range		0		−27	0		−27	V
Minimum Input Voltage		−10			−10			V
Input-Output Differential Voltage	$T_A = 25°C$, $1mA < I_{LOAD} < 200mA$		2.7	3.2		2.7	3.5	V
Quiescent Supply Current	$V_{IN} = -15V$		11	15		11	15	mA
Ripple Rejection	$V_{OUT} = -5.0V$, $f = 120Hz$		70			70		dB
Output Voltage Tolerance	$T_A = 25°C$, (Note 2)		±0.1	±0.5		±0.1	±1.0	%
Output Voltage Change with Temperature ($\Delta V_{OUT}/\Delta Temp.$)	(Note 3)		0.003			0.003		%/°C

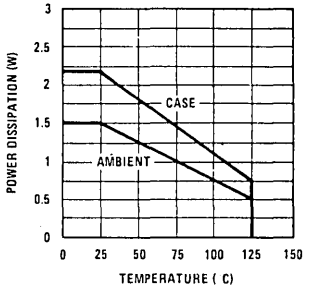
Note 1: Minimum load current is established by I_{LIM}, the current to Q2 (see schematic). I_{LIM} draws directly from the output if the current limit feature is used.

Note 2: For $V_{IN} = -15V$ and V_{OUT} obtained by using R4, R5, R6, and R8 individually.

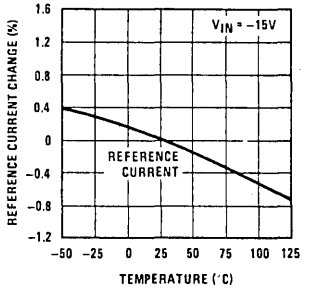
Note 3: Total change over specified temperature range.

Typical Performance Characteristics

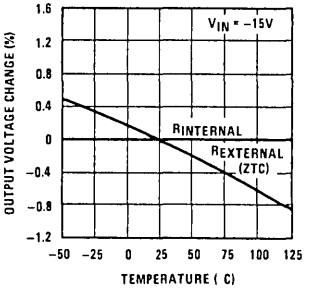
Maximum Power Dissipation



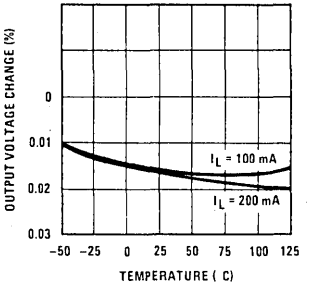
Reference Current Change with Temperature (Normalized)



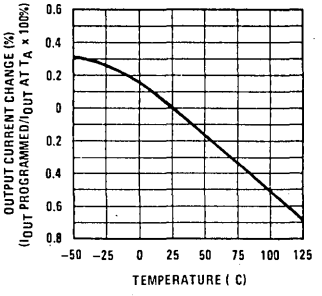
Temperature Stability



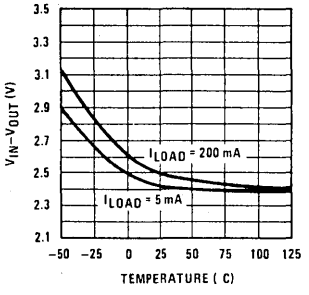
Output Voltage Change with Temperature (Normalized)



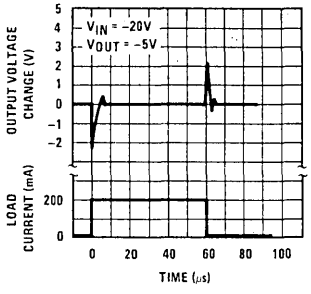
Current Limit



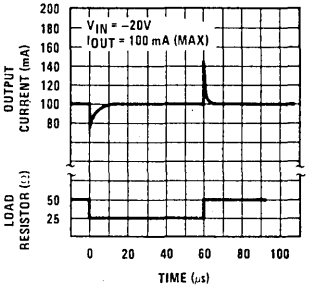
Input-Output Differential Voltage



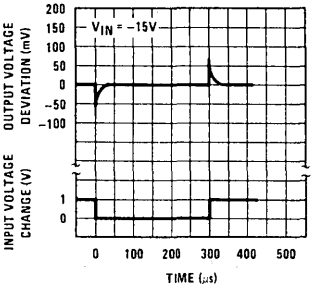
Load Transient Response (Voltage Mode)



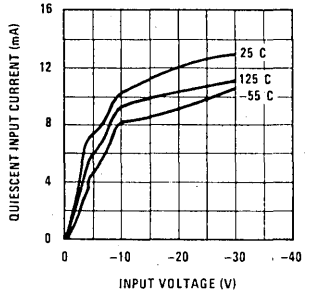
Load Transient Response (Current Mode)



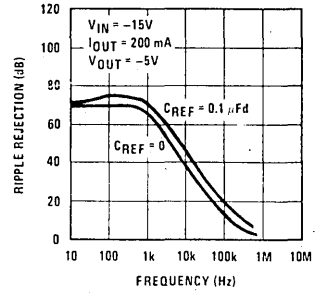
Line Transient Response



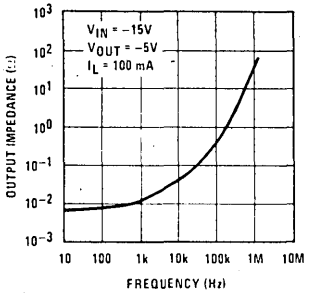
Quiescent Input Current



Ripple Rejection

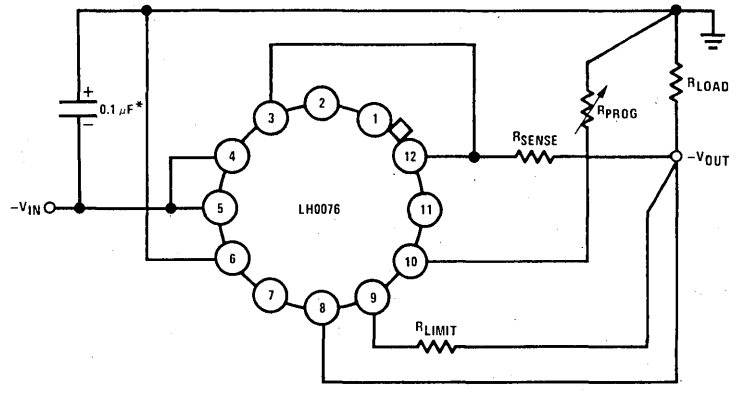


Output Impedance

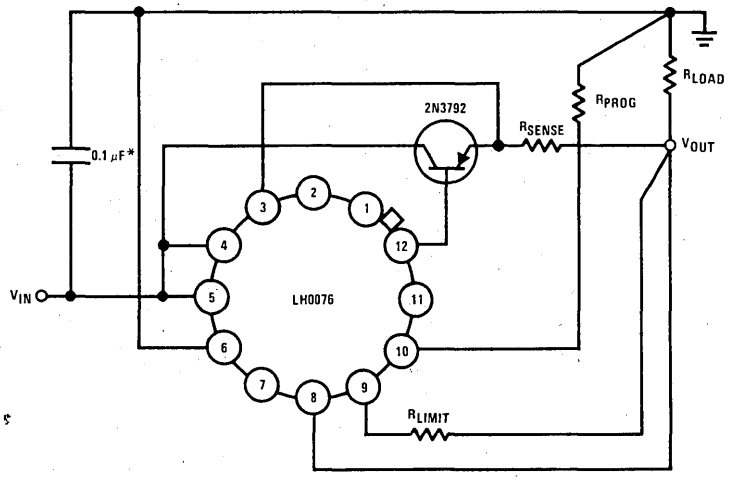


Typical Application (Continued)

Variable Voltage Reference with Current Limit



2-Amp Regulator with Current Limit



*Recommended if device is far from filter capacitors

Application Information

The LH0076 does not require external capacitors for stable operation. However, an input bypass is recommended if the device is far from filter capacitors. A 0.1 μF for input bypassing should be adequate for most applications.

DESCRIPTION OF OPTIONS

External Voltage Programming

An external resistance can be connected between pin 10 and ground to obtain any voltage from 0 to −27V using the following equation:

$$R_{EXT} = \frac{V_{OUT}\ \text{desired}}{-1\ \text{mA}}$$

The reference current (I_{REF}) has a typical temperature coefficient of −60 ppm/°C. Choosing a resistive material with a temperature coefficient of 60 ppm/°C will compensate the negative tempco of the reference current, resulting in an output voltage with minimal change over the operating temperature range. Example of a good resistive material is nichrome, which has a typical tempco of 80 ppm/°C. Nichrome is the resistive material used in the LH0076, resulting in output voltage drift of 20 ppm/°C typically.

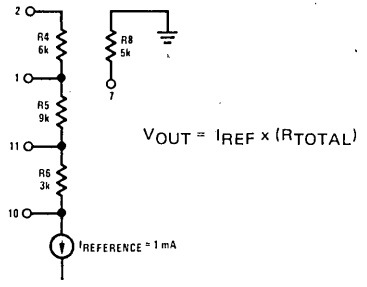
Application Information (Continued)

Because a current source is used as a reference, remote voltage programming is possible.

Internal Voltage Programming

The LH0076 provides various precision output voltages simply by using 1 or more of the internal programming resistors. These voltages may be obtained by using the connections as shown in Table I.

R_{TOTAL} is the total resistance between pin 10 and ground



R4, R5, R6 and R8 are precision trimmed to 0.1%

FIGURE 1

Current Limit Programming

The maximum current output of the device may be limited by adding 2 external resistors as shown in *Figure 2*. The resistor values are calculated using the following equation:

$$I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\,\mu A$$

where R_{SENSE} = 1 to 10Ω

This programming current limit feature can be extended to make the LH0076 a programmable current sink. This can be done by leaving pin 10 open and setting R_{LIMIT} and R_{SENSE} as desired. (See *Figure 3*).

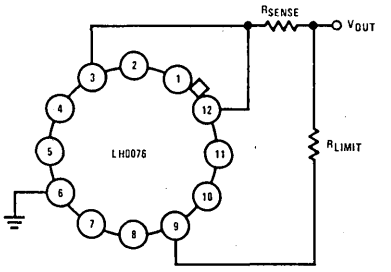


FIGURE 2. Current Limit Programming

For applications where the current limit is used, a minimum load current of 100 μA is established at the output. This arises from the fact that the constant current used in setting maximum output current is 100 μA, and it comes directly from the output of the LH0076. If the total load current is less than this minimum current, the output will drop.

As in the remote voltage adjustment application, remote current sensing can be applied similarly. R_{SENSE} should be placed as close to the output of the LH0076 as possible, but R_{LIMIT} can be a resistor or potentiometer located remotely from the device.

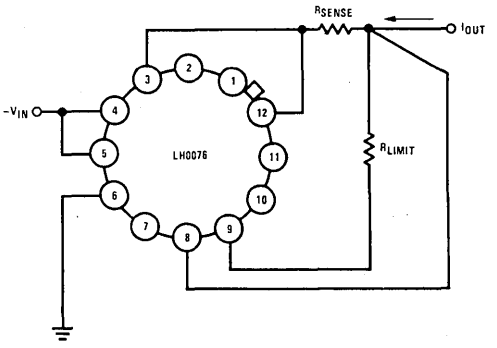


FIGURE 3. Precision Current Sink

TABLE I. Connection Scheme for Internally Available Output Voltages

OUTPUT VOLTAGE (V)	PIN 1	PIN 2	PIN 7	PIN 10	PIN 11
−3					Gnd
−5			•	•	
−6	•	Gnd		•	
−8			•		•
−9	Gnd			•	•
−12	Gnd				
−15		Gnd		•	•
−18		Gnd			

National Semiconductor

LM129/LM329 Precision Reference

General Description

The LM129 and LM329 family are precision multi-current temperature compensated 6.9V zener references with dynamic impedances a factor of 10 to 100 less than discrete diodes. Constructed in a single silicon chip, the LM129 uses active circuitry to buffer the internal zener allowing the device to operate over a 0.5 mA to 15 mA range with virtually no change in performance. The LM129 and LM329 are available with selected temperature coefficients of 0.001, 0.002, 0.005 and 0.01%/°C. These new references also have excellent long term stability and low noise.

A new subsurface breakdown zener used in the LM129 gives lower noise and better long term stability than conventional IC zeners. Further the zener and temperature compensating transistor are made by a planar process so they are immune to problems that plague ordinary zeners. For example, there is virtually no voltage shifts in zener voltage due to temperature cycling and the device is insensitive to stress on the leads.

The LM129 can be used in place of conventional zeners with improved performance. The low dynamic impedance simplifies biasing and the wide operating current allows the replacement of many zener types.

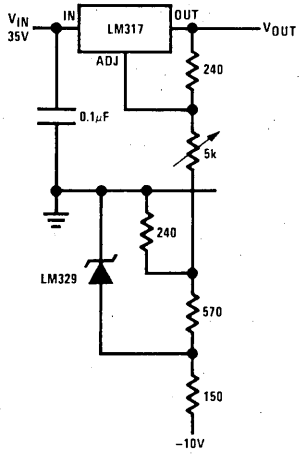
The LM129 is packaged in a 2-lead TO-46 package and is rated for operation over a −55°C to +125°C temperature range. The LM329 for operation over 0−70°C is available in both a hermetic TO-46 package and a TO-92 epoxy package.

Features

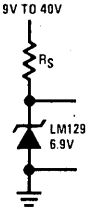
- 0.6 mA to 15 mA operating current
- 0.6Ω dynamic impedance at any current
- Available with temperature coefficients of 0.001%/°C
- 7μV wideband noise
- 5% initial tolerance
- 0.002% long term stability
- Low cost
- Subsurface zener

Typical Applications

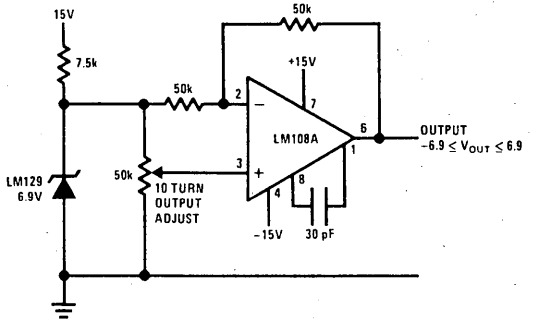
Low Cost 0−25V Regulator



Simple Reference



Adjustable Bipolar Output Reference



Absolute Maximum Ratings

Reverse Breakdown Current	30 mA
Forward Current	2 mA
Operating Temperature Range	
LM129	−55°C to +125°C
LM329	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

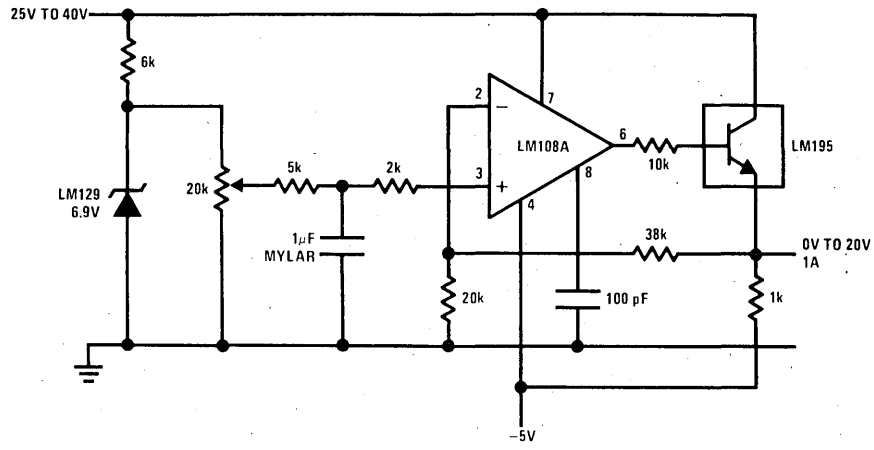
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM129A, B, C			LM329B, C, D			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$T_A = 25°C$, $0.6\ mA \leq I_R \leq 15\ mA$	6.7	6.9	7.2	6.6	6.9	7.25	V
Reverse Breakdown Change with Current	$T_A = 25°C$, $0.6\ mA \leq I_R \leq 15\ mA$		9	14		9	20	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1\ mA$		0.6	1		0.8	2	Ω
RMS Noise	$T_A = 25°C$, $10\ Hz \leq F \leq 10\ kHz$		7	20		7	100	μV
Long Term Stability	$T_A = 45°C \pm 0.1°C$, $I_R = 1\ mA \pm 0.3\%$		20			20		ppm
Temperature Coefficient	$I_R = 1\ mA$							
LM129A			6	10				ppm/°C
LM129B, LM329B			15	20		15	20	ppm/°C
LM129C, LM329C			30	50		30	50	ppm/°C
LM329D						50	100	ppm/°C
Change In Reverse Breakdown Temperature Coefficient	$1\ mA \leq I_R \leq 15\ mA$		1			1		ppm/°C
Reverse Breakdown Change with Current	$1\ mA \leq I_R \leq 15\ mA$		12			12		mV
Reverse Dynamic Impedance	$1\ mA \leq I_R \leq 15\ mA$		0.8			1		Ω

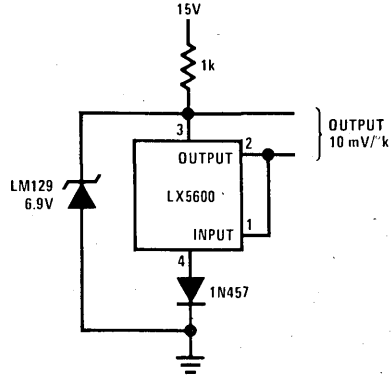
Note 1: These specifications apply for $-55°C \leq T_A \leq +125°C$ for the LM129 and $0°C \leq T_A \leq +70°C$ for the LM329 unless otherwise specified. The maximum junction temperature for an LM129 is 150°C and LM329 is 100°C. For operating at elevated temperature, devices in TO-46 package must be derated based on a thermal resistance of 440°C/W junction to ambient or 80°C/W junction to case. For the TO-92 package, the derating is based on 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to a PC board.

Typical Applications (Cont'd)

0V to 20V Power Reference

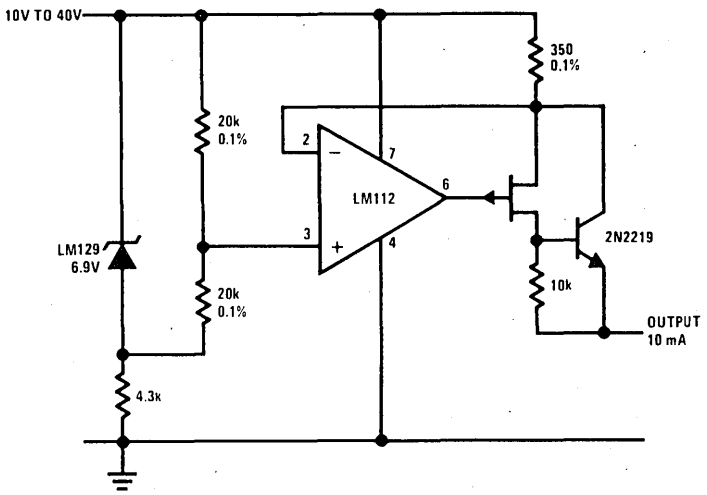


External Reference for Temperature Transducer

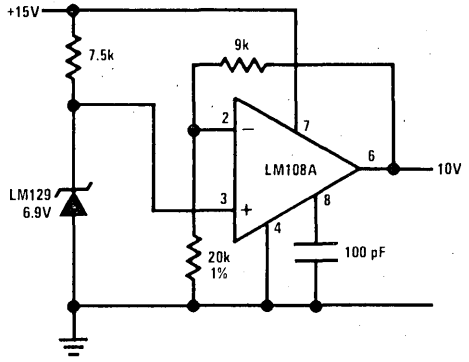


Typical Applications (Cont'd)

Positive Current Source

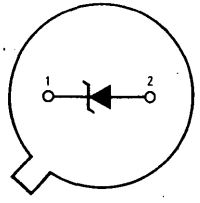


Buffered Reference with Single Supply



Connection Diagrams

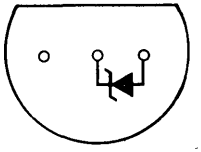
Metal Can Package



BOTTOM VIEW

Order Number LM129AH, LM129BH
LM129CH, LM329BH, LM329CH
or LM329DH
See NS Package H02A

Plastic Package

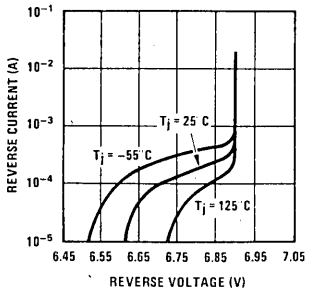


BOTTOM VIEW

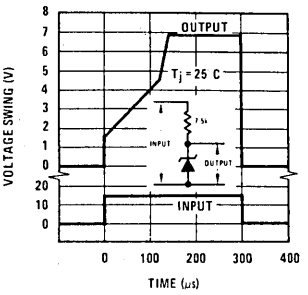
Order Number LM329BZ, LM329CZ
or LM329DZ
See NS Package Z03A

Typical Performance Characteristics

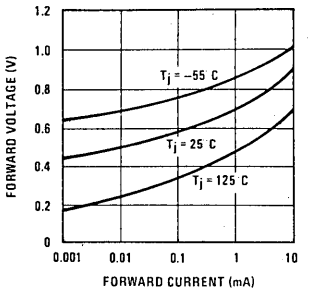
Reverse Characteristics



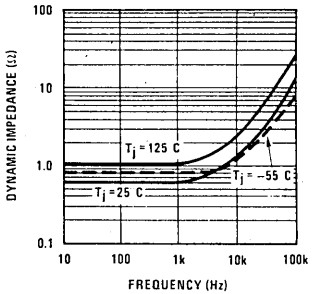
Response Time



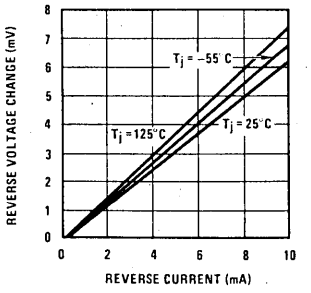
Forward Characteristics



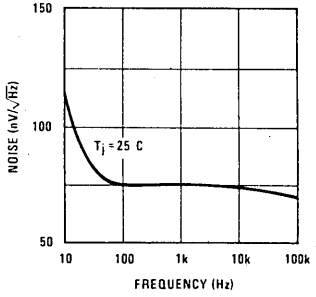
Dynamic Impedance



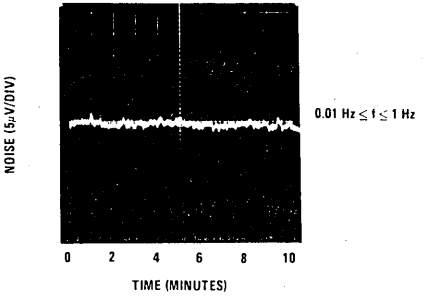
Reverse Voltage Change



Zener Noise Voltage



Low Frequency Noise Voltage



LM199A/LM299A/LM399A Precision Reference

General Description

The LM199A/LM299A/LM399A are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199A series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199A is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

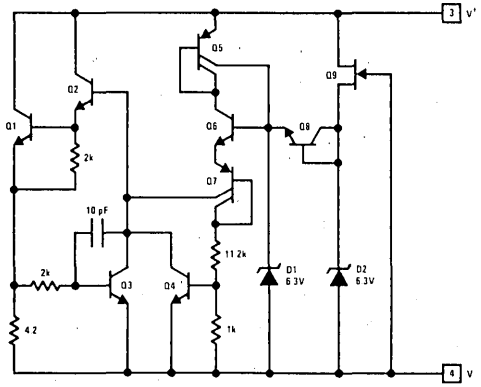
The LM199A can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199A can replace references in existing equipment with a minimum of wiring changes.

The LM199A series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299A is rated for operation from −25°C to +85°C and the LM399A is rated from 0°C to +70°C.

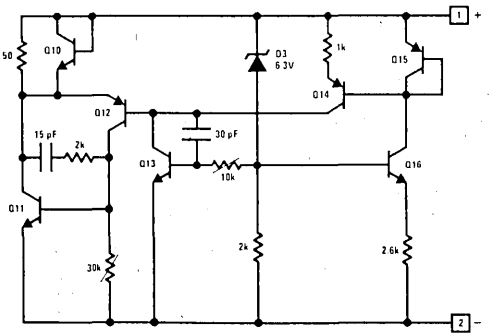
Features

- Guaranteed 0.00005%/°C temperature coefficient
- Low dynamic impedance – 0.5Ω
- Initial tolerance on breakdown voltage – 2%
- Sharp breakdown at 400μA
- Wide operating current – 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization – 300 mW at 25°C
- Long term stability – 20 ppm

Schematic Diagrams



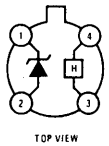
Temperature Stabilizer



Reference

Connection Diagram

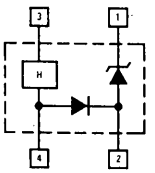
Metal Can Package



TOP VIEW

Order Number
LM199AH
LM299AH
LM399AH
See Package H04D

Functional Block Diagram



Absolute Maximum Ratings

Temperature Stabilizer Voltage	40V
Reverse Breakdown Current	20 mA
Forward Current	1 mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	+40V −0.1V
Operating Temperature Range	
LM199A	−55°C to +125°C
LM299A	−25°C to +85°C
LM399A	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	LM199A, LM299A			LM399A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$0.5\ mA \leq I_R \leq 10\ mA$	6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5\ mA \leq I_R \leq 10\ mA$		6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$		0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \leq T_A \leq 85°C$ } LM199A		0.00002	0.00005				%/°C
	$85°C \leq T_A \leq 125°C$ } LM199A		0.0005	0.0010				%/°C
	$-25°C \leq T_A \leq 85°C$ LM299A		0.00002	0.00005				%/°C
	$0°C \leq T_A \leq 70°C$ LM399A					0.00003	0.0001	%/°C
RMS Noise	$10\ Hz \leq f \leq 10\ kHz$		7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \leq T_A \leq 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$		20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$		8.5	14		8.5	15	mA
	$T_A = -55°C$		22	28				
Temperature Stabilizer Supply Voltage (Note 3)		9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		3			3		Seconds
Initial Turn-on Current	$9 \leq V_S \leq 40$, $T_A = 25°C$		140	200		140	200	mA

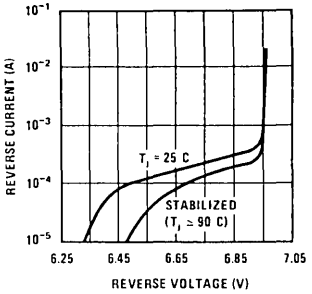
Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55°C \leq T_A \leq +125°C$ for the LM199A; $-25°C \leq T_A \leq +85°C$ for the LM299A and $0°C \leq T_A \leq +70°C$ for the LM399A.

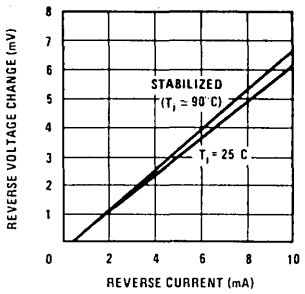
Note 3: CAUTION. If the device is operated for more than 60 seconds with heater supply voltage between 2V and 9V the heater temperature control circuitry is not properly biased and the device can rise to approximately +150°C.

Typical Performance Characteristics

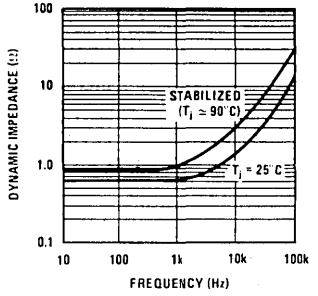
Reverse Characteristics



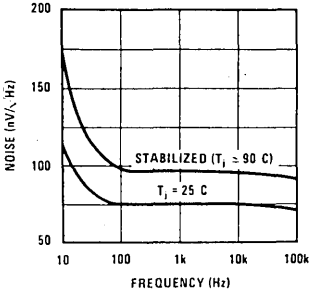
Reverse Voltage Change



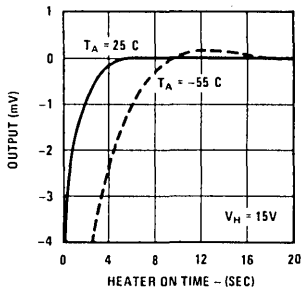
Dynamic Impedance



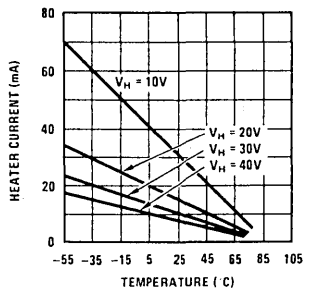
Zener Noise Voltage



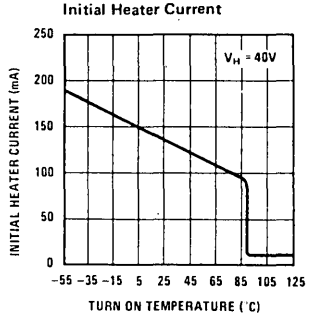
Stabilization Time



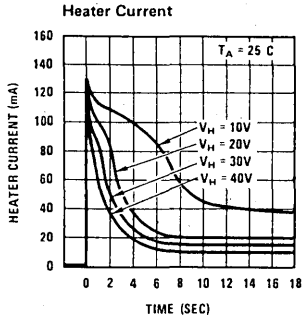
Heater Current



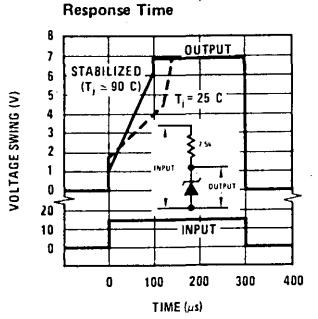
Initial Heater Current



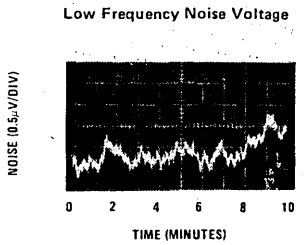
Heater Current



Response Time

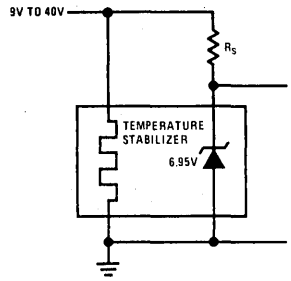


Low Frequency Noise Voltage

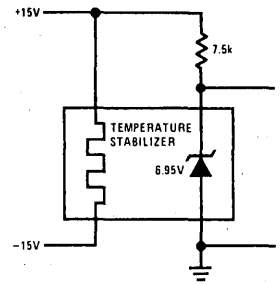


Typical Applications

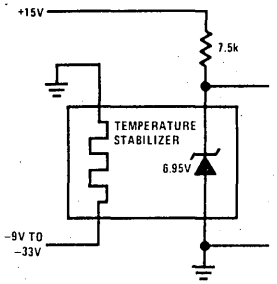
Single Supply Operation



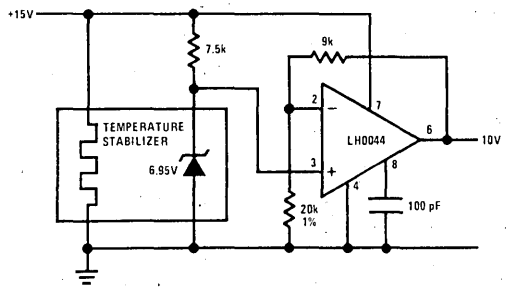
Split Supply Operation



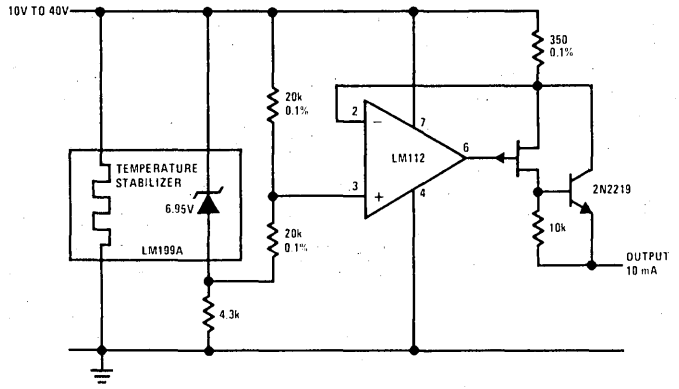
Negative Heater Supply with Positive Reference



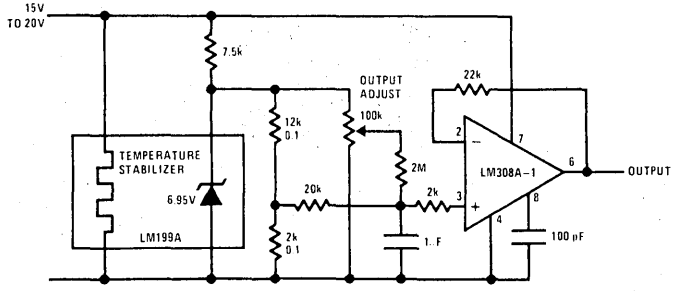
Buffered Reference With Single Supply



Positive Current Source

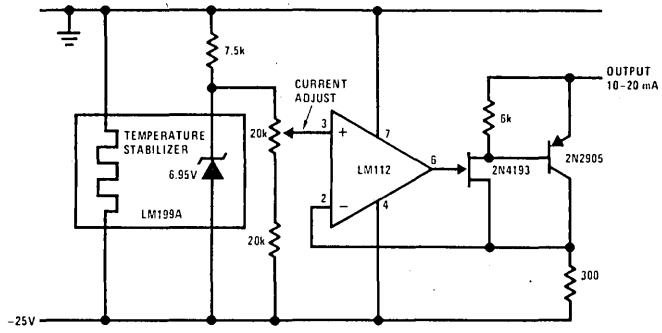


Standard Cell Replacement

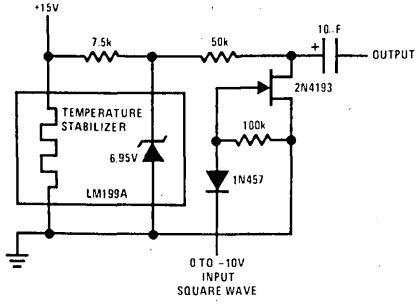


Typical Applications (Cont'd)

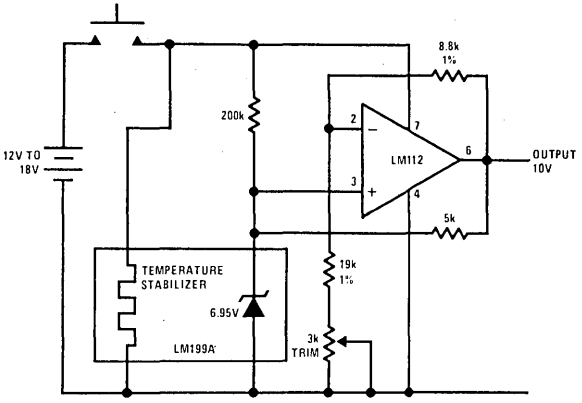
Negative Current Source



Square Wave Voltage Reference

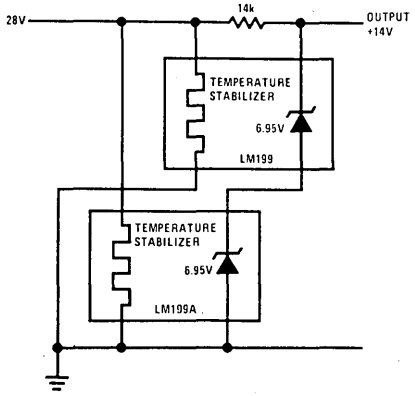


Portable Calibrator*

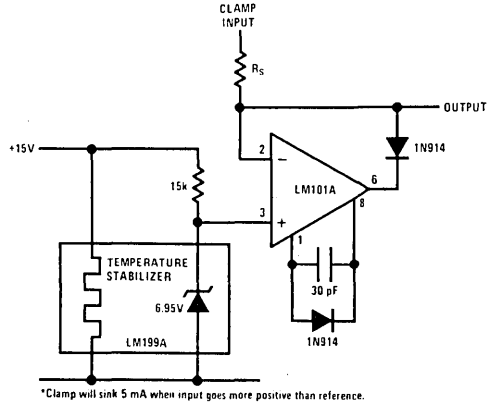


*Warm-up time 10 seconds; intermittant operation does not degrade long term stability.

14V Reference



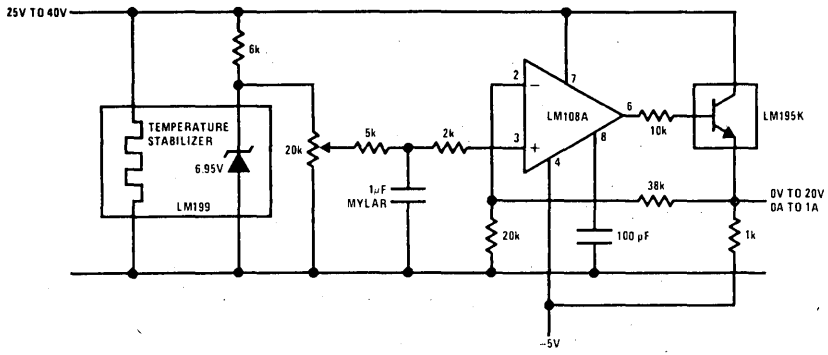
Precision Clamp*



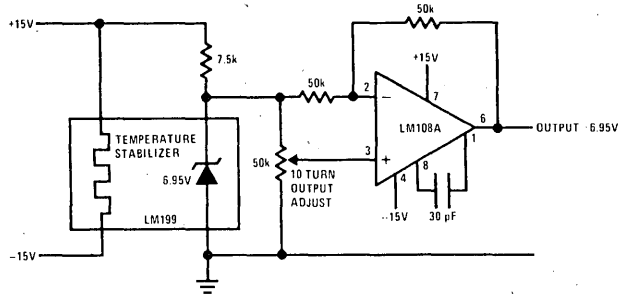
*Clamp will sink 5 mA when input goes more positive than reference.

Typical Applications (Cont'd)

0V to 20V Power Reference



Bipolar Output Reference



National Semiconductor

LM199/LM299/LM399 Precision Reference

General Description

The LM199/LM299/LM399 are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199 series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

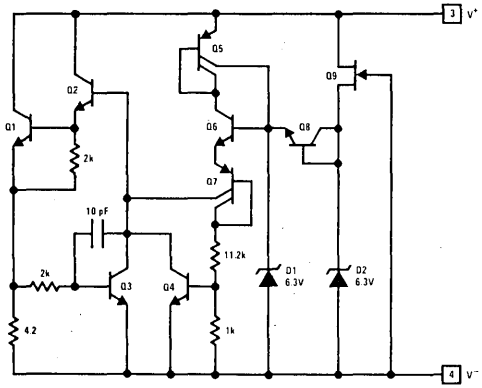
The LM199 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199 can replace references in existing equipment with a minimum of wiring changes.

The LM199 series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299 is rated for operation from −25°C to +85°C and the LM399 is rated from 0°C to +70°C.

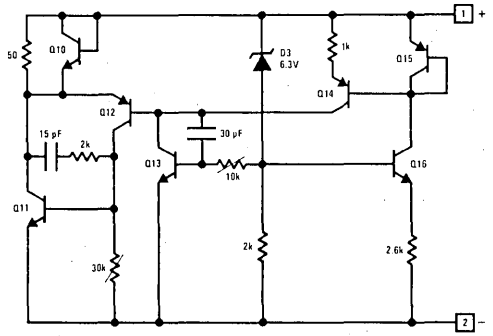
Features

- Guaranteed 0.0001%/°C temperature coefficient
- Low dynamic impedance – 0.5Ω
- Initial tolerance on breakdown voltage – 2%
- Sharp breakdown at 400μA
- Wide operating current – 500μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization – 300 mW at 25°C
- Long term stability – 20 ppm

Schematic Diagrams



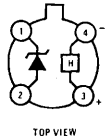
Temperature Stabilizer



Reference

Connection Diagram

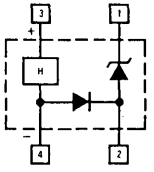
Metal Can Package



TOP VIEW

Order Number
LM199H
LM299H
LM399H
See NS Package H04D

Functional Block Diagram



Absolute Maximum Ratings

Temperature Stabilizer Voltage	40V
Reverse Breakdown Current	20 mA
Forward Current	1 mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	40V −0.1V
Operating Temperature Range	
LM199	−55°C to +125°C
LM299	−25°C to +85°C
LM399	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 2)

PARAMETER	CONDITIONS	LM199/LM299			LM399			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$0.5\ mA \leq I_R \leq 10\ mA$	6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5\ mA \leq I \leq 10\ mA$		6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$		0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \leq T_A \leq 85°C$ LM199		0.00003	0.0001				%/°C
	$85°C \leq T_A \leq 125°C$ LM199		0.0005	0.0015				%/°C
	$-25°C \leq T_A \leq 85°C$ LM299		0.00003	0.0001				%/°C
	$0°C \leq T_A \leq 70°C$ LM399					0.00003	0.0002	%/°C
RMS Noise	$10\ Hz \leq f \leq 10\ kHz$		7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \leq T_A \leq 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$		20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$		8.5	14		8.5	15	mA
	$T_A = -55°C$		22	28				
Temperature Stabilizer Supply Voltage	(Note 3)	9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		3			3		Seconds
Initial Turn-on Current	$9 \leq V_S \leq 40$, $T_A = 25°C$, (Note 3)		140	200		140	200	mA

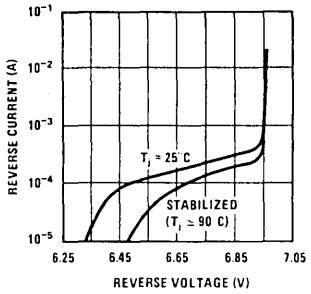
Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55°C \leq T_A \leq +125°C$ for the LM199; $-25°C \leq T_A \leq +85°C$ for the LM299 and $0°C \leq T_A \leq +70°C$ for the LM399.

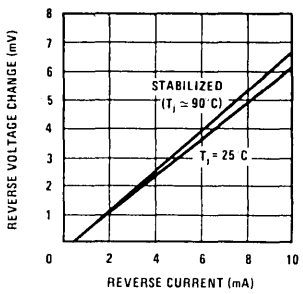
Note 3: This initial current can be reduced by adding an appropriate resistor and capacitor to the heater circuit. See the performance characteristic graphs to determine values.

Typical Performance Characteristics

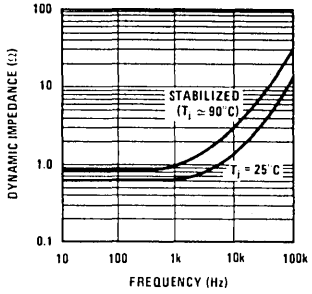
Reverse Characteristics



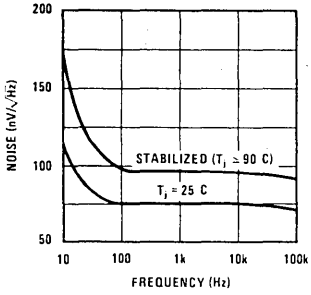
Reverse Voltage Change



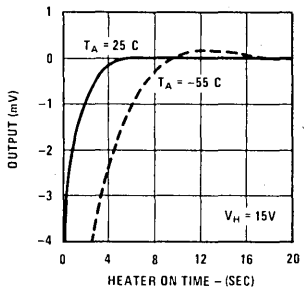
Dynamic Impedance



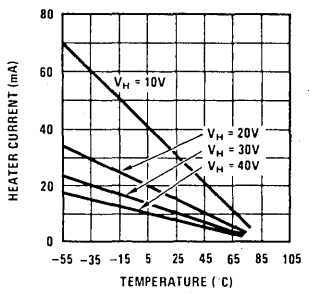
Zener Noise Voltage



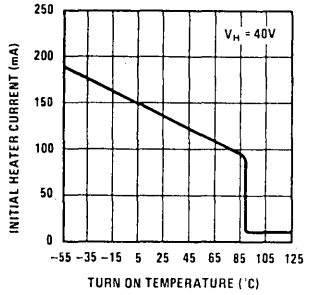
Stabilization Time



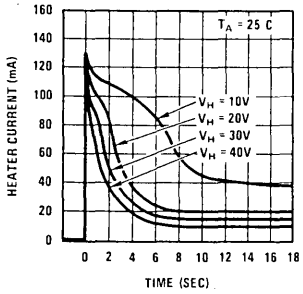
Heater Current



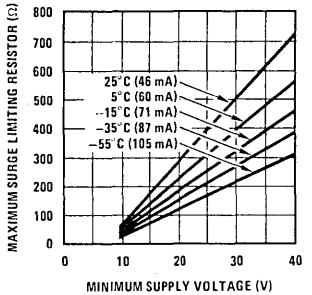
Initial Heater Current



Heater Current (To Limit This Surge, See Next Graph)

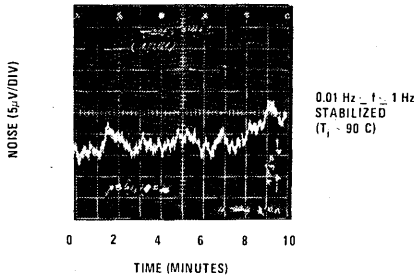


Heater Surge Limit Resistor vs Minimum Supply Voltage at Various Minimum Temperatures

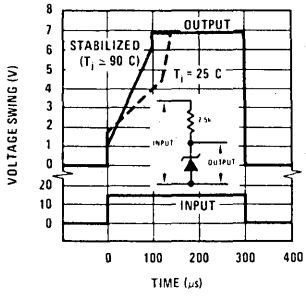


*Heater must be bypassed with a 2 μF or larger tantalum capacitor if maximum value resistors are used. Otherwise, 30% to 50% smaller values must be used. If heater oscillates, resistor value may be too small.

Low Frequency Noise Voltage

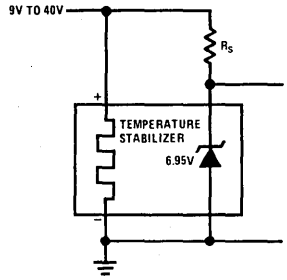


Response Time

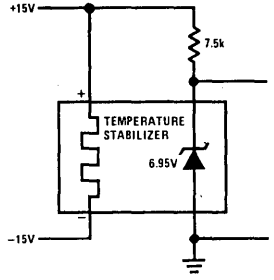


Typical Applications

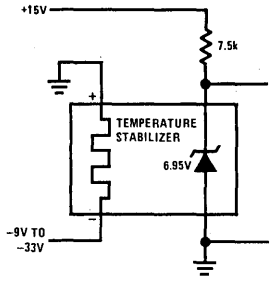
Single Supply Operation



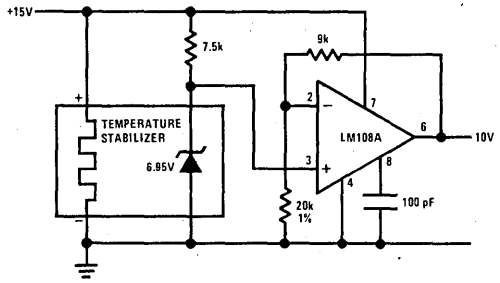
Split Supply Operation



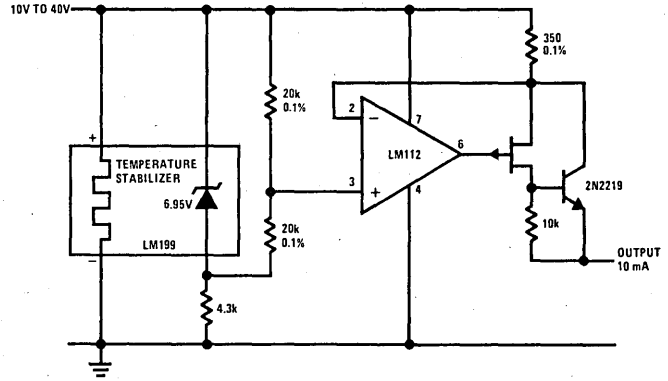
Negative Heater Supply with Positive Reference



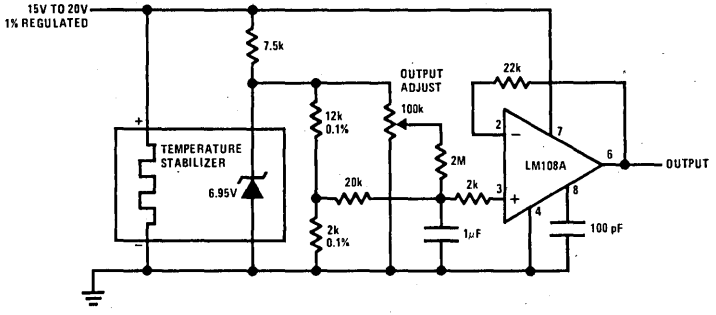
Buffered Reference With Single Supply



Positive Current Source

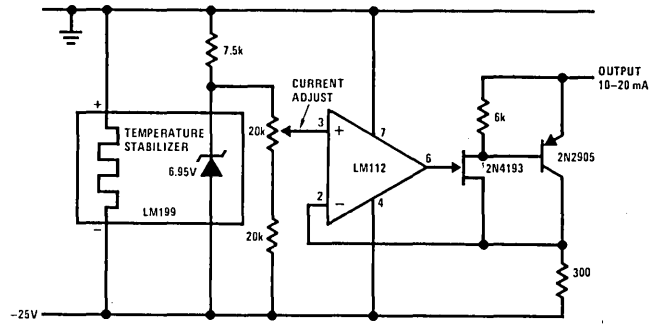


Standard Cell Replacement

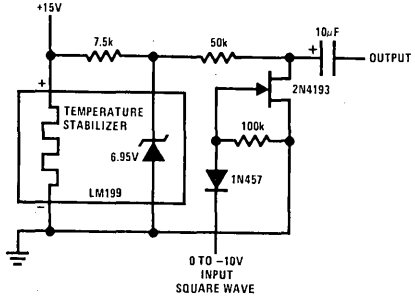


Typical Applications (Continued)

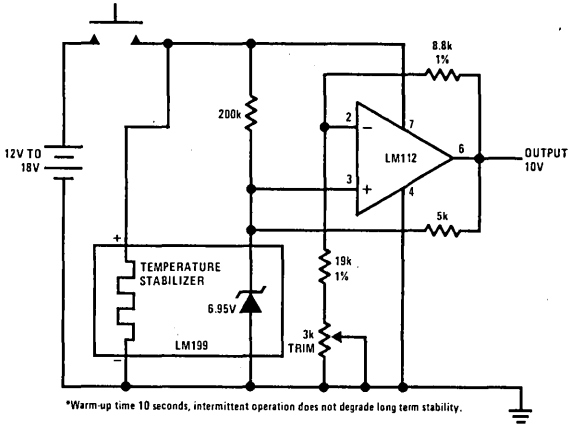
Negative Current Source



Square Wave Voltage Reference

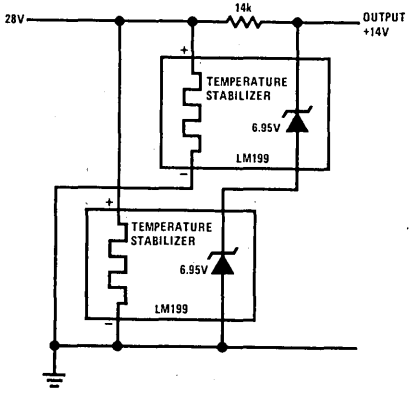


Portable Calibrator*

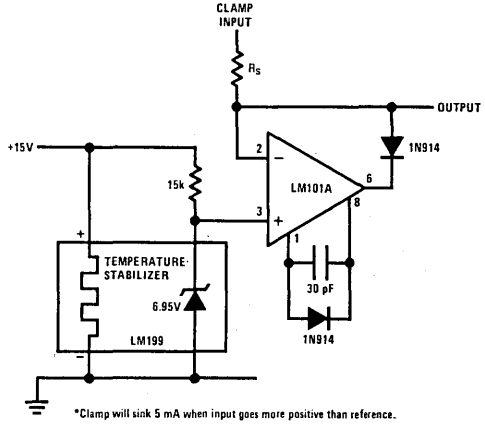


*Warm-up time 10 seconds, intermittent operation does not degrade long term stability.

14V Reference



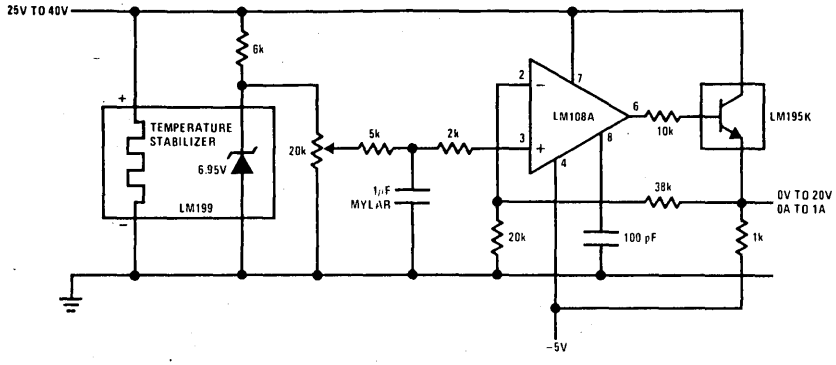
Precision Clamp*



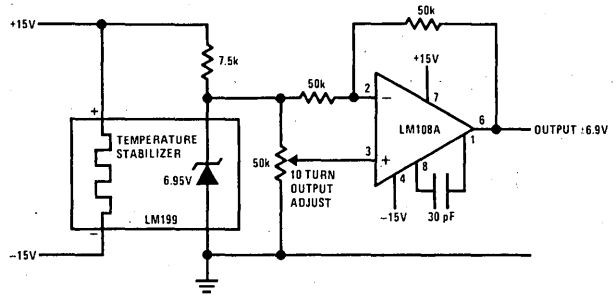
*Clamp will sink 5 mA when input goes more positive than reference.

Typical Applications (Continued)

0V to 20V Power Reference



Bipolar Output Reference



National Semiconductor

PRELIMINARY

LH1605/LH1605C 5 Amp, High Efficiency Switching Regulator

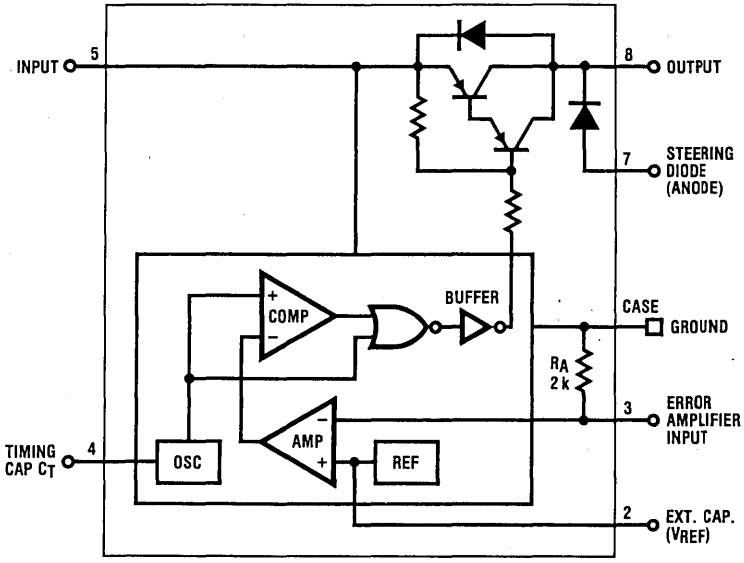
General Description

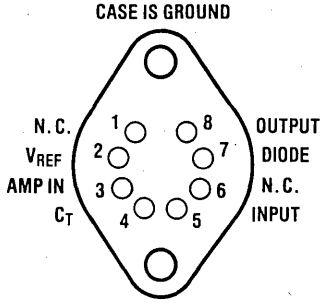
The LH1605 is a hybrid switching regulator with high output current capabilities. It incorporates a temperature-compensated voltage reference, a duty cycle modulator with the oscillator frequency programmable, error amplifier, high current-high voltage output switch, and a power diode. The LH1605 can supply up to 5 A of output current over a wide range of regulated output voltage.

Features

- Step down switching regulator
- Output adjustable from 3.0 to 30V
- 5 A output current
- High efficiency
- Frequency adjustable to 100 kHz
- Standard 8-pin TO-3 package

Block Diagram and Connection Diagram





Order Numbers
LH1605K
LH1605CK

Absolute Maximum Ratings

V_{IN}	Input Voltage	35V Max.
I_O	Output Current	6A
T_J	Operating Temperature	150°C
P_D	Internal Power Dissipation	20W
T_A	Operating Temperature Range	
	LH1605C	−25°C to +85°C
	LH1605	−55°C to +125°C
T_{STG}	Storage Temperature Range	−65°C to +150°C
D.C.	Duty Cycle	20% to 80%
V_R (V_{8-7})	Steering Diode Reverse Voltage	60V
I_D (I_{7-8})	Steering Diode Forward Current	6A

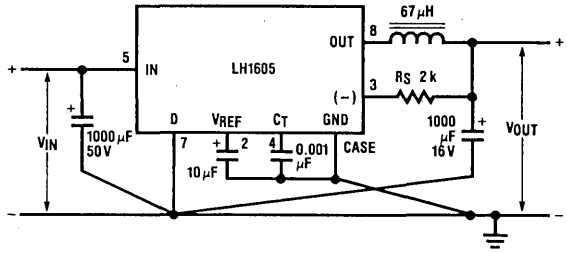
Electrical Characteristics $T_C = 25°C$, $V_{IN} = 15V$, $V_{OUT} = 10V$ unless otherwise specified.

Symbol	Characteristics	Conditions	LH1605			LH1605C			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OUT}	Output Voltage Range	$V_{IN} \geq V_O + 5V$ $I_O = 2A$ (Note 2)	3.0		30	3.0		30	V
V_S	Switch Saturation Voltage	$I_C = 5.0A$ $I_C = 2.0A$		1.6 1.0	2.0 1.2		1.6 1.0	2.0 1.2	V
V_F	Steering Diode On Voltage	$I_D = 5.0A$ $I_D = 2.0A$		1.2 1.0	2.8 2.0		1.2 1.0	2.8 2.0	V
V_{IN}	Supply Voltage Range		10		35	10		35	V
I_R	Steering Diode Reverse Current	$V_R = 25V$		0.1	5.0		0.1	5.0	μA
I_Q	Quiescent Current	$I_{OUT} = 0.2A$		20			20		mA
V_2	Voltage on Pin 2			2.5			2.5		V
$\Delta V_2/\Delta T$	V_2 Temperature Coeff.			100			100		ppm/°C
V_4	Voltage Swing — Pin 4			3.0			3.0		V
I_4	Charging Current — Pin 4			70			70		μA
R_A	Resistance Pin 3 to GND			2.0			2.0		KΩ
$\Delta R_A/\Delta T$	Resistance Temp. Coeff.			75			75		ppm/°C
t_r	Voltage Rise Time	$I_{OUT} = 2.0A$ $I_{OUT} = 5.0A$		350 500			350 500		ns
t_f	Voltage Fall Time	$I_{OUT} = 2.0A$ $I_{OUT} = 5.0A$		300 400			300 400		ns
t_s	Storage Time	$I_{OUT} = 5.0A$		1.5			1.5		μs
t_d	Delay Time			100			100		ns
P_D	Power Dissipation	$V_{OUT} = 10V$ $I_{OUT} = 5.0A$		16			16		W
η	Efficiency			75			75		%
θ_{JC}	Thermal Resistance			5.0			5.0		°C/W

Note 1: θ_{JA} is typically 30°C/W for natural convection cooling.

Note 2: V_{OUT} refers to the output voltage range of a switching supply after the output LC filter as shown in the Typical Application circuit.

Typical Application



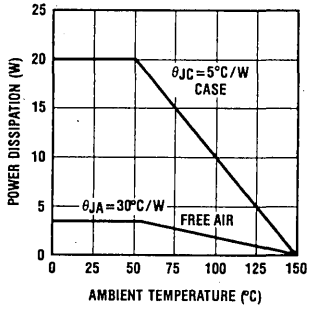
Minimum $V_{IN} - V_{OUT} = 5V$ for proper operation.

$$R_S = \frac{2 \times 10^3 (V_{OUT} - 2.5)}{2.5}$$

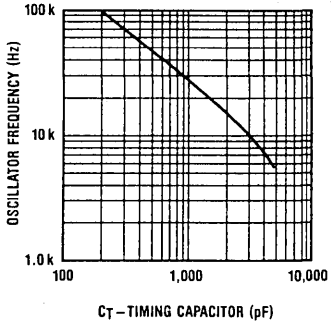
$V_{IN} = 10 - 18V$
$V_{OUT} = 5V$
$I_{OUT} = 3A$ (Max.)
$I_{OUT} = 1A$ (Min.)
$\eta \cong 70\%$

Load Reg. = 50 mV
Line Reg. = 10 mV
Ripple = 20 mV

Power Derating Curve



Frequency vs. Timing Capacitance



Design Equations

$$\text{Efficiency } (\eta) = \frac{P_{OUT} \times 100}{P_{IN}}$$

$$\text{Transistor DC Losses } (P_T) = I_{OUT} \times V_S \left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right)$$

$$\text{Diode DC Losses } (P_D) = I_{OUT} \times V_F \left(\frac{t_{OFF}}{t_{ON} + t_{OFF}}\right)$$

$$\text{Drive Circuit Losses } (D_L) = \frac{V_{IN}^2}{300} \times \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

$$\text{Switching Losses Transistor } (P_S) = V_{IN} \times I_{OUT} \times \frac{t_r + t_f}{2(t_{ON} + t_{OFF})}$$

$$\text{Transistor Duty Cycle} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Diode Duty Cycle} = \frac{t_{OFF}}{t_{ON} + t_{OFF}} = 1 - \frac{V_{OUT}}{V_{IN}}$$

$$\text{Power Inductor } (P_L) = I_{OUT}^2 \times R_L \text{ (Winding Resistance)}$$

$$\text{Efficiency } (\eta) = \frac{V_{OUT} I_{OUT}}{V_{OUT} I_{OUT} + P_T + P_D + D_L + P_S + P_L} \times 100\%$$

Section 8

Analog Switches

8

Section 8. Analog Switches

Function		Drain-Source "On" Resistance	Drain-Gate Leakage Current	t_{ON}	t_{OFF}	Part Number		Page Number
Type	Style					−55°C to 125°C	−25°C to 85°C	
PMOS	DPDT	200Ω	200pA	350ns	600ns	AH0014	AH0014C	8-7
PMOS	DPDT	200Ω	200pA	100ns	600ns	AH0015	AH0015C	8-7
PMOS	Dual DPST	200Ω	200pA	100ns	600ns	AH0019	AH0019C	8-7
NJFET	Dual SPDT	10Ω	10nA	1.0μs	2.5μs	AH0140	AH0140C	8-10
NJFET	Dual SPDT	15Ω	10nA	1.0μs	2.5μs	AH0153	AH0153C	8-10
NJFET	Dual SPDT	30Ω	1nA	0.8μs	1.0μs	AH0129	AH0129C	8-10
NJFET	Dual SPDT	50Ω	1nA	0.8μs	1.0μs	AH0153	AH0153C	8-10
NJFET	Dual SPDT	80Ω	1nA	0.8μs	1.0μs	AH0126	AH0126C	8-10
NJFET	Dual SPDT	10Ω	10nA	1.0μs	2.5μs	AH0141	AH0141C	8-10
NJFET	Dual SPST	15Ω	10nA	1.0μs	2.5μs	AH0151	AH0151C	8-10
NJFET	Dual SPST	30Ω	1nA	0.8μs	1.0μs	AH0133	AH0133C	8-10
NJFET	Dual SPST	50Ω	1nA	0.8μs	1.0μs	AH0152	AH0152C	8-10
NJFET	Dual SPST	80Ω	1nA	0.8μs	1.0μs	AH0134	AH0134C	8-10
NJFET	DPDT	10Ω	10nA	1.0μs	2.5μs	AH0145	AH0145C	8-10
NJFET	DPDT	15Ω	10nA	1.0μs	2.5μs	AH0163	AH0163C	8-10
NJFET	DPDT	30Ω	1nA	0.8μs	1.0μs	AH0139	AH0139C	8-10
NJFET	DPDT	50Ω	1nA	0.8μs	1.0μs	AH0164	AH0164C	8-10
NJFET	DPDT	80Ω	1nA	0.8μs	1.0μs	AH0142	AH0142C	8-10
NJFET	SPDT	10Ω	10nA	1.0μs	2.5μs	AH0146	AH0146C	8-10
NJFET	SPDT	15Ω	10nA	1.0μs	2.5μs	AH0161	AH0161C	8-10
NJFET	SPDT	30Ω	1nA	0.8μs	1.0μs	AH0144	AH0144C	8-10
NJFET	SPDT	50Ω	1nA	0.8μs	1.0μs	AH0162	AH0162C	8-10
NJFET	SPDT	80Ω	1nA	0.8μs	1.0μs	AH0143	AH0143C	8-10
NJFET	Dual SPST	100Ω	1nA	1.5μs	0.75μs	AH2114	AH2114C	8-17

Additional information on analog switches may be found in the *FET* and *Linear* Data Books.

Analog Switches/Multiplexers Selection Guide

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
Dual SPST					
10	±10	AH0141/DG141	TTL	−18, 12	0.8/1.1μs
30	±10	AH0133/DG133	TTL	−18, 12	0.5/0.9μs
80	±10	AH0134/DG134	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0151/DG151	TTL	±15	0.8/1.1μs
50	±7.5	AH0152/DG152	TTL	±15	0.5/0.9μs
Quad SPST					
200-600	±10	AH0015	TTL	−20, 10, 5	100/400 ns
*200	±10	LF11201	TTL	±15	90/500 ns
*200	±10	LF11202	TTL	±15	90/500 ns
*200	±10	LF11331	TTL	±15	90/500 ns
*200	±10	LF11332	TTL	±15	90/500 ns
*200	±10	LF11333	TTL	±15	90/500 ns
*250	±10	LF13201	TTL	±15	90/500 ns
*250	±10	LF13202	TTL	±15	90/500 ns
*250	±10	LF13331	TTL	±15	90/500 ns
*250	±10	LF13332	TTL	±15	90/500 ns
*250	±10	LF13333	TTL	±15	90/500 ns
280	±7.5	CD4066	CMOS	±7.5	
850	±7.5	CD4016	CMOS	±7.5	
*30	±7.5	AM193	TTL	±15, 5	180/150 ns
*75	±10	AM194	TTL−	±15, 5	300/150 ns

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
SPDT					
10	±10	AH0146/DG146	TTL	−18, 12	0.8/1.1μs
30	±10	AH0144/DG144	TTL	−18, 12	0.5/0.9μs
80	±10	AH0143/DG143	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0161/DG161	TTL	±15	0.8/1.1μs
50	±7.5	AH0162/DG162	TTL	±15	0.5/0.9μs
100	±9	AH2114 (Sw. 1)	15V TTL	±15	35/600 ns
		(Sw. 2)			1.2μs/50 ns
Triple SPDT					
280	±7.5	CD4053	CMOS	±7.5	150/150 ns
Dual DPST					
10	±10	AH0140/DG140	TTL	−18, 12	0.8/1.1μs
30	±10	AH0129/DG129	TTL	−18, 12	0.5/0.9μs
80	±10	AH0126/DG126	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0153/DG153	TTL	±15	0.8/1.1μs
50	±7.5	AH0154/DG154	TTL	±15	0.5/0.9μs
200-600	±10	AH0019	TTL	−20, 10, 5	100/400 ns
Dual DPDT					
10	±10	AH0145/DG145	TTL	−18, 12	0.8/1.1μs
30	±10	AH0139/DG139	TTL	−18, 12	0.5/0.9μs
80	±10	AH0142/DG142	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0163/DG163	TTL	±15	0.8/1.1μs
50	±7.5	AH0164/DG164	TTL	±15	0.5/0.9μs
200-600	±10	AH0014	TTL	−20, 10, 5	350/400 ns

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
MULTIPLEXERS					
4-Channel Differential					
280	±7.5	CD4052	CMOS	±7.5	150/150 ns
*350	12,−15	LF11509	TTL	±15	1/0.2μs
270	±7.5	CD4529B	CMOS	±7.5	50/50 ns
6-Channel					
250-1500	50 mA	AM2009/MM4504/ MM5504	TTL	−15, 5	
8-Channel					
250-400	±5	AM3705	TTL	−15, 5	300/600 ns
*350	12,−15	LF11508	TTL	±15	1/0.2μs
270	±7.5	CD4529B	CMOS	±7.5	50/50 ns
280	±7.5	CD4051	CMOS	±7.5	150/150 ns

Notes:

R_{ON} max @ $T_A = 25°C$.

V_A/I = maximum voltage or current to be safely switched.

Part number = basic number/alternate number (i.e., AM181/DG181). May be ordered by either number.

*Preferred devices.

AM, AH5 Series data sheets may be found in the *FET Data Book*.

LF Series products are to be found in the *Linear Data Book*.

CD Series data sheets are in the *CMOS Data Book*.

Analog Switches Cross Reference Guide

DEVICE NUMBER	TYPE/R_{ON}/V_A/V_S	NATIONAL PIN-FOR-PIN	FUNCTIONAL EQUIVALENT
Analog Devices			
AD7516	4-SPST/280Ω/±7.5V/±7.5V	CD4066	
Fairchild			
F4016	4-SPST/800Ω/±7.5V/±7.5V	CD4016	
F4051	8-Ch. MUX/280Ω/±7.5V/±7.5V	CD4051	
F4052	4-Ch. MUX/280Ω/±7.5V/±7.5V	CD4052	
F4053	3-SPDT/280Ω/±7.5V/±7.5V	CD4053	
F4066	4-SPST/280Ω/±7.5V/±7.5V	CD4066	
Harris			
HD4051	8-Ch MUX/280Ω/±7.5V/±7.5V	CD4051	
HD4052	4-Ch MUX/280Ω/±7.5V/±7.5V	CD4052	
HD4053	3 SPDT/280Ω/±7.5V/±7.5V	CD4053	
HD4066	4-SPST/280Ω/±7.5V/±7.5V	CD4066	
Intersil			
DG126/DG426	2-DPST/80Ω/±10V/–18V,12V	AH0126	
DG129/DG429	2-DPST/30Ω/±10V/–18V,12V	AH0129	
DG133/DG433	2-SPST/30Ω/±10V/–18V,12V	AH0133	
DG134/DG434	2-SPST/80Ω/±10V/–18V,12V	AH0134	
DG139/DG439	DPDT/30Ω/±10V/±15V	AH0139	
DG140/DG440	2-DPST/10Ω/±10V/–18V,12V	AH0140	
DG141/DG441	2-SPST/10Ω/±10V/–18V,12V	AH0141	
DG142/DG442	DPDT/80Ω/±10V/–18V,12V	AH0142	
DG143/DG443	SPDT/80Ω/±10V/–18V,12V	AH0143	
DG144/DG444	SPDT/30Ω/±10V/–18V,12V	AH0144	
DG145/DG445	2-DPST/10Ω/±10V/–18V,12V	AH0145	
DG146/DG446	SPDT/10Ω/±10V/–18V,12V	AH0146	
DG151/DG451	2-SPST/15Ω/±7.5V/±15V	AH0151	
DG152/DG452	2-SPST/50Ω/±7.5V/±15V	AH0152	
DG153/DG453	2-DPST/10Ω/±7.5V/±15V	AH0153	
DG154/DG454	2-DPST/50Ω/±7.5V/±15V	AH0154	
DG161/DG461	SPDT/15Ω/±7.5V/±15V	AH0161	
DG162/DG462	SPDT/50Ω/±7.5V/±15V	AH0162	
DG163/DG463	DPDT/15Ω/±7.5V/±15V	AH0163	
DG164/DG464	DPDT/50Ω/±7.5V/±15V	AH0164	
DG172	4-SPST/200–600Ω/±10V/–20V, 10V, 5V		AH0015
IH5001	SPST/30Ω/±8V/–18V,12V		1/2AH0133
IH5002	SPST/50Ω/±8V/–18V,12V		1/2AH0133
IH5003	2-SPST/30Ω/±10V/–18V,12V		AH0133
IH5004	2-SPST/50Ω/±10V/–18V,12V		AH0134
IH5005	2-SPST/10Ω/±10V/–18V,12V		AH0141
IH5006	2-SPST/30Ω/±10V/–18V,12V		AH0133
IH5007	2-SPST/80Ω/±10V/–18V,12V		AH0134
MM450/MM550	2-DPDT/200–600Ω/±10V	MM450/MM550	
MM451/MM551	4-Ch. MUX/200–600Ω/±10V	MM451/MM551	
MM452/MM552	4-SPST/200–600Ω/±10V	MM452/MM552	
MM455/MM555	3-SPST/200–600Ω/±10V	MM455/MM555	
DG508	8-Ch. MUX/450Ω/*/±15V	LF11508	
DG509	4-Ch. Diff. MUX/450Ω/*/±15V	LF11509	
IH5060	16-Ch. MUX/400Ω/*/±15V	LF11506	
IH5070	8-Ch. Diff. MUX/400Ω/*/±15V	LF11507	
Motorola			
MC14016	4-SPST/400Ω/±7.5V/±7.5V	CD4016	
MC14051	8-Ch. MUX/280Ω/±7.5V/±7.5V	CD4051	
MC14052	4-Ch. MUX/280Ω/±7.5V/±7.5V	CD4052	
MC14053	3-SPDT/280Ω/±7.5V/±7.5V	CD4053	
MC14066	4-SPDT/280Ω/±7.5V/±7.5V	CD4066	
MC14529	4-Ch. MUX/270Ω/±7.5V/±7.5V		CD4051

*Denotes items which have a maximum analog voltage of ±15V, the National equivalent devices have ±10V maximum analog voltage.

Analog Switches Cross Reference Guide

DEVICE NUMBER	TYPE/R_{ON}/V_A/V_S	NATIONAL PIN-FOR-PIN	FUNCTIONAL EQUIVALENT
RCA			
CD4016	4-SPST/850Ω/±7.5V/±7.5V	CD4016	
CD4051	8-Ch. MUX/280Ω/±7.5V/±7.5V	CD4051	
CD4052	4-Ch. MUX/280Ω/±7.5V/±7.5V	CD4052	
CD4053	3-SPDT/280Ω/±7.5V/±7.5V	CD4053	
CD4066	4-SPST/280Ω/±7.5V/±7.5V	CD4066	
Siliconix			
DG126	2-DPST/80Ω/±10V/−18V,12V	AH0126	
DG129	2-DPST/30Ω/±10V/−18V,12V	AH0129	
DG133	2-SPST/30Ω/±10V/−18V,12V	AH0133	
DG134	2-SPST/80Ω/±10V/−18V,12V	AH0134	
DG139	DPDT/30Ω/±10V/±15V	AH0139	
DG140	2-DPST/10Ω/±10V/−18V,12V	AH0140	
DG141	2-SPST/10Ω/±10V/ 18V,12V	AH0141	
DG142	DPDT/80Ω/±10V/−18V,12V	AH0142	
DG143	SPDT/80Ω/±10V/−18V,12V	AH0143	
DG144	SPDT/30Ω/±10V/−18V,12V	AH0144	
DG145	2-DPST/10Ω/±10V/−18V,12V	AH0145	
DG146	SPDT/10Ω/±10V/−18V,12V	AH0146	
DG151	2-SPST/15Ω/±7.5V/±15V	AH0151	
DG152	2-SPST/50Ω/±7.5V/±15V	AH0152	
DG153	2-DPST/10Ω/±7.5V/±15V	AH0153	
DG154	2-DPST/50Ω/±7.5V/±15V	AH0154	
DG161	SPDT/15Ω/±7.5V/±15V	AH0161	
DG162	SPDT/50Ω/±7.5V/±15V	AH0162	
DG163	DPDT/15Ω/±7.5V/±15V	AH0163	
DG164	DPDT/50Ω/±7.5V/±15V	AH0164	
DG172	4-SPST/200–600Ω/±10V/–20V, 10V,5V		AH0015
DG173	DPDT/150–500Ω/±10V/–20V 10V,5V	AH0014	
DG201	4-SPST/100Ω/*/±15V	LF11201	
DG501	8-Ch. MUX/200–800Ω/±5V/–15V,5V		AM3705
DG511	4-Ch. Diff. MUX/200–700Ω/±10V/ –20V, 10V		MM454/MM554

DEVICE NUMBER	TYPE/R_{ON}/V_A/V_S	NATIONAL PIN-FOR-PIN	FUNCTIONAL EQUIVALENT
DG506	16-Ch. MUX/400Ω/*/±15V	LF11506	
DG507	8-Ch. Diff. MUX/400Ω/*/±15V	LF11507	
DG508	8-Ch. MUX/400Ω/*/±15V	LF11508	
DG509	4-Ch. Diff. MUX/400Ω/*/±15V	LF11509	
DGM122	2-DPST/100–500Ω/±10V/–20V, 10V,5V		AH0019
SI455/SI555	3-SPST/200–600Ω/±10V/–20V, 10V,5V		MM455/MM555
Solitron			
CM4016	4-SPST/400Ω/±7.5V/±7.5V	CD4016	
CM4051	8-Ch. MUX/280Ω/±7.5V/±7.5V	CD4051	
CM4052	4-Ch. MUX/280Ω/±7.5V/±7.5V	CD4052	
CM4053	3-SPDT/280Ω/±7.5V/±7.5V	CD4053	
CM4116	4-SPST/800Ω/±7.5V/±7.5V	CD4016	
Teledyne—Crystalonics			
CAG-13	2-SPST/50Ω/±10V/–18V,15V		AH0134
CAG-21	2-DPST/30Ω/–6V,10V/–18V,15V		AH0129
CAG-22	2-SPST/30Ω/–6V,10V/–18V,15V		AH0133
CAG-23	2-SPST/50Ω/±10V/–18V,15V		AH0134
CAG-24	2-SPST/30Ω/–6V,10V/–18V,15V		AH0133
CAG-27-10	2-SPST/10Ω/–6V,10V/–18V,15V		AH0141
CAG-30	SPST/60Ω/±10V/±15V,5V		1/2AM182
CAG-42	2-SPST/60Ω/±10V/–18V,15V		AH0134
CAG-45	2-SPST/60Ω/±10V/–18V,15V		AH0134
CAG-48	2-SPST/60Ω/±10V/–18V,15V		AH0134
CD4066	4-SPST/280Ω/±7.5V/±7.5V	CD4066	
CS4R	2-DPST/15Ω/±10V/–18V,15V		AH0140
Texas Instruments			
TF4016	4-SPST/400Ω/±7.5V/±7.5V	CD4016	
TF4051	8-Ch. MUX/280Ω/±7.5V/±7.5V	CD4051	
TF4052	4-Ch. MUX/280Ω/±7.5V/±7.5V	CD4052	
TF4053	3-SPDT/280Ω/±7.5V/±7.5V	CD4053	

National Semiconductor

AH0014/AH0014C DPDT, AH0015/AH0015C Quad SPST, AH0019/AH0019C Dual DPST-TTL/DTL Compatible MOS Analog Switches

General Description

This series of TTL/DTL compatible MOS analog switches feature high speed with internal level shifting and driving. The package contains two monolithic integrated circuit chips: the MOS analog chip is similar to the MM450 type which consists of four MOS analog switch transistors; the second chip is a bipolar I.C. gate and level shifter. The series is available in hermetic dual-in-line package.

Features

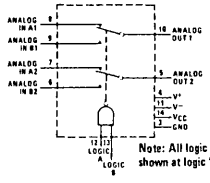
- Large analog voltage switching ±10V
- Fast switching speed 500ns
- Operation over wide range of power supplies
- Low ON resistance 200Ω
- High OFF resistance $10^{11}\Omega$
- Analog signals in excess of 25MHz
- Fully compatible with DTL or TTL logic
- Includes gating and level shifting

These switches are particularly suited for use in both military and industrial applications such as commutators in data acquisition systems, multiplexers, A/D and D/A converters, long time constant integrators, sample and hold circuits, modulators/demodulators, and other analog signal switching applications.

The AH0014, AH0015 and AH0019 are specified for operation over the −55°C to +125°C military temperature range. The AH0014C, AH0015C and AH0019C are specified for operation over the −25°C to +85°C temperature range.

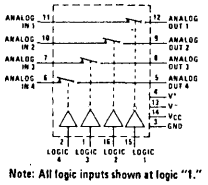
8

Block and Connection Diagrams



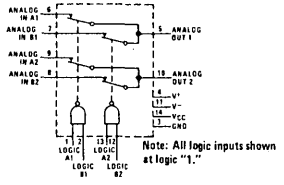
Order Number AH0014D or AH0014CD
See Package D14D

Quad SPST



Order Number AH0015D or AH0015CD
See Package D16C

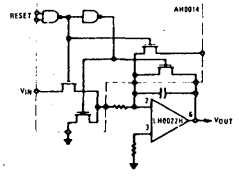
Dual DPST



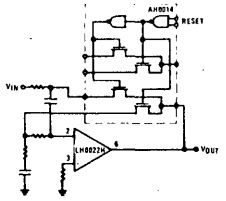
Order Number AH0019D or AH0019CD
See Package D14D

Typical Applications

Integrator



Reset Stabilized Amplifier



*Previously called NH0014/NH0014C and NH0019/NH0019C

Absolute Maximum Ratings

V_{CC} Supply Voltage	7.0V
V^- Supply Voltage	−30V
V^+ Supply Voltage	+30V
V^+/V^- Voltage Differential	40V
Logic Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AH0014, AH0015, AH0019	−55°C to +125°C
AH0014C, AH0015C, AH0019C	−25°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.5V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 2.4V			5	μA
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			1	μA
Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 0.4V		0.2	0.4	mA
Power Supply Current Logical "1" Input – each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "0" Input – each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 0V				
AH0014, AH0014C			1.5	3.0	mA
AH0015, AH0015C			0.22	0.41	mA
AH0019, AH0019C			0.22	0.41	mA
Analog Switch ON Resistance – each gate	V_{IN} (Analog) = +10V		75	200	Ω
	V_{IN} (Analog) = −10V		150	600	Ω
Analog Switch OFF Resistance			10^{11}		Ω
Analog Switch Input Leakage Current – each input (Note 4)	V_{IN} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		25	200	pA
	T_A = 125°C		25	200	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.1	10	nA
	T_A = 70°C		30	100	nA
Analog Switch Output Leakage Current – each output (Note 4)	V_{OUT} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		40	400	pA
	T_A = 125°C		40	400	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.05	10	nA
	T_A = 70°C		4	50	nA
Analog Input (Drain) Capacitance	1 MHz @ Zero Bias		8	10	pF
Output Source Capacitance	1 MHz @ Zero Bias		11	13	pF
Analog Turn-OFF Time – t_{OFF}	See test circuit; T_A = 25°C		600	750	ns
Analog Turn-ON Time – t_{ON}	See test circuit; T_A = 25°C				
AH0014, AH0014C			350	425	ns
AH0015, AH0015C			100	150	ns
AH0019, AH0019C			100	150	ns

Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for AH0014, AH0015, AH0019 and −25°C to +85°C for AH0014C, AH0015C, AH0019C. V^- = −20V. V^+ = +10V and an analog test current of 1 mA unless otherwise specified.

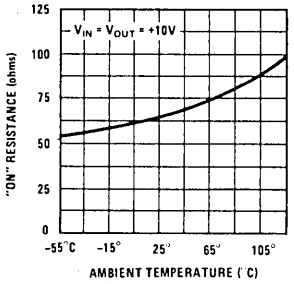
Note 2: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V. V^+ = +10V, V^- = −22V.

Note 3: Current measured is drawn from V_{CC} supply.

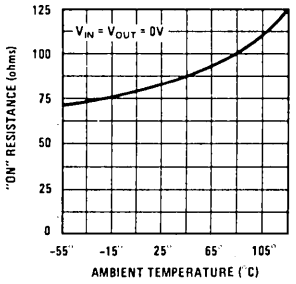
Note 4: All analog switch pins except measurement pin are tied to V^+.

Analog Switch Characteristics (Note 2)

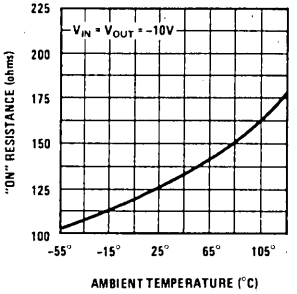
R_{ON} vs Temperature



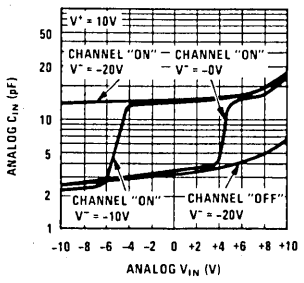
R_{ON} vs Temperature



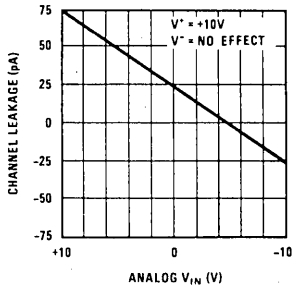
R_{ON} vs Temperature



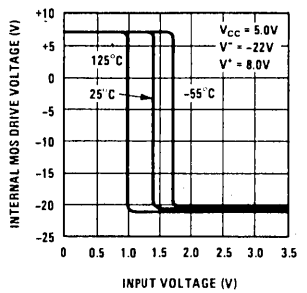
C_{IN} vs V_{IN}



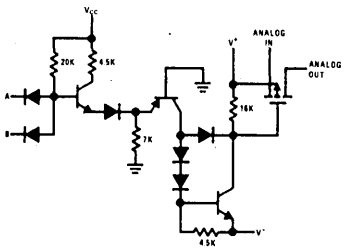
Leakage vs V_{IN} (Channel "OFF")



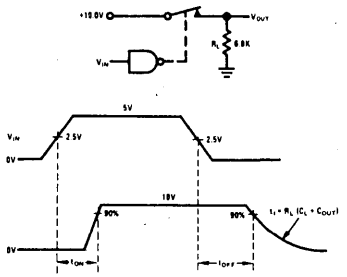
Driver Gate V_{IN} vs V_{OUT}



Schematic (Single Driver Gate and MOS Switch Shown)

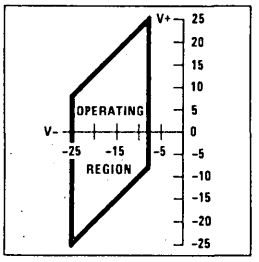


Analog Switching Time Test Circuit



Selecting Power Supply Voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V^- is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V^+ is governed by supply V^-. With a value chosen for V^-, V^+ may be selected as any value along a vertical line passing through the V^- value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



National Semiconductor

AH0120/AH0130/AH0140/AH0150/AH0160 Series Analog Switches

General Description

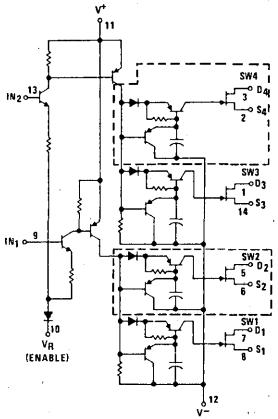
The AH0100 series represents a complete family of junction FET analog switches. The inherent flexibility of the family allows the designer to tailor the device selection to the particular application. Switch configurations available include dual DPST, dual SPST, DPDT, and SPDT. $r_{ds(ON)}$ ranges from 10 ohms through 100 ohms. The series is available in both 14-lead and 14-lead cavity DIP. Important design features include:

- TTL/DTL and RTL compatible logic inputs
- Up to 20 V_{P-P} analog input signal
- $r_{ds(ON)}$ less than 10Ω (AH0140, AH0141, AH0145, AH0146)
- Analog signals in excess of 40 MHz
- "OFF" power less than 1 mW
- Gate to drain bleed resistors eliminated
- Fast switching, t_{ON} is typically 0.4 μs, t_{OFF} is 1.0 μs
- Operation from standard op amp supply voltages, ± 15V, available (AH0150/AH0160 series)
- Pin compatible with the popular DG 100 series

The AH0100 series is designed to fulfill a wide variety of analog switching applications including commutators, multiplexers, D/A converters, sample and hold circuits, and modulators/demodulators. The AH0100 series is guaranteed over the temperature range −55°C to +125°C; whereas, the AH0100C series is guaranteed over the temperature range −25°C to +85°C

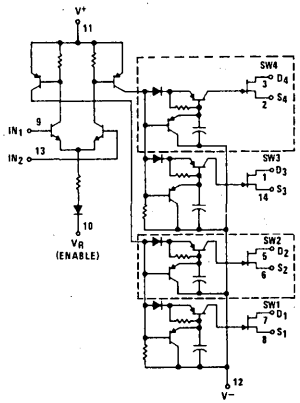
Schematic Diagrams

DUAL DPST and DUAL SPST



Note: Dotted line portions are not applicable to the dual SPST.

DPDT (diff.) and SPDT (diff.)

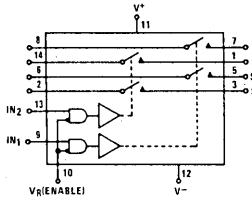


Note: Dotted line portions are not applicable to the SPDT (differential).

Order any of the devices below using the part number with a D suffix. See Package D14C. Additionally, AH0133C, AH0134C, AH0151C, and AH0152C are available with N suffix. See Package N14A.

Logic and Connection Diagrams

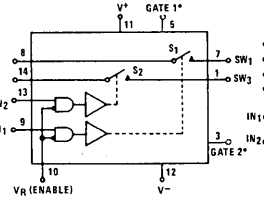
DUAL DPST



HIGH LEVEL (±10V)
AH0140 (10Ω)
AH0129 (30Ω)
AH0126 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0153 (15Ω)
AH0154 (50Ω)

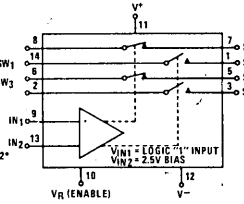
DUAL SPST
* Pinned out in N Package only.



HIGH LEVEL (±10V)
AH0141 (10Ω)
AH0133 (30Ω)
AH0134 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0151 (15Ω)
AH0152 (50Ω)

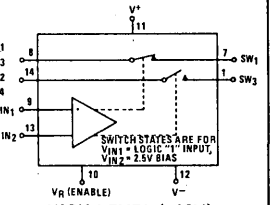
DPDT (diff.)



HIGH LEVEL (±10V)
AH0145 (10Ω)
AH0139 (30Ω)
AH0142 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0163 (15Ω)
AH0164 (50Ω)

SPDT (diff.)



HIGH LEVEL (±10V)
AH0146 (10Ω)
AH0144 (30Ω)
AH0143 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0161 (15Ω)
AH0162 (50Ω)

Absolute Maximum Ratings

	High Level	Medium Level
Total Supply Voltage ($V^+ - V^-$)	36V	34V
Analog Signal Voltage ($V^+ - V_A$ or $V_A - V^-$)	30V	25V
Positive Supply Voltage to Reference ($V^+ - V_R$)	25V	25V
Negative Supply Voltage to Reference ($V_R - V^-$)	22V	22V
Positive Supply Voltage to Input ($V^+ - V_{IN}$)	25V	25V
Input Voltage to Reference ($V_{IN} - V_R$)	±6V	±6V
Differential Input Voltage ($V_{IN} - V_{IN2}$)	±6V	±6V
Input Current, Any Terminal	30 mA	30 mA
Power Dissipation	See Curve	
Operating Temperature Range AH0100 Series	−55°C to +125°C	
AH0100C Series	−25°C to +85°C	
Storage Temperature Range	−65°C to +150°C	
Lead Temperature (Soldering, 10 sec)	300°C	

Electrical Characteristics for "HIGH LEVEL" Switches (Note 1)

PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DPDT (DIFF)	SPDT (DIFF)	$V^+ = 12.0V$, $V^- = -18.0V$, $V_R = 0.0V$		TYP	MAX	
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	$T_A = 25°C$	2.0	60	µA
							Over Temp. Range		120	µA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	$T_A = 25°C$	.01	.1	µA
							Over Temp. Range		2.0	µA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	−1.0	−1.8	mA
							Over Temp. Range		−2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	−1.0	−1.4	mA
							Over Temp. Range		−1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	1.0	10	µA
							Over Temp. Range		25	µA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	−1.0	−10	µA
							Over Temp. Range		−25	µA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	−1.0	−10	µA
							Over Temp. Range		−25	µA
Switch ON Resistance	$r_{ds(ON)}$	AH0126	AH0134	AH0142	AH0143	$V_D = 10V$ $I_D = 1$ mA	$T_A = 25°C$	45	80	Ω
							Over Temp. Range		150	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0129	AH0133	AH0139	AH0144	$V_D = 10V$ $I_D = 1$ mA	$T_A = 25°C$	25	30	Ω
							Over Temp. Range		60	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0140	AH0141	AH0145	AH0146	$V_D = 10V$ $I_F = 1$ mA	$T_A = 25°C$	8	10	Ω
							Over Temp. Range		20	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -10V$	$T_A = 25°C$	.01	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	$V_{DS} = ±20V$	$T_A = 25°C$	0.8	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0140	AH0141	AH0145	AH0146	$V_{DS} = ±20V$	$T_A = 25°C$	4	10	nA
							Over Temp. Range		1.0	µA
Switch Turn-ON Time	t_{ON}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		0.5	0.8	µs
Switch Turn-ON Time	t_{ON}	AH0140	AH0141	AH0145	AH0146	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		0.8	1.0	µs
Switch Turn-OFF Time	t_{OFF}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		0.9	1.6	µs
Switch Turn-OFF Time	t_{OFF}	AH0140	AH0141	AH0145	AH0146	See Test Circuit $V_A = ±10V$ $T_A = 25°C$		1.1	2.5	µs

Note 1: Unless otherwise specified these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

Electrical Characteristics for "MEDIUM LEVEL" Switches (Note 1)

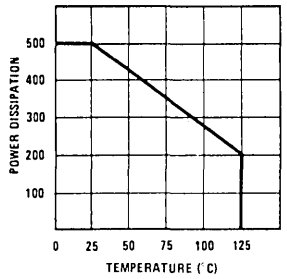
PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DUAL DPDT	SPDT (DIFF)	$V^+ = +15.0V$, $V^- = -15V$, $V_R = 0V$		TYP	MAX	
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	$T_A = 25°C$	20	60	µA
							Over Temp. Range		120	µA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	$T_A = 25°C$	.01	0.1	µA
							Over Temp. Range		2	µA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.8	mA
							Over Temp. Range		-2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.4	mA
							Over Temp. Range		-1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	1.0	10	µA
							Over Temp. Range		25	µA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	-1.0	-10	µA
							Over Temp. Range		-25	µA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				V_{IN1} V_{IN2} 0.8V	$T_A = 25°C$	-1.0	-10	µA
							Over Temp. Range		-25	µA
Switch ON Resistance	$r_{ds(ON)}$	AH0153	AH0151	AH0163	AH0161	$V_D = 7.5V$, $I_D = 1$ mA	$T_A = 25°C$	10	15	Ω
							Over Temp. Range		30	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0154	AH0152	AH0164	AH0162	$V_D = 7.5V$, $I_D = 1$ mA	$T_A = 25°C$	45	50	Ω
							Over Temp. Range		100	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -7.5V$	$T_A = 25°C$	.01	2	nA
							Over Temp. Range		500	nA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0153	AH0151	AH0163	AH0161	$V_{DS} = \pm 15V$	$T_A = 25°C$	5	10	nA
							Over Temp. Range		1.0	µA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0154	AH0152	AH0164	AH0162	$V_{DS} = \pm 15.0V$	$T_A = 25°C$	1.0	2.0	nA
							Over Temp. Range		200	nA
Switch Turn-ON Time	t_{ON}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.8	1.0	µs
Switch Turn-ON Time	t_{ON}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.5	0.8	µs
Switch Turn-OFF Time	t_{OFF}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		1.1	2.5	µs
Switch Turn-OFF Time	t_{OFF}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.9	1.5	µs

Note 1: Unless otherwise specified, these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

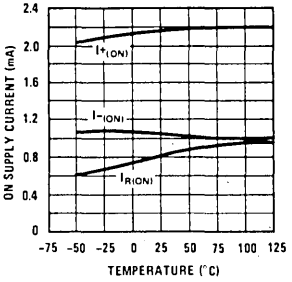
Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

Typical Performance Characteristics

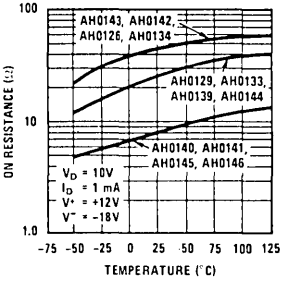
Power Dissipation vs Temperature



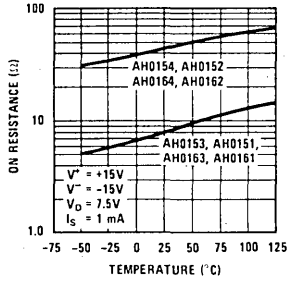
ON Supply Current vs Temperature



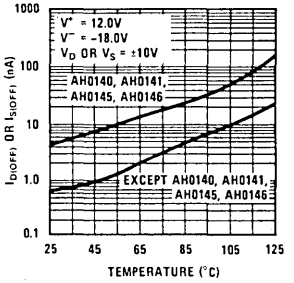
$r_{ds(ON)}$ vs Temperature AH0120 thru AH0140 Series



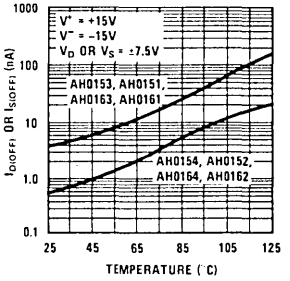
$r_{ds(ON)}$ vs Temperature AH0150/AH0160 Series



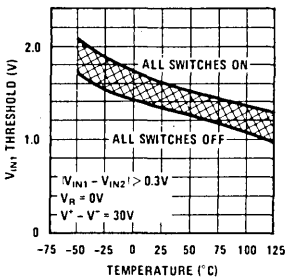
Leakage Current vs Temperature AH0120, AH0130, & AH0140



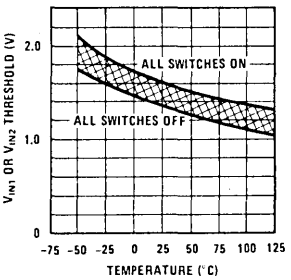
Leakage Current vs Temperature AH0150 & AH0160



Single Ended Switch Input Threshold vs Temperature

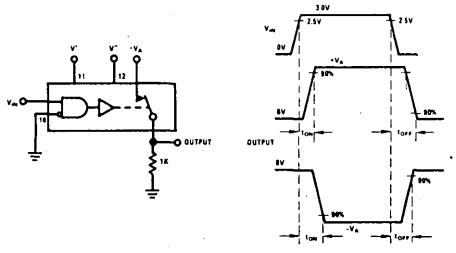


Differential Switch Input Threshold vs Temperature

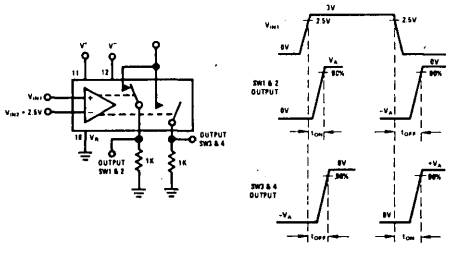


Switching Time Test Circuits

Single Ended Input



Differential Input



Applications Information

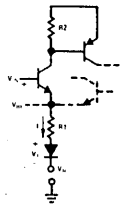
1. INPUT LOGIC COMPATIBILITY

A. Voltage Considerations

In general, the AH0100 series is compatible with most DTL, TTL, and RTL logic families. The ON-input threshold is determined by the V_{BE} of the input transistor plus the V_f of the diode in the emitter leg, plus I x R_1, plus V_R. At room temperature and V_R = 0V, the nominal ON threshold is: 0.7V+0.7V+0.2V, = 1.6V. Over temperature and manufacturing tolerances, the threshold may be as high as 2.5V and as low as 0.8V. The rules for proper operation are:

$V_{IN} - V_R \geq 2.5V$ All switches ON

$V_{IN} - V_R \leq 0.8V$ All switches OFF



B. Input Current Considerations

$I_{IN(ON)}$, the current drawn by the driver with V_{IN} = 2.5V is typically 20 μA at 25°C and is guaranteed less than 120 μA over temperature. DTL, such as the DM930 series can supply 180 μA at logic "1" voltages in excess of 2.5V. TTL output levels are comparable at 400 μA. The DTL and TTL can drive the AH0100 series directly. However, at low temperature, DC noise margin in the logic "1" state is eroded with DTL. A pull-up resistor of 10 kΩ is recommended when using DTL over military temperature range.

If more than one driver is to be driven by a DM930 series (6K) gate, an external pull-up resistor should be added. The value is given by:

$$R_P = \frac{11}{N-1} \text{ for } N > 2$$

where:

R_P = value of the pull-up resistor in kΩ

N = number of drivers.

C. Input Slew Rate

The slew rate of the logic input must be in excess of 0.3V/μs in order to assure proper operation of the analog switch. DTL, TTL, and RTL output rise times are far in excess of the minimum slew rate requirements. Discrete logic designs, however, should include consideration of input rise time.

2. ENABLE CONTROL

The application of a positive signal at the V_R terminal will open all switches. The V_R (ENABLE) signal must be capable of rising to within 0.8V of $V_{IN(ON)}$ in the OFF state and of sinking $I_{R(ON)}$ milliamps in the ON state (at $V_{IN(ON)} - V_R >$ 2.5V). The V_R terminal can be driven from most TTL and DTL gates.

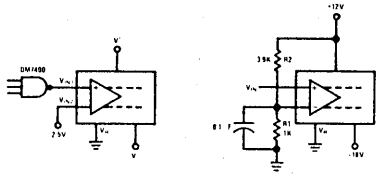
3. DIFFERENTIAL INPUT CONSIDERATIONS

The differential switch driver is essentially a differential amplifier. The input requirements for proper operation are:

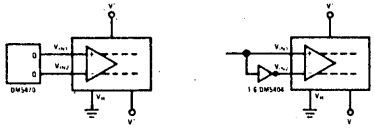
$$|V_{IN1} - V_{IN2}| \geq 0.3V$$

$$2.5 \leq (V_{IN1} \text{ or } V_{IN2}) - V_R \leq 5V$$

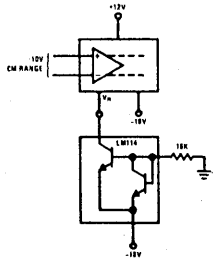
The differential driver may be furnished by a DC level as shown below. The level may be derived from a voltage divider to V^+ or the 5V V_{CC} of the DTL logic. In order to assure proper operation, the divider should be "stiff" with respect to I_{IN2}. Bypassing R1 with a 0.1 μF disc capacitor will prevent degradation of t_{ON} and t_{OFF}.



Alternatively, the differential driver may be driven from a TTL flip-flop or inverter.



Connection of a 1 mA current source between V_R and V^- will allow operation over a ±10V common mode range. Differential input voltage must be less than the 6V breakdown, and input threshold of 2.5V and 300mV differential overdrive still prevail.



4. ANALOG VOLTAGE CONSIDERATIONS

The rules for operating the AH0100 series at supply voltages other than those specified essentially breakdown into OFF and ON considerations. The OFF considerations are dictated by the maximum negative swing of the analog signal and the pinch off of the JFET switch. In the OFF state, the gate of the FET is at $V^- + V_{BE} + V_{SAT}$ or about 1.0V above the V^- potential. The maximum V_P of the FET switches is 7V. The most negative analog voltage, V_A, swing which can be accomodated for any given supply voltage is:

$$|V_A| \leq |V^-| - V_P - V_{BE} - V_{SAT} \text{ or}$$

$$|V_A| \leq |V^-| - 8.0 \text{ or } |V^-| \geq |V_A| + 8.0V$$

For the standard high level switches, $V_A \leq |-18| + 8 = -10V$. The value for V^+ is dictated by the maximum positive swing of the analog input voltage. Essentially the collector to base junction of the turn-on PNP must remain reversed biased for all positive value of analog input voltage. The base of the PNP is at $V^+ - V_{SAT} - V_{BE}$ or $V^+ - 1.0V$. The PNP's collector base junction should have at least 1.0V reverse bias. Hence, the most positive analog voltage swing which may be accommodated for a given value of V^+ is:

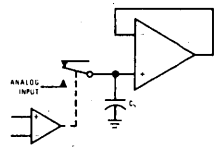
$$V_A \leq V^+ - V_{SAT} - V_{BE} - 1.0V \text{ or}$$

$$V_A \leq V^+ - 2.0V \text{ or } V^+ \geq V_A + 2.0V$$

For the standard high level switches, $V_A = 12 - 2.0V = +10V$.

5. SWITCHING TRANSIENTS

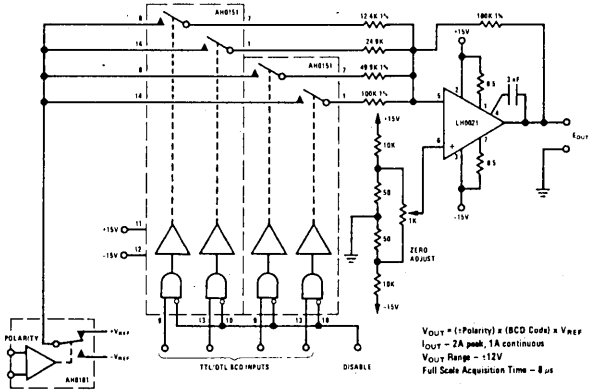
Due to charge stored in the gate-to-source and gate-to-drain capacitances of the FET switch, transients may appear in the output during switching. This is particularly true during the OFF to ON transition. The magnitude and duration of the transient may be minimized by making source and load impedance levels as small as practical.



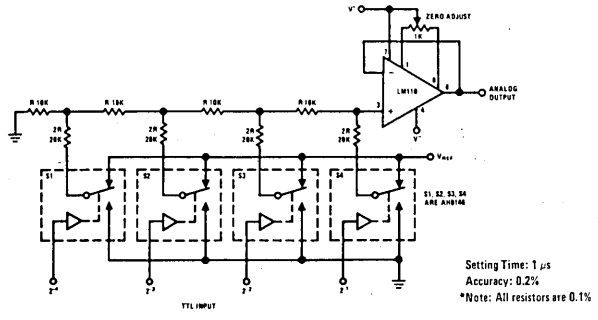
Furthermore, transients may be minimized by operating the switches in the differential mode; i.e., the charge delivered to the load during the ON to OFF transition is, to a large extent, cancelled by the OFF to ON transition.

Typical Applications

Programmable One Amp Power Supply

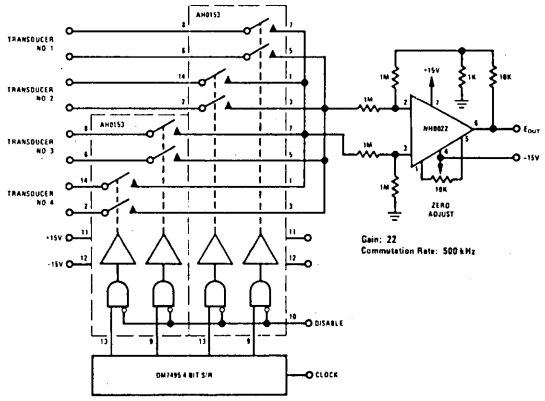


Four to Ten Bit D to A Converter (4 Bits Shown)



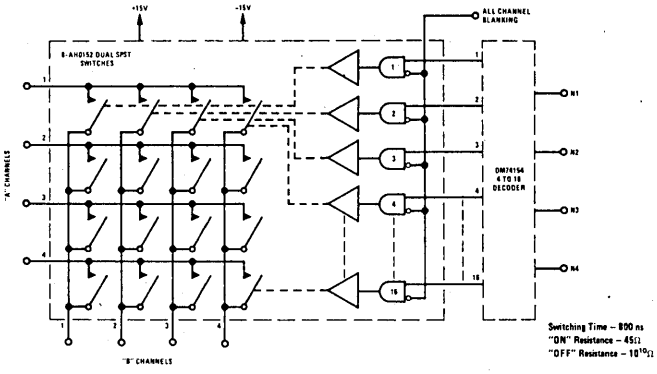
Typical Applications (Cont'd)

Four Channel Differential Transducer Commutator



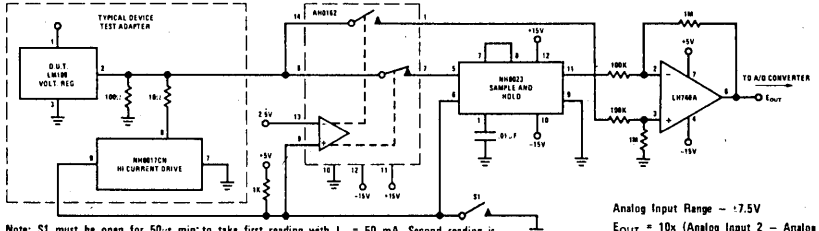
Gain: 22
Commutation Rate: 500 kHz

4 x 4 Cross Point Analog Switch



Switching Time – 800 ns
"ON" Resistance – 45Ω
"OFF" Resistance – $10^{10}\Omega$

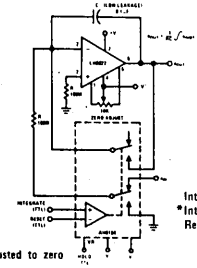
Delta Measurement System for Automatic Linear Circuit Tester



Analog Input Range – ±7.5V
E_{OUT} = 10x (Analog Input 2 – Analog Input 1)
Error Rate – 0.01% F.S./sec

Note: S1 must be open for 50μs min to take first reading with I_L = 50 mA. Second reading is taken with S2 closed. With S1 and other set-up forcing functions under computer control, system will measure line and load regulation on voltage regulators, voltage gain, offset current, CMRR and PSRR on op amps as well as other circuits requiring measurement of the change of a parameter with the change of a forcing function.

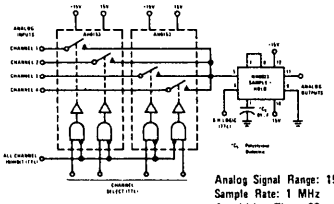
Precision Long Time Constant Integrator with Reset



Integration Internal = 10 sec
*Integration Error = 100μV
Reset Time: 30μs

*Note: V_{OS} adjusted to zero

Four Channel Commutator



Analog Signal Range: $15V_{P-P}$
Sample Rate: 1 MHz
Acquisition Time: 20μs
Drift Rate: 0.5 mV/sec

National Semiconductor

AH2114/AH2114C DPST Analog Switch

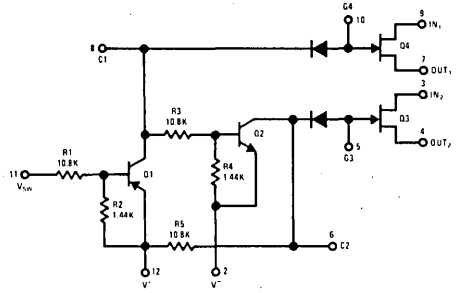
General Description

The AH2114 is a DPST analog switch circuit comprised of two junction FET switches and their associated driver. The AH2114 is designed to fulfill a wide variety of high level analog switching applications including multiplexers, A to D Converters, integrators, and choppers. Design features include:

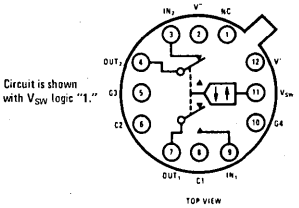
- Low ON resistance, typically 75Ω
- High OFF resistance, typically 10^{11}Ω
- Large output voltage swing, typically ± 10V
- Input signals in excess of 40 MHz
- Turn-ON and turn-OFF times typically 1 μs

The AH2114 is guaranteed over the temperature range −55°C to +125°C whereas the AH2114C is guaranteed over the temperature range 0°C to +85°C.

Schematic and Connection Diagrams

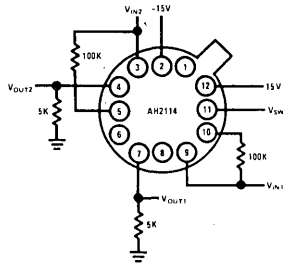


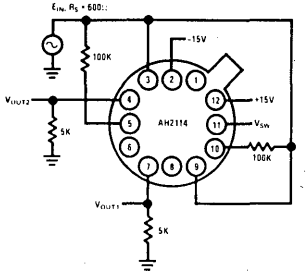
Metal Can Package

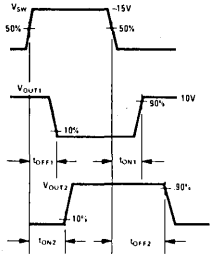


Order Number AH2114G or AH2114CG
See Package H12C

AC Test Circuit and Waveforms







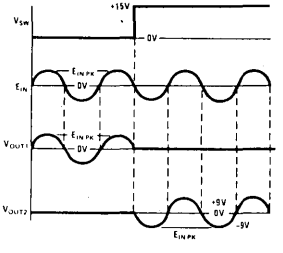


FIGURE 1.

FIGURE 2.

Absolute Maximum Ratings

Vplus Supply Voltage	+25V
Vminus Supply Voltage	-25V
Vplus--Vminus Differential Voltage	40V
Logic Input Voltage	25V
Power Dissipation (Note 3)	1.36W
Operating Temperature Range	
AH2114	-55°C to +125°C
AH2114C	0°C to +85°C
Storage Temperature Range	-65°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	AH2114			AH2114C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Static Drain-Source "On" Resistance	I_D = 1.0 mA, V_{GS} = 0V, T_A = 25°C		75	100		75	125	Ω
	I_D = 1.0 mA, V_{GS} = 0V			150			160	Ω
Drain-Gate Leakage Current	V_{DS} = 20V, V_{GS} = -7V, T_A = 25°C		0.2	1.0		0.2	5.0	nA
				60			60	nA
FET Gate-Source Breakdown Voltage	I_G = 1.0 μA, V_{DS} = 0V	35			35			V
Drain-Gate Capacitance	V_{DG} = 20V, I_S = 0, f = 1.0 MHz, T_A = 25°C		4.0	5.0		4.0	5.0	pF
Source-Gate Capacitance	V_{DG} = 20V, I_D = 0, f = 1.0 MHz, T_A = 25°C		4.0	5.0		4.0	5.0	pF
Input 1 Turn-ON Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		35	60		35	60	ns
Input 2 Turn-ON Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		1.2	1.5		1.2	1.2	μs
Input 1 Turn-OFF Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		0.6	0.75		0.6	0.75	μs
Input 2 Turn-OFF Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		50	80		50	80	ns
DC Voltage Range	T_A = 25°C (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V
AC Voltage Range	T_A = 25°C (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V

Note 1: Unless otherwise specified these specifications apply for pin 12 connected to +15V, pin 2 connected to -15V, -55°C to 125°C for the AH2114, and 0°C to 85°C for the AH2114C.

Note 2: All typical values are for T_A = 25°C.

Note 3: Derate linearly at 100°C/W above 25°C.

Section 9

MOS Clock Drivers

Section 9. MOS Clock Drivers

Features	V_{OUT} (Max)	I_{OUT} (Max)	PRF	t_{ON}	t_{OFF}	Part Number		Page Number
						−55°C to 125°C	−25°C to 85°C	
Single Phase, DC Coupled	30V	0.3A	≤ 5MHz	50ns	75ns	MH0007	MH0007	9-4
Two Phase, DC Coupled	30V	0.5A	≤ 2MHz	35ns	60ns	MH0009	MH0009C	9-6
Single Phase, DC Coupled	30V	1.0A	≤ 10MHz	15ns	50ns	MH0012	MH0012C	9-8
Two Phase, AC Coupled	30V	0.5A	≤ 2MHz	35ns	60ns	MH0013	MH0013C	9-10
Two Phase, AC Coupled	30V	0.5A	≤ 1MHz	30ns	60ns	DS0025	DS0025C	9-14
Two Phase, AC Coupled	20V	1.5A	≤ 5MHz	12ns	15ns	DS0026	DS0026C	9-17

Note: Refer to Application Note AN-76 for additional information on clock drivers. For additional interface product information, refer to the *Interface Databook*.

National Semiconductor

MH0007/MH0007C DC Coupled MOS Clock Driver

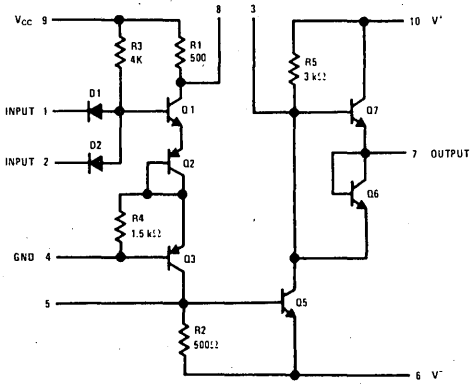
General Description

The MH0007 is a voltage translator and power booster designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with inputs or clocks of MOS FET type devices. The design allows the user a wide latitude in selection of supply voltages, and is especially useful in normally "off" applications, since power dissipation is typically only 5 milliwatts in the "off" state.

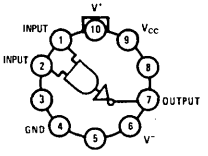
Features

- 30 volts (max) output swing
- Standard 5V power supply
- Peak currents in excess of ±300 mA available
- Compatible with all MOS devices
- High speed: 5 MHz with nominal load
- External trimming possible for increased performance

Schematic and Connection Diagrams



10 Pin TO-100 Package

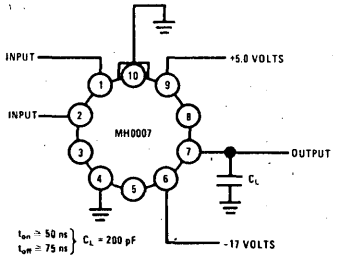


TOP VIEW

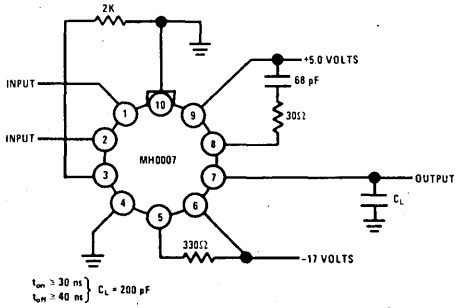
Order Number MH0007H or MH0007CH
See Package H10E

Typical Applications

Switching Time Test Configuration



High Speed Operation



Absolute Maximum Ratings

V_{CC} Supply Voltage	8V
V^- Supply Voltage	−40V
V^+ Supply Voltage	+28V
$(V^+ - V^-)$ Voltage Differential	30V
Input Voltage	5.5V
Power Dissipation (T_A = 25°C)	800 mW
Peak Output Current	±500 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range MH0007	−55°C to +125°C
MH0007C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 1)

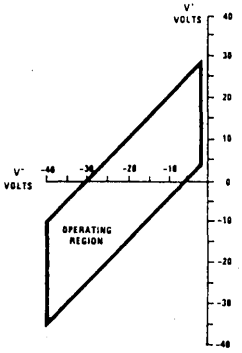
PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.5V	2.2			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			100	μA
Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V		1.0	1.5	mA
Logical "1" Output Voltage	V_{CC} = 5.5V, I_{OUT} = 30 mA, V_{IN} = 0.8V	$V^+ - 4.0$			V
	V_{CC} = 5.5V, I_{OUT} = 1 mA, V_{IN} = 0.8V	$V^+ - 2.0$			V
Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OUT} = 30 mA, V_{IN} = 2.2V			$V^- + 2.0$	V
Transition Time to Logical "0" Output	C_L = 200 pF (Note 3)		50		ns
Transition Time to Logical "1" Output	C_L = 200 pF (Note 3)		75		ns

Note 1: Min/max limits apply across the guaranteed range of −55°C to +125°C for the MH0007, and from 0°C to +85°C for the MH0007C, for all allowable values of V^- and V^+

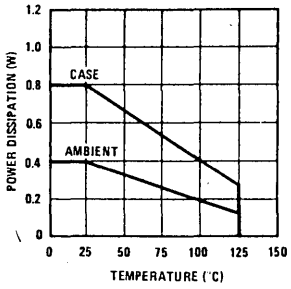
Note 2: All typical values measured at T_A = 25°C with V_{CC} = 5.0 volts, V^- = −25 volts, V^+ = 0 volts.

Note 3: Transition time measured from time V_{IN} = 50% value until V_{OUT} has reached 80% of final value.

Allowable Values for V^- and V^+



Maximum Power Dissipation



National Semiconductor

MH0009/MH0009C DC Coupled Two Phase MOS Clock Driver

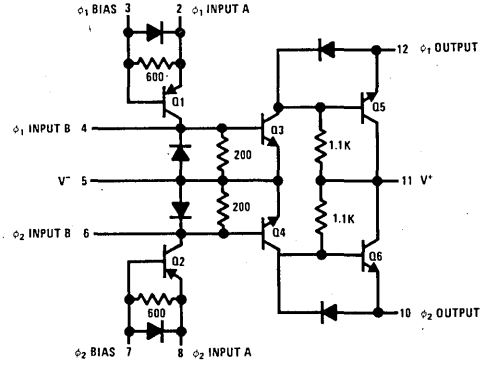
General Description

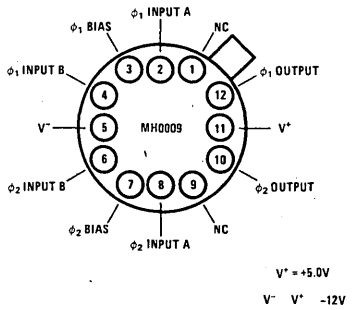
The MH0009/MH0009C is high speed, DC coupled, dual MOS clock driver designed to operate in conjunction with high speed line drivers such as the DM8830, DM7440, or DM7093. The transition from TTL/DTL to MOS logic level is accomplished by PNP input transistors which also assure accurate control of the output pulse width.

Features

- DC logically controlled operation
- Output Swings – to 30V
- Output Currents – in excess of ±500 mA
- High rep rate – in excess of 2 MHz
- Low standby power

Schematic and Connection Diagrams





Order Number MH0009G
or MH0009CG
See Package H12B

Typical Applications

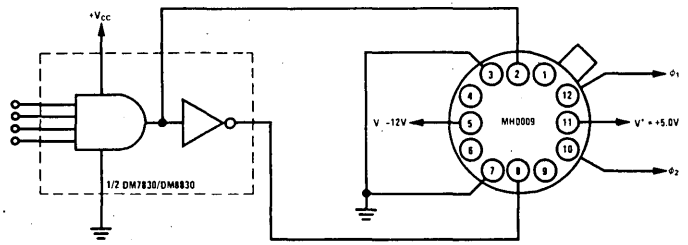


FIGURE 1

Absolute Maximum Ratings

V^- Supply Voltage: Differential (Pin 5 to Pin 3) or (Pin 5 to Pin 7)	-40V
V^+ Supply Voltage: Differential (Pin 11 to Pin 5)	30V
Input Current: (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±500 mA
Power Dissipation (Note 2 and Figure 2)	1.5W
Storage Temperature	-65°C to +150°C
Operating Temperature: MH0009	-55°C to +125°C
MH0009C	0°C to 85°C
Lead Temperature (Soldering, 10 Sec.)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ON}	C_{IN} = .0022 μF C_L = .001 μF		10	35	ns
t_{rise}	C_{IN} = .0022 μF C_L = .001 μF		40	50	ns
Pulse Width (50% to 50%)	C_{IN} = .0022 μF C_L = .001 μF	340	400	440	ns
t_{fall}	C_{IN} = .0022 μF C_L = .001 μF		80	120	ns
t_{delay}	C_{IN} = 600 pF C_L = 200 pF		10		ns
t_{rise}	C_{IN} = 600 pF C_L = 200 pF		15		ns
Pulse Width (50% to 50%)	C_{IN} = 600 pF C_L = 200 pF	40	70	120	ns
t_{fall}	C_{IN} = 600 pF C_L = 200 pF		40		ns

Note 1: Characteristics apply for circuit of Figure 1. With V^- = -20 volts; V^+ = 0 volts; V_{CC} = 5.0 volts. Minimum and maximum limits apply from -55°C to +125°C for the MH0009 and from 0°C to +85°C for the MH0009C. Typical values are for T_A = 25°C.
Note 2: Transient power is given by $P = fC_L (V^+ - V^-)^2$ watts, where: f = repetition rate, C_L = load capacitance, and $(V^+ - V^-)$ = output swing.
Note 3: For typical performance data see the MH0013/MH0013C data sheet.

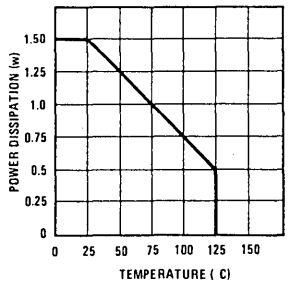


FIGURE 2. Maximum Power Dissipation

National Semiconductor

MH0012/MH0012C High Speed MOS Clock Driver

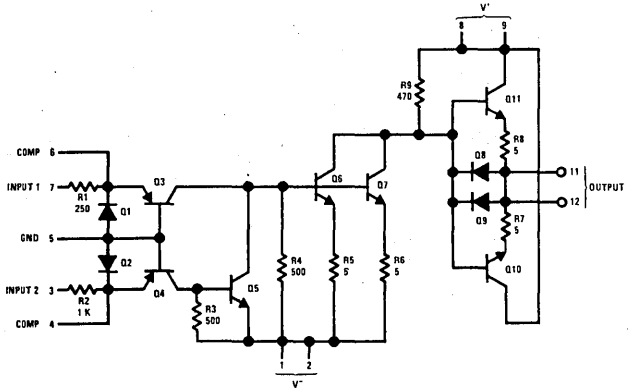
General Description

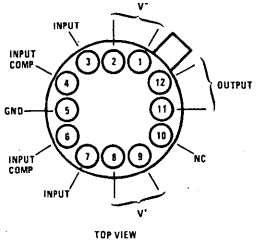
The MH0012/MH0012C is a high performance clock driver that is designed to be driven by the DM7830/DM8830 or other line drivers or buffers with high output current capability. It will provide a fixed width pulse suitable for driving MOS shift registers and other clocked MOS devices.

Features

- High output voltage swings—12 to 30 volts
- High output current drive capability—1000 mA peak
- High repetition rate—10 MHz at 18 volts into 100 pF
- Low standby power—less than 30 mW

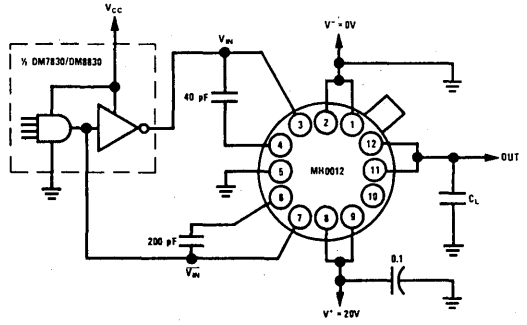
Schematic and Connection Diagrams



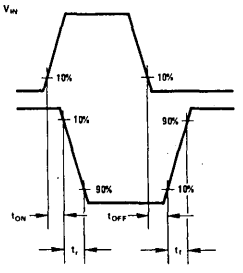


Order Number MH0012G
or MH0012CG
See Package H12B

Typical Applications (AC Test Circuit)



Timing Diagram



Absolute Maximum Ratings

V^- Supply Voltage: Differential (Pin 1 or 2 to Pin 5)	-40V
V^+ Supply Voltage: Differential (Pin 8 or 9 to Pin 1 or 2)	30V
Input Current: (Pin 3 or 7)	±75 mA
Peak Output Current	±1000 mA
Maximum Output Load - See Figure 2	
Power Dissipation - See Figure 1	1.5W
Storage Temperature	-65°C to +150°C
Operating Temperature: MH0012	-55°C to +125°C
MH0012C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

DC Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} < V^- + 2V$		1.0	2.0	V
Logic "0" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} > V^+ - 1.5V$	0.4	0.6		V
Logic "1" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = 1mA$, $V_{IN} = 2.0V$		$V^- + 1.0$	$V^- + 2.0$	V
Logic "0" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = -1mA$, $V_{IN} = 0.4V$	$V^+ - 1.5$	$V^+ - 0.7$		V
I_{DC} (V^- Supply)	$V^+ - V^- = 20V$, $V_{IN} = 2.0V$		34	60	mA

AC Electrical Characteristics

PARAMETER	CONDITIONS (Note 3)	MIN	TYP	MAX	UNITS
Turn-On Delay (t_{ON})	$V^+ - V^- = 20V$, $V_{CC} = 5.0V$ $C_L = 200$ pF, f = 1.0 MHz $T_A = 25°C$		10	15	ns
Rise Time (t_r)			5	10	ns
Turn-Off Delay (t_{OFF})			35	50	ns
Fall Time (t_f)			35	45	ns

Note 1: Characteristics apply for circuit of Figure 1. Min and max limits apply from -55°C to +125°C for the MH0012 and from 0°C to +85°C for the MH0012C. Typical values are for $T_A = 25°C$.

Note 2: Due to the very fast rise and fall times, and the high currents involved, extremely short connections and good by passing techniques are required.

Note 3: All conditions apply for each parameter.

Power Dissipation

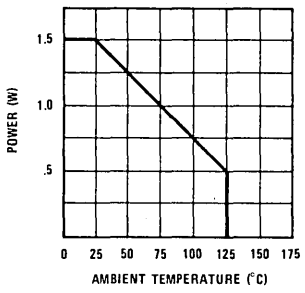


Figure 1.

Maximum Output Load vs Voltage Swing vs Rise Times

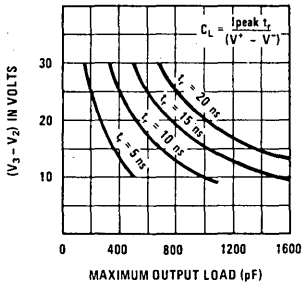
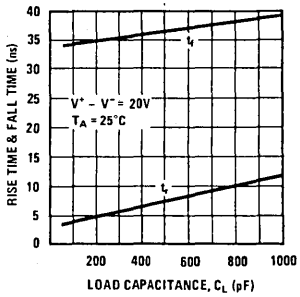


Figure 2.

Rise and Fall Times vs Load Capacitance



Applications Information

Power Dissipation Considerations

The power dissipated by the MH0012 may be divided into three areas of operation = ON, OFF and switching. The OFF power is approximately 30 mW and is dissipated by R_2 when Pin 3 is in the logic "1" state. The OFF power is neglible and will be ignored in the subsequent discussion. The ON power is dissipated primarily by Q_3 and R_9 and is given by:

$$P_{ON} \cong [V^- | I_{IN} + \frac{(V^+ - V^-)^2}{R_9}] \; DC \qquad (1)$$

Where:

$$DC = \text{Duty Cycle} = \frac{\text{ON Time}}{\text{ON Time \& OFF Time}}$$

I_{IN} is given by $\frac{V_{IN} - V_{BE3}}{R_1}$ and equation (1) becomes:

$$P_{ON} = \left[\frac{(V_{IN} - V_{BE3})|V^-|}{R_1} + \frac{(V^+ - V^-)^2}{R_9}\right] DC \qquad (2)$$

For $V_{IN} = 2.5V$, $V_{BE3} = 0.7V$, $V^+ = 0V$, $V^- = -20V$, and DC = 20%, $P_{ON} \cong 200$ mW.

The transient power incurred during switching is given by:

$$P_{AC} = (V^+ - V^-)^2 \, C_L f \qquad (3)$$

For $V^+ = 0V$, $V^- = -20V$, $C_L = 200$ pF, and f = 5.0 MHz, $P_{AC} = 400$ mW.

The total power is given by:

$$P_T = P_{AC} + P_{ON} \qquad (4)$$

$$P_T \leq P_{MAX}$$

For the above example, $P_T = 600$ mW.

National Semiconductor

MH0013/MH0013C Two Phase MOS Clock Driver

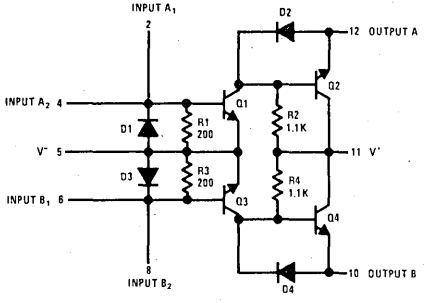
General Description

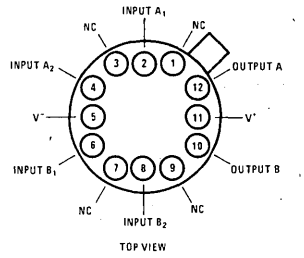
The MH0013/MH0013C is a general purpose clock driver that is designed to be driven by DTL or TTL line drivers or buffers with high output current capability. It will provide fixed width clock pulses for both high threshold and low threshold MOS devices. Two external input coupling capacitors set the pulse width maximum, below which the output pulse width will closely follow the input pulse width or logic control of output pulse width may be obtained by using larger value input capacitors and no input resistors.

Features

- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 500 mA
- High Repetition Rate—up to 5.0 MHz
- Pin Compatible with the MH0009/MH0009C
- "Zero" Quiescent Power

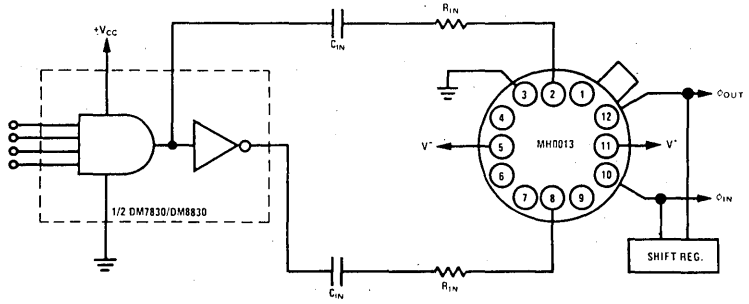
Schematic and Connection Diagrams

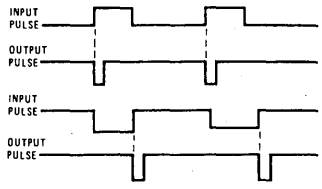




Order Number MH0013G or MH0013CG
See Package H12B

Typical Applications





Absolute Maximum Ratings

$(V^+ - V^-)$ Voltage Differential	30V
Input Current (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±600 mA
Power Dissipation (Figure 7)	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature MH0013	−55°C to +125°C
MH0013C	0°C to +85°C
Lead Temperature (Soldering, 10 sec 1/16" from Case)	300°C

Electrical Characteristics (Note 1 and Figure 8)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "0" Output Voltage	I_{OUT} = −50 mA I_{IN} = 1.0 mA	$V^+ - 3.0$	$V^+ - 1.0$		V
	I_{OUT} = −10 mA I_{IN} = 1.0 mA		$V^+ - 0.7$	$V^+ - 0.5$	V
Logical "1" Output Voltage	I_{OUT} = 50 mA I_{IN} = 10 mA		$V^- + 1.5$	$V^- + 2.0$	V
					V
Power Supply Leakage Current	$(V^+ - V^-)$ = 30V $I_{OUT} = I_{IN}$ = 0 mA		1.0	100	μA
Negative Input Voltage Clamp	I_{IN} = − 10 mA	$V^- - 1.2$	$V^- - 0.8$		V
$t_{d\,ON}$			20	35	ns
t_{rise}			35	50	ns
$t_{d\,OFF}$ (Note 2)	C_{IN} = 0.0022 μF R_{IN} = 0Ω		30	60	ns
t_{fall} (Note 2)	C_L = 0.001 μF	40	50	80	ns
t_{fall} (Note 3)		40	70	120	ns
Pulse Width (50% to 50%) (Note 3)		340	420	490	ns
t_{rise}	C_{IN} = 500 pF		15		ns
t_{fall}	R_{IN} = 0Ω		20		ns
Pulse Width (50% to 50%) (Note 3)	C_L = 200 pF		110		ns
Positive Output Voltage Swing			$V^+ - 0.7V$		V
Negative Output Voltage Swing			$V^- + 0.7V$		V

Note 1: Min/Max limits apply over guaranteed operating temperature range of −55°C to +125°C for MH0013 and 0°C to +85°C for MH0013C, with V^- = −20V and V^+ = 0V unless otherwise specified. Typical values are for 25°C.

Note 2: Parameter values apply for clock pulse width determined by input pulse width.

Note 3: Parameter values apply for input pulse width greater than output clock pulse width.

TABLE I. Typical Drive Capability of One Half MH0013 at 70°C Ambient

$(V_3 - V_2)$ VOLTS	FREQUENCY MHz	PULSE WIDTH ns	TYPICAL R_{IN} Ω	TYPICAL C_{IN} pF	OUTPUT DRIVE CAPABILITY IN pF[1]	RISE TIME LIMIT ns[2]
28					50	–
20	4.0	100	0	750	200	7
16					350	10
28					100	5
20	2.0	200	10	1600	400	14
16					700	19
28					400	19
20	1.0	200	0	2300	1000	34
16					1700	45
28					2800	130
20	0.5	500	10	4000	5500	183
16					9300	248

Note 1: Output load is the maximum load that can be driven at 70°C without exceeding the package rating under the given conditions.

Note 2: The rise time given is the minimum that can be used without exceeding the peak transient output current for the full rated output load.

Circuit Operation

Input current forced into the base of Q1 through the coupling capacitor C_{IN} causes Q1 to be driven into saturation, swinging the output to $V^- + V_{CE}(SAT) + V_{DIODE}$.

When the input current has decayed, or has been switched, such that Q1 turns off, Q2 receives base drive through R2, turning Q2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q1 always switches off before Q2 begins to supply current; hence, high internal transient currents from V^+ to V^- cannot occur.

Typical Performance Characteristics

FIGURE 1. Output Load vs Voltage Swing

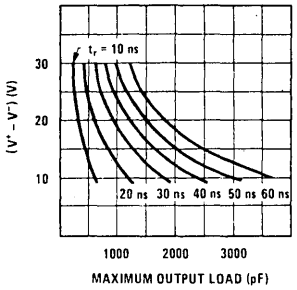


FIGURE 2. Transient Power vs Rep. Rate vs C_L

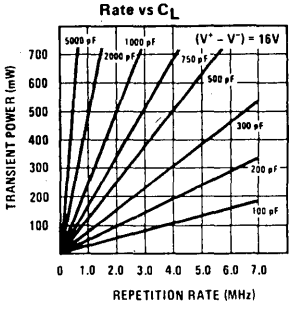


FIGURE 3. Transient Power vs Rep. Rate vs C_L

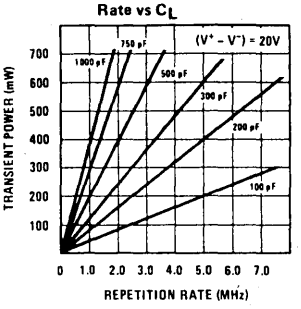


FIGURE 4. Average Internal Power vs Output Swing vs Duty Cycle

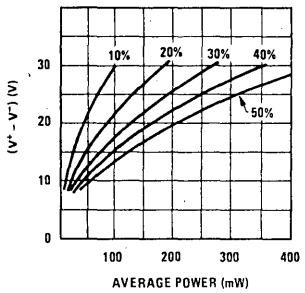


FIGURE 5. Typical Clock Pulse Variations vs Ambient Temperature

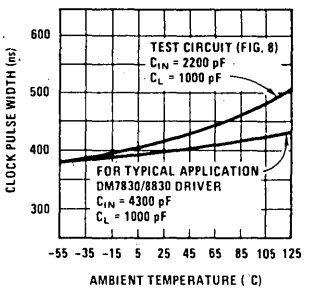


FIGURE 6. R_{IN} vs C_{IN} vs Pulse Width

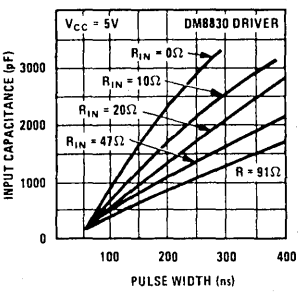
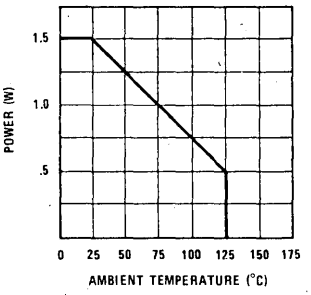
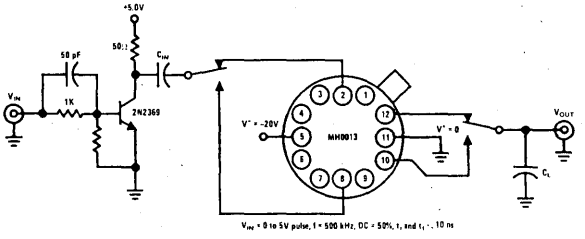


FIGURE 7. Package Power Derating



AC Test Circuit



Timing Diagram

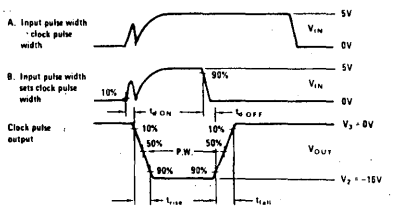


Figure 8

Pulse Width

Maximum output pulse width is a function of the input driver characteristics and the coupling capacitance and resistance. After being turned on, the input current must fall from its initial value I_{IN} peak to below the input threshold current I_{IN} min $\simeq V_{BE}/R1$ for the clock driver to turn off. For example, referring to the test circuit of Figure 8, the output pulse width, 50% to 50%, is given by

$$pw_{OUT} \cong \frac{1}{2}(t_{rise} + t_{fall})$$

$$+ R_O C_{IN} \ln \frac{I_{IN}\ peak}{I_{IN}\ min} \cong 400 \text{ ns.}$$

For operation with the input pulse shorter than the above maximum pulse width, the output pulse width will be directly determined by the input pulse width.

$$pw_{OUT} = pw_{IN} + t_{d\,OFF} + t_{d\,ON} + \frac{1}{2}(t_{fall} + t_{rise})$$

Typical maximum pulse width for various C_{IN} and R_{IN} values are given in Figure 6.

Fan-Out Calculation

The drive capability of the MH0013 is a function of system requirements, i.e., speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition. Some typical fan-outs for conditions are given in Table 1.

Transient Current

The maximum peak output current of the MH0013 is given as 600 mA. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{T_R} \qquad (1)$$

This can give a maximum limit to the load.

Figure 1 shows maximum voltage swing and capacitive load for various rise times.

1. *Transient Output Power*

The average transient power (P_{AC}) dissipated is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (F).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times F \qquad (2)$$

Figures 2 and 3 show transient power for two different values of $(V^+ - V^-)$ versus output load and frequency.

2. *Internal Power*

"0" State

Negligible (<3 mW)

"1" State

$$P_{INT} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle.} \qquad (3)$$

Figure 4 gives various values of internal power versus ouptut voltage and duty cycle.

3. *Input Power*

The average input power is a function of the input current and duty cycle. Due to input voltage clamping, this power contribution is small and can therefore be neglected. At maximum duty cycle of 50%, at 25°C, the average input power is less than 10 mW per phase for $R_{IN}C_{IN}$ controlled pulse widths. For pulse widths much shorter than $R_{IN}C_{IN}$, and maximum duty cycle of 50%, input power could be as high as 30 mW, since I_{IN} peak is maintained for the full duration of the pulse width.

4. *Package Power Dissipation*

Total Average Power = Transient Output Power + Internal Power + Input Power

Typical Example *Calculation for One Half MH0013C*

How many MM506 shift registers can be driven by an MH0013C driver at 1 MHz using a clock pulse width of 400 ns, rise time 30–50 ns and 16 volts amplitude over the temperature range 0–70°C?

Power Dissipation

From the graph of power dissipation versus temperature, Figure 7, it can be seen that an MH0013C at 70°C can dissipate 1W without a heat sink; therefore, each half can dissipate 500 mW.

Transient Peak Current Limitation

From Figure 1 (equation 1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 1140 pF.

Average Internal Power

Figure 4 (equation 3) gives an average power of 102 mW at 16V 40% duty cycle.

Input power will be a maximum of 8 mW.

Transient Output Power

For one half of the MH0013C

500 mW = 102 mW + 8 mW
+ transient output power

390 mW = transient output power

Using Figure 2 (equation 2) at 16V, 1 MHz and 390 mW, each half of the MH0013C can drive a 1520 pF load. This is, however, in excess of the load derived from the transient current limitation (Figure 1, equation 1), and so a maximum load of 1140 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is $\frac{1140}{80}$ or 14 registers.

For nonsymmetrical clock widths, drive capability is improved.

National Semiconductor

DS0025/DS0025C Two-Phase MOS Clock Driver

General Description

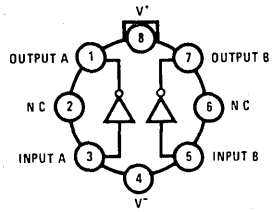
The DS0025/DS0025C is monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL/DTL line drivers or buffers such as the DM932, DS8830 or DM7440. Two input coupling capacitors are used to perform the level shift from TTL/DTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse widths may be set by selection of the input capacitors eliminating the need for tight input pulse control.

Features

- 8-lead TO-5 or 8-lead dual-in-line package
- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DM932, DS8830, DM7440 (SN7440)
- "Zero" Quiescent Power

Connection Diagrams

Metal Can Package

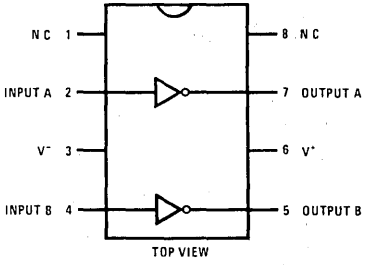


Note: Pin 4 connected to case.

TOP VIEW

Order Number DS0025H or DS0025CH
See NS Package H08C

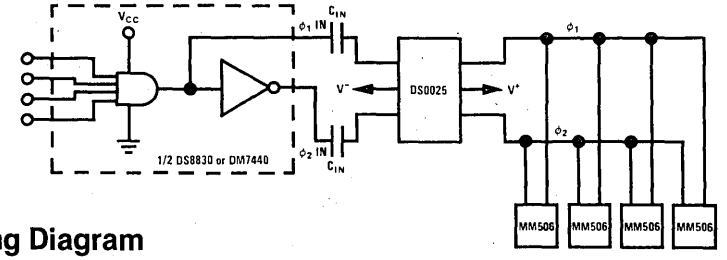
Dual-In-Line Package



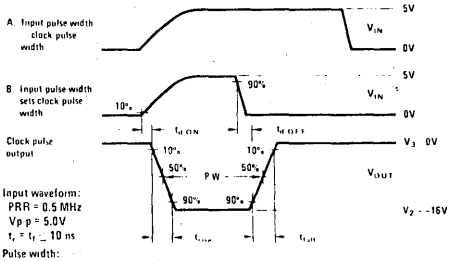
TOP VIEW

Order Number DS0025CN-8
See NS Package N08A

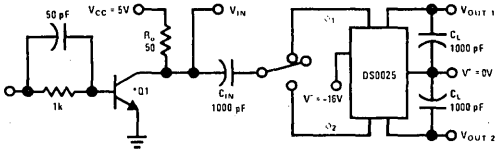
Typical Applications



Timing Diagram



AC Test Circuit



*Q1 is selected high speed NPN switching transistor.

Absolute Maximum Ratings (Note 1)

$(V^+ - V^-)$ Voltage Differential	30V
Input Current	100 mA
Peak Output Current	1.5A
Storage Temperature	−65°C to +150°C
Operating Temperature DS0025	−55°C to +125°C
DS0025C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Notes 2 and 3) See test circuit

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{dON}	Turn-On Delay Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF			15	30	ns
t_{RISE}	Rise Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF			25	50	ns
t_{dOFF}	Turn-Off Delay Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF, (Note 4)			30	60	ns
t_{FALL}	Fall Time	C_{IN} = 0.001μF, R_{IN} = 0Ω,	(Note 4)	60	90	120	ns
		C_L = 0.001μF	(Note 5)	100	150	250	ns
PW	Pulse Width (50% to 50%)	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF (Note 5)			500		ns
V_{O+}	Positive Output Voltage Swing	V_{IN} = 0V, I_{OUT} = −1 mA		V^+−1.0	V^+−0.7V		V
V_{O-}	Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA			V^-+0.7V	V^-+1.5V	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS0025 and across the 0°C to +70°C range for the DS0025C.

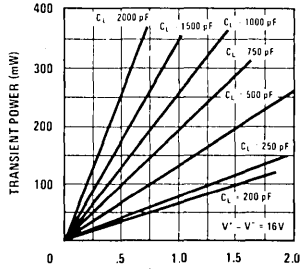
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Parameter values apply for clock pulse width determined by input pulse width.

Note 5: Parameter values for input pulse width greater than output clock pulse width.

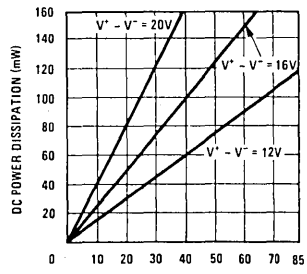
Typical Performance

Transient Power vs Rep. Rate



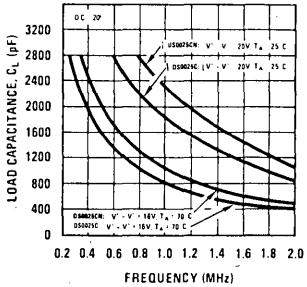
$$P_{AC} = (V^+ - V^-)^2 f C_L$$

DC Power (P_{DC}) vs Duty Cycle



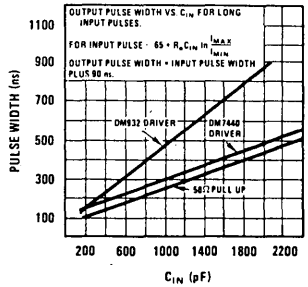
$$P_{DC} = \frac{(V^+ - V^-)^2 (DC)}{1k}$$

Maximum Load Capacitance



$$C_L \leq \frac{(P_{MAX})(1k) - (V^+ - V^-)^2 (DC)}{(f)(1k)(V^+ - V^-)^2} < \frac{(I_{pk})(t_r)}{V^+ - V^-}$$

Output PW Controlled by C_{IN}



I_{MAX} = Peak current delivered by driver

$$I_{MIN} \cong \frac{V_{BE}}{R1} = \frac{0.6}{1k}$$

Applications Information

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents from V^- to V^+ cannot occur.

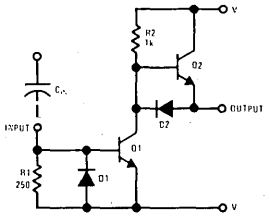


FIGURE 1. DS0025 Schematic (One-Half Circuit)

Fan-Out Calculation

The drive capability of the DS0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

Transient Current

The maximum peak output current of the DS0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{t_r} \qquad (1)$$

Typical rise times into 1000 pF load is 25 ns For $V^+ - V^- = 20V$, I = 0.8A.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \qquad (2)$$

For $V^+ - V^- = 20V$, f = 1.0 MHz, C_L = 1000 pF, P_{AC} = 400 mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

= 80 mW for $V^+ - V^- = 20V$, DC = 20%

Package Power Dissipation

Total average power = transient output power + internal power

Example Calculation

How many MM506 shift registers can be driven by a DS0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30-50 ns and 16V amplitude over the temperature range 0-70°C?

Power Dissipation:

At 70°C the DS0025CN can dissipate 870 mW when soldered into printed circuit board.

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one-half of the DS0025C, 870 mW ÷ 2 can be dissipated.

435 mW = 50 mW + transient output power

385 mW = transient output power

Using equation (2) at 16V, 1 MHz and 350 mW, each half of the DS0025CN can drive a 1367 pF load. This is less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 1367 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is 1367/80 or 17 registers.

National Semiconductor

DS0026, DS0056 5 MHz Two-Phase MOS Clock Drivers

General Description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76A.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to $(V^+ - 0.1V)$ in the off state.

For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

These devices are available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt ceramic DIP, and TO-8 packages.

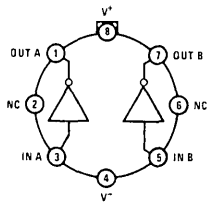
Features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

9

Connection Diagrams (Top Views)

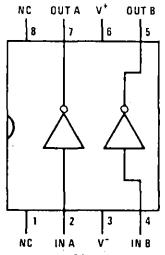
TO-5 Package



Note: Pin 4 connected to case.

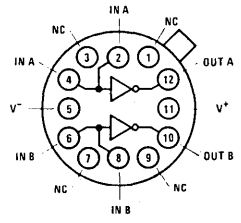
Order Number DS0026H or DS0026CH
See NS Package H08C

Dual-In-Line Package



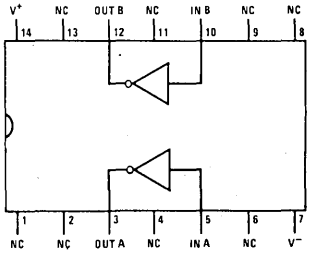
Order Number DS0026CJ-8, DS0026CN-8 or DS0026J-8
See NS Package J08A or N08A

TO-8 Package



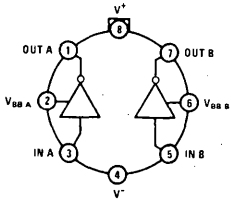
Order Number DS0026H or DS0026CH
See NS Package H12B

Flat Package



Order Number DS0026W
See NS Package W14A

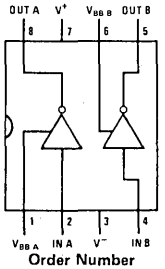
TO-5 Package



Note: Pin 4 connected to case.

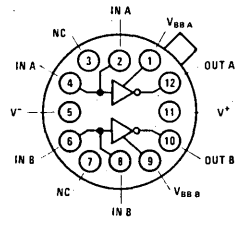
Order Number DS0056H or DS0056CH
See NS Package H08C

Dual-In-Line Package



Order Number DS0056J-8, DS0056CJ-8 or DS0056CN-8
See NS Package J08A or N08A

TO-8 Package



Order Number DS0056H or DS0056CH
See NS Package H12B

Absolute Maximum Ratings (Note 1)

$V^+ - V^-$ Differential Voltage	22V	Operating Temperature Range	
Input Current	100 mA	DS0026, DS0056	−55°C to +125°C
Input Voltage ($V_{IN} - V^-$)	5.5V	DS0026C, DS0056C	0°C to +70°C
Peak Output Current	1.5A	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logic "1" Input Voltage	$V^- = 0V$		2	1.5		V
I_{IH}	Logic "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logic "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logic "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OL}	Logic "1" Output Voltage	$V_{IN} - V^- = 2.4V$			V^-+0.7	V^-+1.0	V
V_{OH}	Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$, $V_{BB} \geq V^+ + 1.0V$	DS0026	V^+−1.0	V^+−0.7		V
			DS0056	V^+−0.3	V^+−0.1		V
$I_{CC(ON)}$	"ON" Supply Current	$V^+ - V^- = 20V$ $V_{IN} - V^- = 2.4V$ (Note 6) (one side on)	DS0026		30	40	mA
			DS0056		12	30	mA
$I_{CC(OFF)}$	"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0V$	70°C		10	100	μA
			125°C		10	500	μA

Switching Characteristics ($T_A = 25°C$) (Notes 5 and 7)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ON}	Turn-on Delay	*(Figure 1)*		5	7.5	12	ns
		(Figure 2)			11		ns
t_{OFF}	Turn-off Delay	*(Figure 1)*			12	15	ns
		(Figure 2)			13		ns
t_r	Rise Time	*(Figure 1)*, (Note 5)	C_L = 500 pF		15	18	ns
			C_L = 1000 pF		20	35	ns
		(Figure 2), (Note 5)	C_L = 500 pF		30	40	ns
			C_L = 1000 pF		36	50	ns
t_f	Fall Time	*(Figure 1)*, (Note 5)	C_L = 500 pF		12	16	ns
			C_L = 1000 pF		17	25	ns
		(Figure 2), (Note 5)	C_L = 500 pF		28	35	ns
			C_L = 1000 pF		31	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000$ pF, over the temperature range of −55°C to +125°C for the DS0026, DS0056 and 0°C to +70°C for the DS0026C, DS0056C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

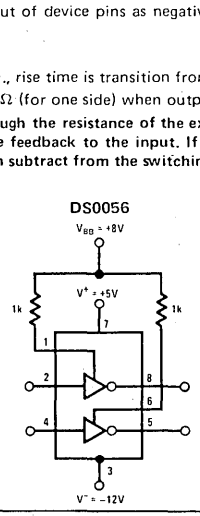
Note 4: All typical values for the $T_A = 25°C$.

Note 5: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

Note 6: I_{BB} for DS0056 is approximately $(V_{BB} - V^-)/1\ k\Omega$ (for one side) when output is low.

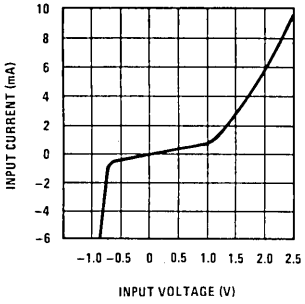
Note 7: The high current transient (as high as 1.5A) through the resistance of the external interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

Typical V_{BB} Connection

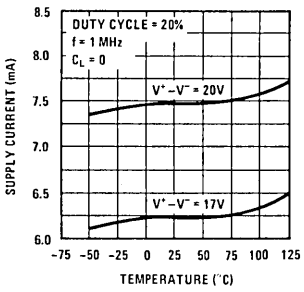


Typical Performance Characteristics

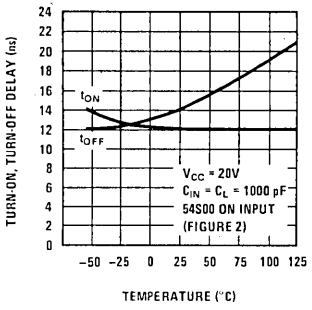
Input Current vs Input Voltage



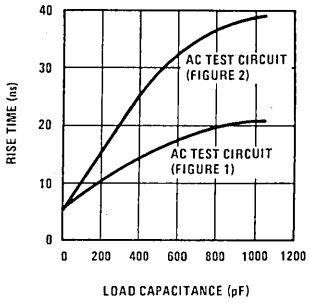
Supply Current vs Temperature



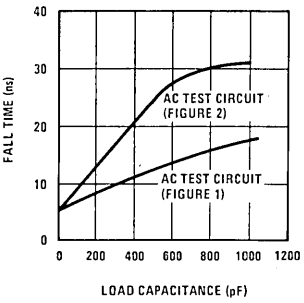
Turn-On and Turn-Off Delay vs Temperature



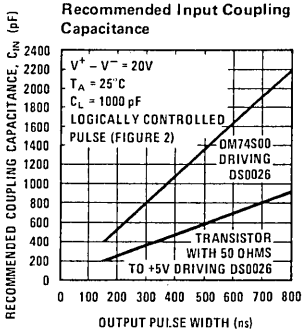
Rise Time vs Load Capacitance



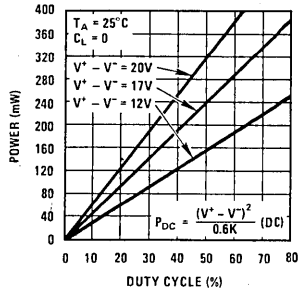
Fall Time vs Load Capacitance



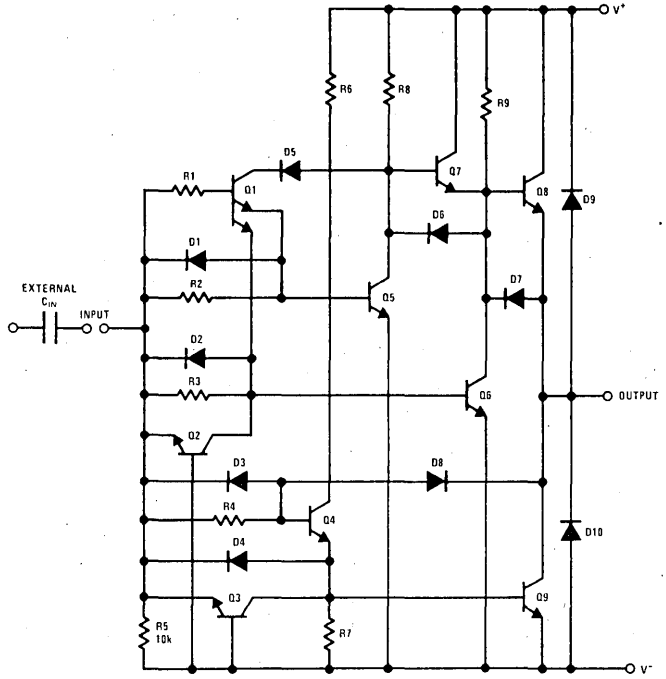
Recommended Input Coupling Capacitance



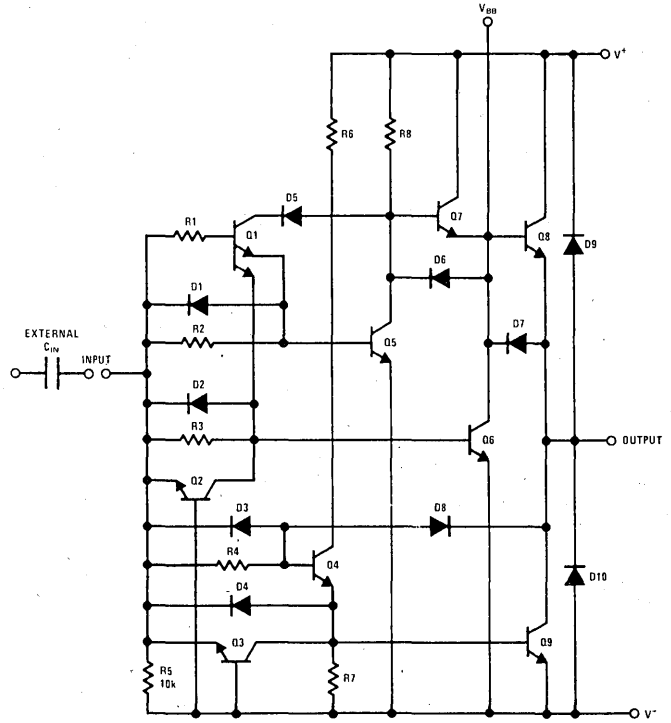
DC Power (P_{DC}) vs Duty Cycle



Schematic Diagrams

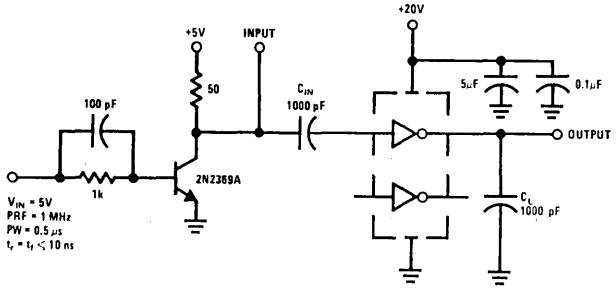


1/2 DS0026



1/2 DS0056

AC Test Circuits and Switching Time Waveforms



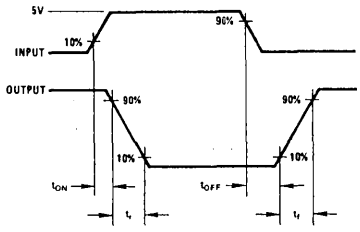
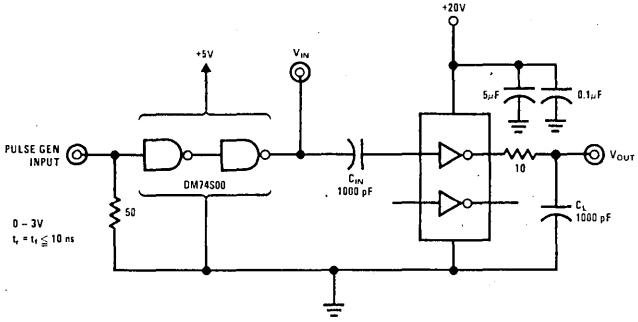


FIGURE 1.



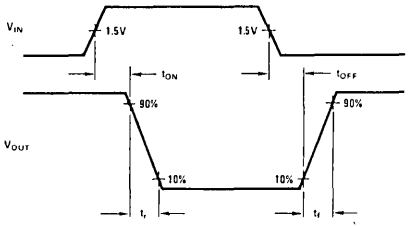
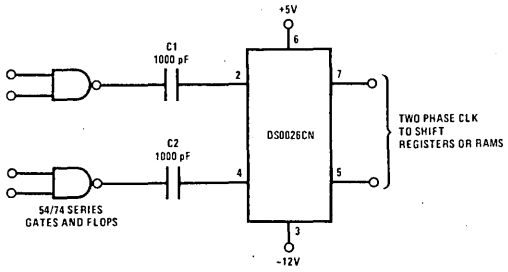


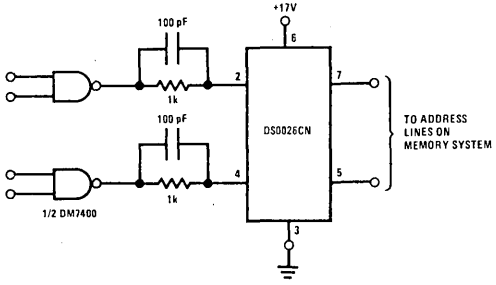
FIGURE 2.

Typical Applications

AC Coupled MOS Clock Driver



DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



Application Hints

DRIVING THE MM5262 WITH THE DS0056 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 6* shows the clock

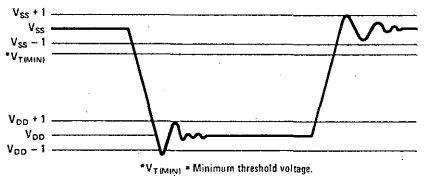


FIGURE 6. Clock Waveform

specification, in diagram form, with idealized ringing sketched in. The ringing of the clock about the V_{SS} level is particularly critical. If the $V_{SS} - 1$ V_{OH} is not maintained, at *all* times, the information stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were −1.3V, the clock going to $V_{SS} - 1$ would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.

Controlling the clock ringing is particulary difficult because of the relative magnitude of the allowable ringing, compared to the magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damping resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10 ohms to 20 ohms is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

The recommended clock driver for use with the MM4262/MM5262 is the DS0056/DS0056C dual clock driver. This device is designed specifically for use with dynamic circuits using a substrate, V_{BB}, supply. Typically it will drive a 1000 pF load with 20 ns rise and fall times. *Figure 7* shows a schematic of a single driver.

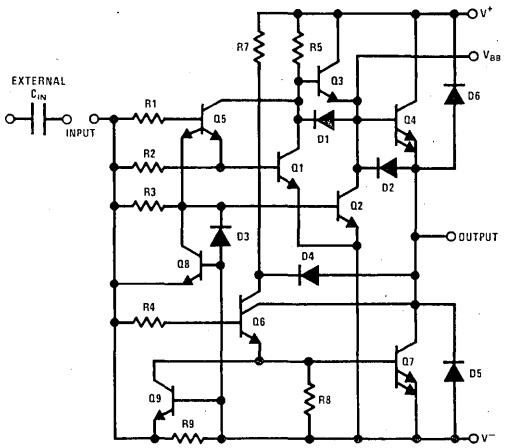


FIGURE 7. Schematic of 1/2 DS0056

In the case of the MM5262, V^+ is a +5V and V_{BB} is +8.5V. V_{BB} should be connected to the V_{BB} pin shown in *Figure 7* through a 1 kΩ resistor. This allows transistor Q4 to saturate, pulling the output to within a $V_{CE(SAT)}$ of the V^+ supply. This is critical because as was shown before, the $V_{SS} - 1.0$V clock level must not be exceeded at any time. Without the V_{BB} pull up on the base of Q4 the output at best will be 0.6V below the V^+ supply and can be 1V below the V^+ supply reducing the noise margin or this line to zero.

Application Hints (Cont'd)

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 8* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

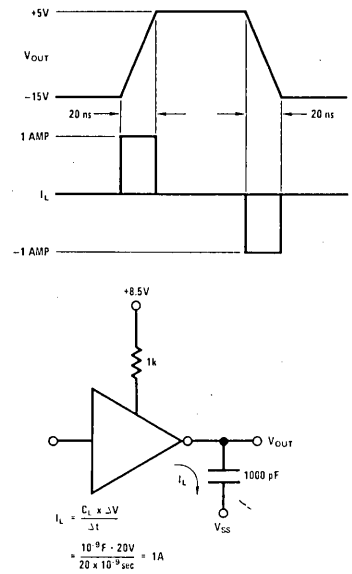


FIGURE 8. Clock Waveforms (Voltage and Current)

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies, A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. A bypass capacitor for each DS0056 is recommended. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0056 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since this noise is difficult to detect with an oscilloscope it is often overlooked.

Lastly, the clock lines must be considered as noise generators. *Figure 9* shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock tranisent from the 7404 because of the inductance, L.

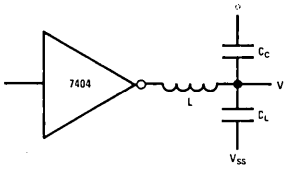


FIGURE 9. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \left(\frac{1}{56+1}\right) = 0.35V$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.3V of noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1\ mA$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262, coupling noise from the $\phi 2$ clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from $\phi 1$ clock.

Section 10

Digital Drivers

10

Section 10. Digital Drivers

These devices accept TTL or DTL input and provide extended output capability for actuators and displays

Typical Application Function	I_{OUT}	V_{SAT}	LV_{CEO}	t_{ON}	t_{OFF}	Part Number		Page Number
						−55°C to 125°C	−25°C to 85°C	
Motor, Relay, Current Sourcing	1.6A	1.5V	45V	0.40μs	7.0μs	DH0006H	DH0006CH DH0006CN	10-4
Lamps, Relay, Current Sourcing	0.25A	0.4V	40V	0.16μs	0.22μs	DH0008H	DH0008CH DH0008CN	10-7
Lamp Driver, Current Sinking	0.4A	1.0V	40V	0.26μs	2.2μs	DH0011H	DH0011CH DH0011CN	10-10
Lamp Driver, Current Sinking	0.5A	0.6V	50V	0.16μs	0.22μs	DH0011AH		10-13
Relay, Display, Current Sinking	0.25A	0.6V	70V	50ns	500ns		DH0016CN	10-16
Display, Current Sinking	0.50A	0.6V	50V	50ns	1.5μs		DH0017CN	10-16
Display, Current Sinking	0.05A	0.6V	100V	50ns	1.5μs		DH0018CN	10-16
Hammer Driver	5.0A	2.0V	45V	0.4μs	7.0μs	DH0028H	DH0028CH DH0028CN	10-19
Level Translator	100mA	0.5V	−25V	25ns	75ns	DH0034D DH0034H	DH0034CD DH0034CH	10-21
Pin Diode	±0.5A	1.0V	30V	10ns	30ns	DH0035G	DH0035CG	10-24
Electrostatic Print-head Driver,	20mA		425	12μs	1.8μs		DH0069CJ	10-26

Note: Also see the Interface Databook for other driver products.

National Semiconductor

DH0006/DH0006C Current Driver

General Description

The DH0006/DH0006C is an integrated high voltage, high current driver designed to accept standard DTL or TTL logic levels and drive a load of up to 400 mA at 28 volts. AND inputs are provided along with an Expander connection, should additional gating be required. The addition of an external capacitor provides control of the rise and fall times of the output in order to decrease cold lamp surges or to minimize electromagnetic interference if long lines are driven.

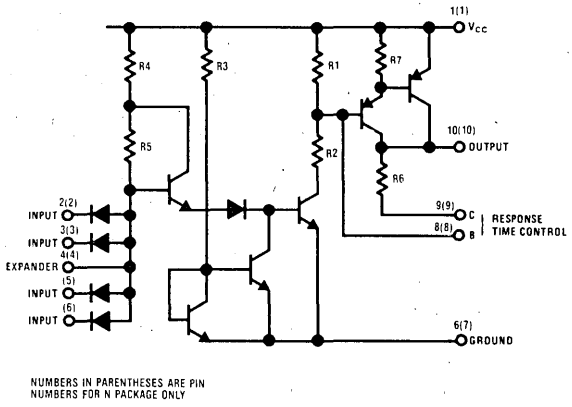
Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

*Previously called NH0006/NH0006C

Features

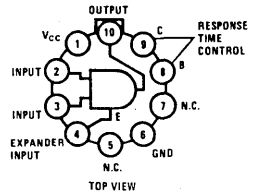
- Operation from a Single +10V to +45V Power Supply.
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply.
- 1.5A, 50 ms, Pulse Current Capability.

Schematic and Connection Diagrams



NUMBERS IN PARENTHESES ARE PIN NUMBERS FOR N PACKAGE ONLY

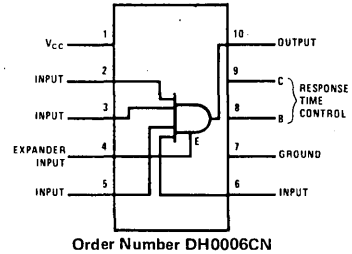
Metal Can Package



TOP VIEW

Order Number DH0006H or DH0006CH
See Package H10F

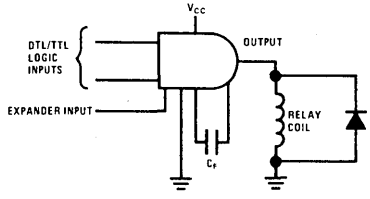
Dual-In-Line Package



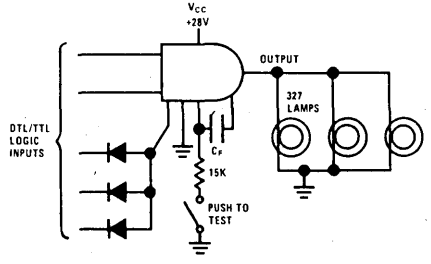
Order Number DH0006CN
See Package N10B

Typical Applications

Relay Driver



Lamp Driver with Expanded Inputs



Absolute Maximum Ratings

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0 mA
Peak Output Current (50 ms On/1 sec Off)	1.5A
Operating Temperature	
DH0006	−55°C to +125°C
DH0006C, DH0006CN	0°C to +70°C
Storage Temperature	−65°C to +150°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	V
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 400 mA	26.5	27.0		V
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1K		.001	.01	V
Logical "1" Output Voltage	V_{CC} = 10V, V_{IN} = 2.0V, I_{OUT} = 150 mA	8.8	9.2		V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = .4V		−0.8	−1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V		0.5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0.8V		1.6	2.0	mA
"On" Power Supply Current	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 0 mA			8	mA
Rise Time	V_{CC} = 28V, R_L = 82Ω		0.10		μs
Fall Time	V_{CC} = 28V, R_L = 82Ω		0.8		μs
T_{on}	V_{CC} = 28V, R_L = 82Ω		0.26		μs
T_{off}	V_{CC} = 28V, R_L = 82Ω		2.2		μs

Note 1: Unless otherwise specified, limits shown apply from −55°C to 125°C for DH0006 and 0°C to 70°C for DH0006C.

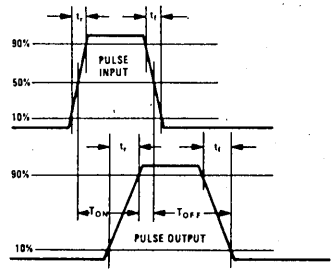
Note 2: Typical values are for 25°C ambient.

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and a ϕ_{JA} of 210°C/W.

Note 4: Power rating for the DH0006CN Molded DIP based on a maximum junction temperature of +150°C and a thermal resistance of 175°C/W when mounted in a standard DIP socket.

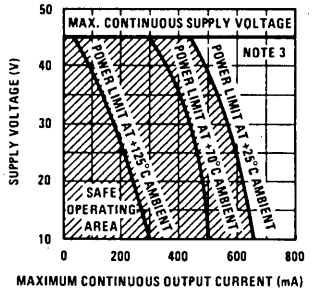
Note 5: Power rating for the DH0006CN Molded DIP based on a maximum junction temperature of +150°C and a thermal resistance of 150°C/W when mounted on a 1/16 inch thick, epoxy-glass board with ten 0.03 inch wide 2 ounce copper conductors.

Switching Time Waveforms

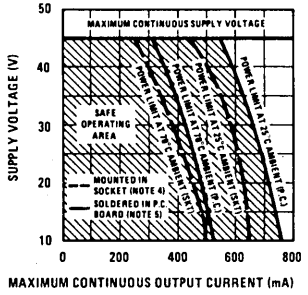


Typical Performance Characteristics

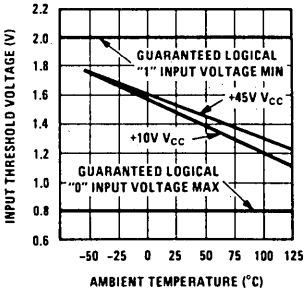
Maximum Continuous Output Current For TO-5



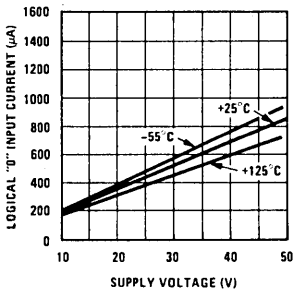
Maximum Continuous Output Current For Molded DIP



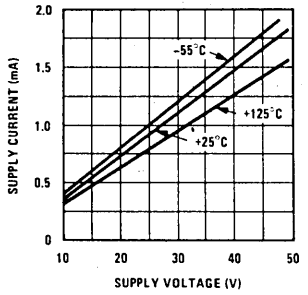
Input Threshold Voltage vs Temperature



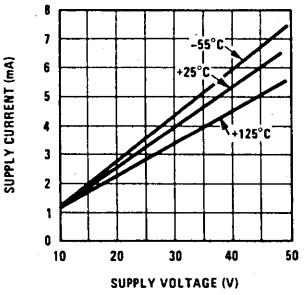
Logical "0" Input Current



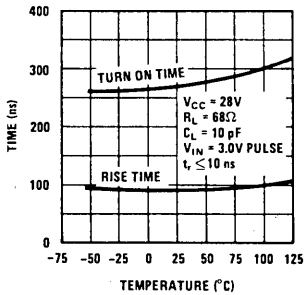
"OFF" Supply Current Drain



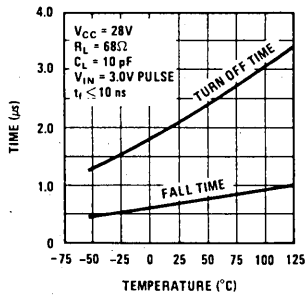
"ON" Supply Current Drain



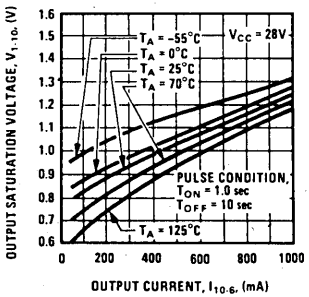
Turn On And Rise Time



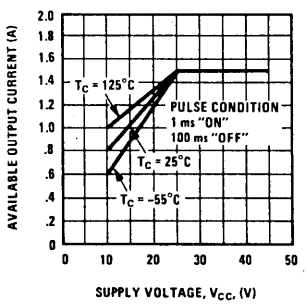
Turn Off and Fall Time



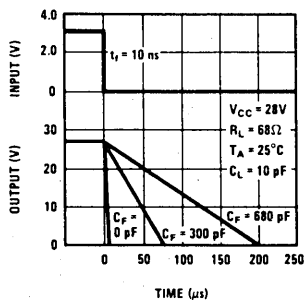
Output Saturation Voltage



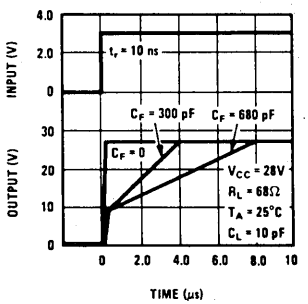
Available Output Current



Turn Off Control



Turn On Control



National Semiconductor

DH0008/DH0008C High Voltage, High Current Driver

General Description

The DH0008/DH0008C is an integrated high voltage, high current driver, designed to accept standard DTL or TTL input levels and provide a pulsed load of up to 3A from a continuous supply voltage up to 45V. AND inputs are provided with an EXPANDER connection, should additional gating be required.

Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

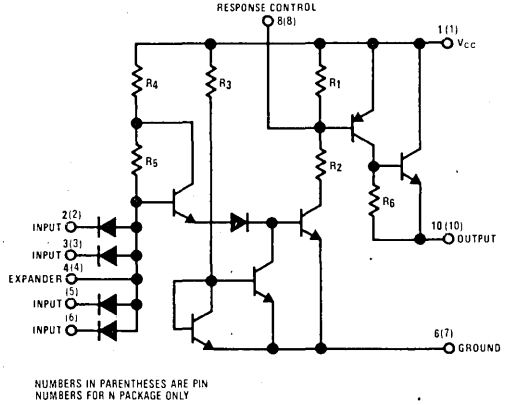
The high pulse current capability makes the DH0008/DH0008C ideal for driving nonlinear resistive loads such as incandescent lamps. The *Previously called NH0008/NH0008C circuit also requires only one power supply for circuit functional operation.

The DH0008 is available in a 10-pin TO-5 package; the DH0008C is also available in a 10-pin TO-5, in addition to a 10-lead molded dual-in-line package.

Features

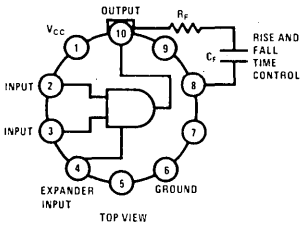
- Operation from a Single +10V to +45V Power Supply.
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply.
- 3.0A, 50 ms, Pulse Current Capability.

Schematic and Connection Diagrams



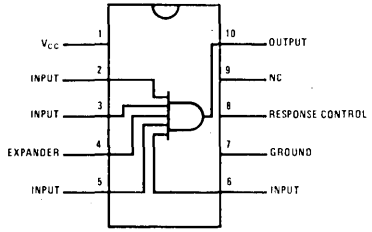
NUMBERS IN PARENTHESES ARE PIN NUMBERS FOR N PACKAGE ONLY

Metal Can Package



Order Number DH0008H or DH0008CH
See Package H10F

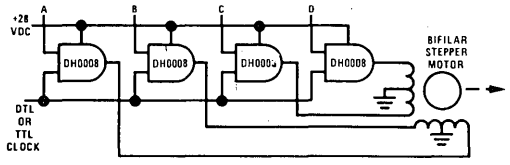
Dual-In-Line Package



Order Number DH0008CN
See Package N10B

Typical Applications

Controller for Closed Loop Stepper Motor



Switching Sequence

Step	A	B	C	D
1	1	0	1	0
2	1	0	0	1
3	0	1	0	1
4	0	1	1	0
1	1	0	1	0

To reverse the direction use a 4, 3, 2, 1 sequence

Absolute Maximum Ratings

Peak Power Supply Voltage (for 0.1s)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0mA
Peak Output Current (50ms On/1s Off)	3.0A
Operating Temperature	
DH0008	−55°C to +125°C
DH0008C	0°C to +70°C
Storage Temperature	−65°C to +150°C

Electrical Characteristics (Note 1)

Parameter	Conditions	Min.	Typ. (Note 2)	Max.	Units
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	V
Logical "1" Output Voltage	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 1.6A 50ms On/1s Off	43	43.5		V
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1kΩ		0.02	0.1	V
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 0.8A 50ms On/1s Off	26.5	27.1		V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0.4V		−0.8	−1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V		0.5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0V		1.6	2.0	mA
"On" Power Supply Current	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 0mA			8.0	mA
Rise Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		0.2		μs
Fall Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		3.0		μs
T_{ON}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		0.4		μs
T_{OFF}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		7.0		μs

Note 1: Unless otherwise specified limits shown apply from −55°C to 125°C for DH0008 and 0°C to 70°C for DH0008C.

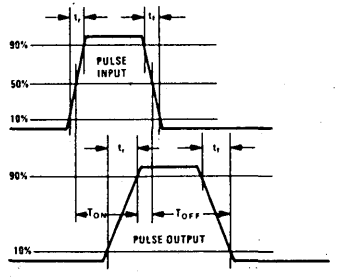
Note 2: Typical values are 25°C.

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and a θ_{JA} of 210°C/W.

Note 4: Power ratings for the DH0008CN Molded DIP based on a maximum junction temperature of 150°C and a thermal resistance of 150°C/W when mounted in a standard DIP socket.

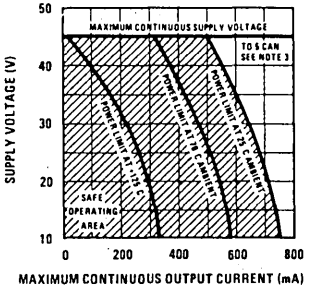
Note 5: Power ratings for the DH0008CN Molded DIP based on a maximum junction temperature of 150°C and a thermal resistance of 115°C/W when mounted on a 1/16 inch thick, epoxy glass board with ten 0.03 inch wide 2 ounce copper conductors.

Switching Time Waveforms

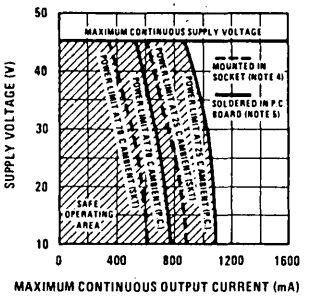


Typical Performance Characteristics

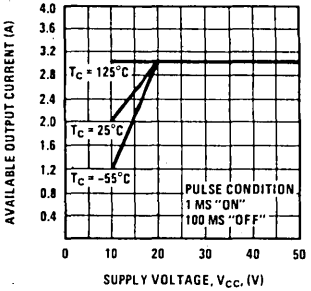
Maximum Continuous Output Current for TO-5 Package



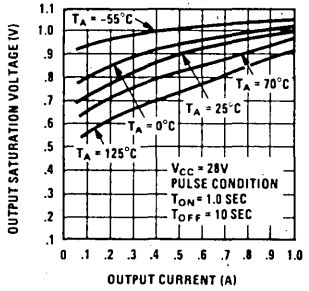
Maximum Continuous Output Current for Molded DIP



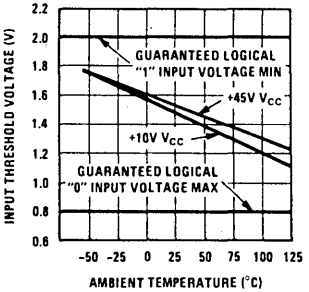
Available Output Current



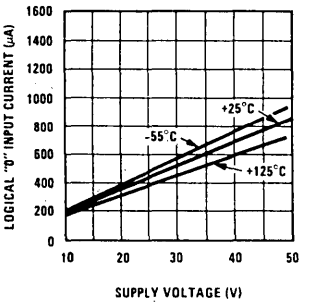
Output Saturation Voltage



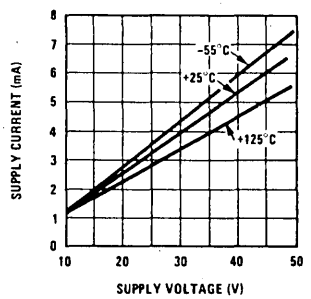
Input Threshold Voltage vs Temperature



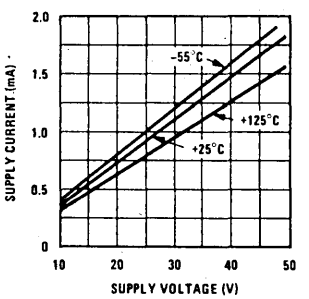
Logical "0" Input Current



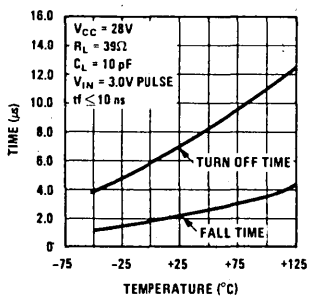
ON Supply Current Drain



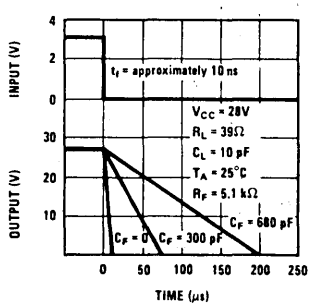
OFF Supply Current Drain



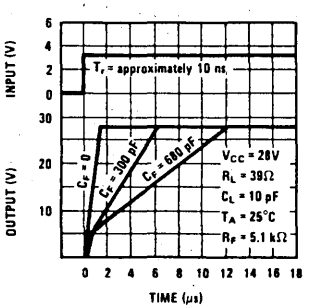
Turn OFF and Fall Times



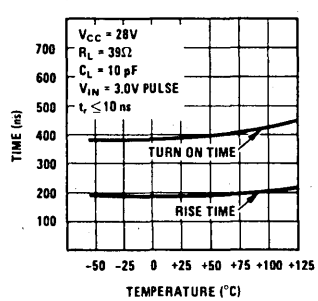
Turn ON Control



Turn OFF Control



Turn ON and Rise Time



National Semiconductor

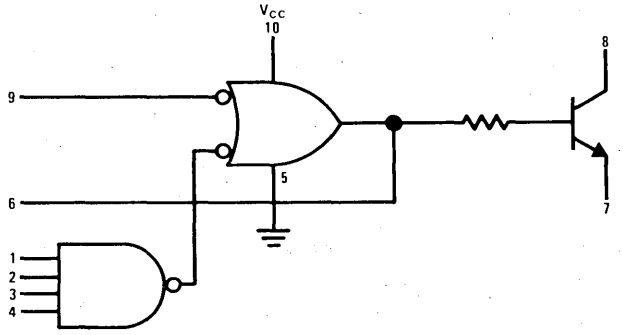
DH0011/DH0011C/DH0011CN High Voltage High Current Drivers

General Description

The DH0011 high voltage, high current driver family consists of hybrid integrated circuits which provide a wide range of variations in temperature range, package, and output current drive capability. A summary of the variations is listed below.

Applications include driving lamps, relays, cores, and other devices requiring several hundred milliamp currents at voltages up to 40V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects the base of the output transistor.

Logic Diagram



Ordering Information

NSC DESIGNATION	PACKAGE	TEMPERATURE RANGE	OUTPUT CURRENT CAPABILITY
DH0011H	H10C	-55°C to +125°C	250 mA
DH0011CH	H10C	0°C to +70°C	150 mA
DH0011CN	N10B	0°C to +70°C	150 mA

Absolute Maximum Ratings

V_{CC}		8V
Collector Voltage (Output)		40V
Input Reverse Current		1.0 mA
Power Dissipation		800 mW
Operating Temperature Range	DH0011	−55°C to +125°C
	DH0011C/DH0011CN	0°C to +70°C
Storage Temperature		−65°C to 150°C

Electrical Characteristics

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	MIN	MAX
1	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CCL}	V_8		V_{OL}
2	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CCL}	V_8		V_{OL}
3	V_{IL}				GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
4		V_{IL}			GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
5			V_{IL}		GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
6				V_{IL}	GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
7				GND	GND	I_{OL2}			V_{IH}	V_{CCL}	V_6		V_{OL2}
8	V_R	GND	GND	GND	GND					V_{CCH}	I_1		I_R
9	GND	V_R	GND	GND	GND					V_{CCH}	I_2		I_R
10	GND	GND	V_R	GND	GND					V_{CCH}	I_3		I_R
11	GND	GND	GND	V_R	GND					V_{CCH}	I_4		I_R
12					GND				V_R	V_{CCH}	I_9		I_R
13	V_F	V_R	V_R	V_R	GND					V_{CCH}	I_1		$-I_F$
14	V_R	V_F	V_R	V_R	GND					V_{CCH}	I_2		$-I_F$
15	V_R	V_R	V_F	V_R	GND					V_{CCH}	I_3		$-I_F$
16	V_R	V_R	V_R	V_F	GND					V_{CCH}	I_4		$-I_F$
17				GND	GND				V_F	V_{CCH}	I_9		$-I_F$
18					GND		GND			V_{CCL}	V_6	V_{OH}	
19	GND				GND		GND	V_{OX}		V_{CCL}	I_8		I_{OX}
20					GND		GND			V_{PD}	I_{10}		I_{PDH}
21	GND				GND					V_{MAX}	I_{10}		I_{MAX}
22*					GND					V_{PD}			t_{ON}
23*					GND					V_{PD}			t_{OFF}

*See Test Circuits and Waveforms on Page 4.

Forcing Functions (Note 1) DH0011

PARAMETER	−55°C	+25°C	+125°C	UNITS
V_{CCL}	4.5	4.5	4.5	V
V_{CCH}	5.5	5.5	5.5	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	1.4	1.1	0.8	V
V_{IH}	2.1	1.9	1.7	V
V_R	4.0	4.0	4.0	V
V_F	0.0	0.0	0.0	V
I_{OL1}	250	250	250	mA
I_{OL2}	8.0	8.0	7.5	mA
V_{OX}	40.0	40.0	40.0	V

Note 1: Temperature Range −55°C to +125°C

Forcing Functions (Note 2) DH0011C, DH0011CN

PARAMETER	0°C	+25°C	+70°C	UNITS
V_{CCL}	5.00	5.0	5.0	V
V_{CCH}	5.00	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	1.20	1.1	.95	V
V_{IH}	2.00	1.9	1.8	V
V_R	4.00	4.0	4.0	V
V_F	0.45	0.45	0.5	V
I_{OL1}	150	150	150	mA
I_{OL2}	8.0	8.0	7.5	mA
V_{OX}	40.00	40.0	40.0	V

Test Limits (Note 1) DH0011

PARAMETER	-55°C		+25°C		+125°C		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL1}		0.45		0.4		0.45	V
V_{OL2}		0.45		0.4		0.45	V
V_{OH}	2.20		2.00		1.80		V
I_R				2.0		5.0	μA
$-I_F$		1.60		1.6		1.5	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				29.6			mA
t_{ON}				160			ns
t_{OFF}				220			ns

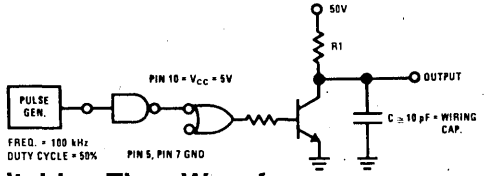
Test Limits (Note 2) DH0011C, DH0011CH

PARAMETER	0°C		+25°C		+70°C		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL1}		0.45		0.45		0.5	V
V_{OL2}		0.45		0.45		0.5	V
V_{OH}	2.05		1.95		1.85		V
I_R				5.0		10.0	μA
$-I_F$		1.40		1.4		1.35	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				34.0			mA

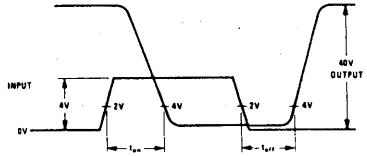
Note 1: Temperature Range -55°C to +125°C

Note 2: Temperature Range 0°C to +70°C

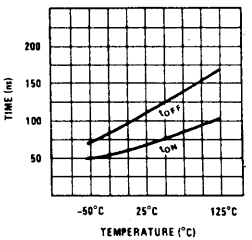
Switching Time Test Circuit



Switching Time Waveforms



Typical Switching Times



National Semiconductor

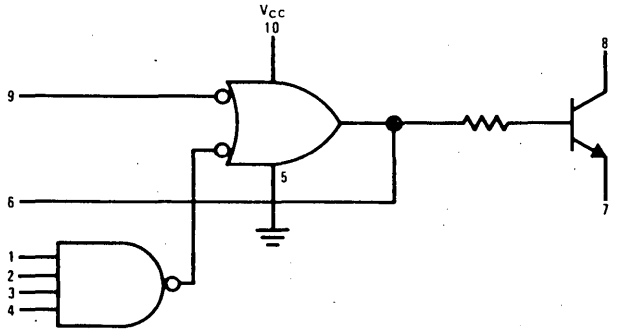
DH0011A High Voltage High Current Driver

General Description

The DH0011A High Voltage, High Current Driver family consists of hybrid integrated circuits which provide a wide range of variations in temperature range, package, and output current drive capability.

Applications include driving lamps, relays, cores, and other devices requiring several hundred milliamp currents at voltages up to 50V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects to the base of the output transistor.

Logic Diagram



Ordering Information

NSC Designation	Package	Temperature Range	Output Capability
DH0011AH	H10C	−55°C to +125°C	500mA

Absolute Maximum Ratings

V_{CC}	8V
Collector Voltage (Output)	50V
Input Reverse Current	1.0 mA
Power Dissipation	800 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C

Electrical Characteristics

Test No.	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Sense	Min.	Max.
1	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CC}	V_8		V_{OL1}
2	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
3	V_{IL}				GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
4		V_{IL}			GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
5			V_{IL}		GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
6				V_{IL}	GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
7				GND	GND	I_{OL2}			V_{IH}	V_{CC}	V_6		V_{OL2}
8	V_R	GND	GND	GND	GND					V_{CC}	I_1		I_R
9	GND	V_R	GND	GND	GND					V_{CC}	I_2		I_R
10	GND	GND	V_R	GND	GND					V_{CC}	I_3		I_R
11	GND	GND	GND	V_R	GND					V_{CC}	I_4		I_R
12					GND				V_R	V_{CC}	I_9		I_R
13	V_F	V_R	V_R	V_R	GND					V_{CC}	I_1		$-I_F$
14	V_R	V_F	V_R	V_R	GND					V_{CC}	I_2		$-I_F$
15	V_R	V_R	V_F	V_R	GND					V_{CC}	I_3		$-I_F$
16	V_R	V_R	V_R	V_F	GND					V_{CC}	I_4		$-I_F$
17				GND	GND				V_F	V_{CC}	I_9		$-I_F$
18					GND		GND			V_{CC}	V_6	V_{OH}	
19	GND				GND		GND	V_{OX}		V_{CC}	I_8		I_{OX}
20					GND					V_{PD}	I_{10}		I_{PD}
21	GND				GND					V_{MAX}	I_{10}		I_{MAX}
22*					GND					V_{PD}			t_{ON}
23*					GND					V_{PD}			t_{OFF}

*See Test Circuits and Waveforms on Page 3.

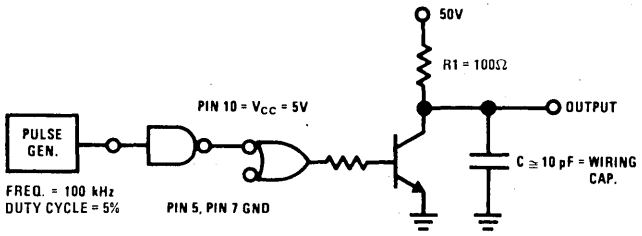
Forcing Functions DH0011A

Parameter	−55°C	+25°C	+125°C	Units
				V
V_{CC}	5.0	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	0.85	0.85	0.85	V
V_{IH}	1.9	1.8	1.6	V
V_R	4.5	4.5	4.5	V
V_F	0.45	0.45	0.45	V
I_{OL1}	500	500	500	mA
I_{OL2}	16	16	16	mA
V_{OX}	50.0	50.0	50.0	V

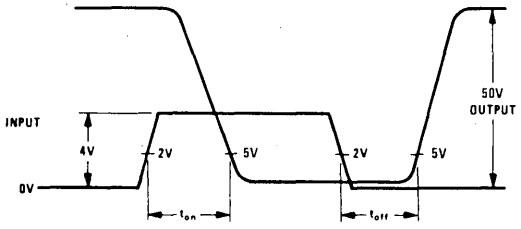
Limits DH0011A

Parameter	−55°C		+25°C		+125°C		Units
	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OL1}		0.6		0.6		0.6	V
V_{OL2}		0.45		0.45		0.45	V
V_{OH}	1.95		1.85		1.65		V
I_R				60		60	μA
$-I_F$		1.6		1.6		1.6	mA
I_{OX}				5.0		200	μA
I_{PD}				12.2			mA
I_{MAX}				10			mA
t_{ON}				160			ns
t_{OFF}				220			ns

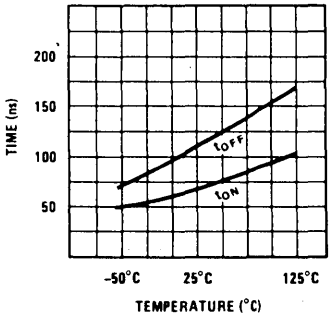
Switching Time Test Circuit



Switching Time Waveforms



Typical Switching Times



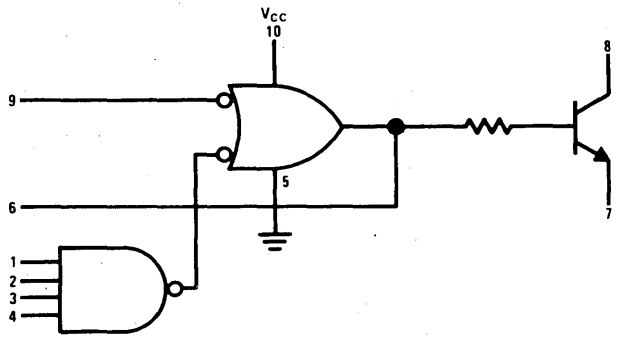
National Semiconductor

DH0016CN, DH0017CN, DH0018CN High Voltage High Current Drivers

General Description

This high-voltage, high-current driver family consists of hybrid integrated circuits which provide a wide range of output currents and output voltages. Applications include driving lamps, relays, cores, and other devices requiring up to 500 mA and withstanding voltages up to 100V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects to the base of the output transistor.

Logic Diagram



Ordering Information

NSC DESIGNATION	PACKAGE	OUTPUT CHARACTERISTICS	
		Maximum Standoff Voltage	Current
DH0016CN	N10B	70V	250 mA
DH0017CN	N10B	50V	500 mA
DH0018CN	N10B	100V	500 mA

Absolute Maximum Ratings

V_{CC}		8V
Input Voltage		8V
Collector Voltage	DH0016CN	70V
	DH0017CN	50V
	DH0018CN	100V
Output Surge Current	DH0016CN	1.0A
	DH0017CN & DH0018CN	2.0A
Power Dissipation		455mW
Operating Temperature Range		0°C to +70°C
Storage Temperature		−65°C to +150°C

Electrical Characteristics

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMITS MIN	LIMITS MAX
2	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CC}	V_8		V_{OL1}
3	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
4		V_{IL}			GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
5			V_{IL}		GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
6				V_{IL}	GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
7	V_{IL}				GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
8		V_{IL}			GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
9			V_{IL}		GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
10				V_{IL}	GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
11				GND	GND	I_{OL2}			V_{IH}	V_{CC}	V_6		V_{OL2}
12	V_R	GND	GND	GND	GND					V_{CC}	I_1		I_R
13	GND	V_R	GND	GND	GND					V_{CC}	I_2		I_R
14	GND	GND	V_R	GND	GND					V_{CC}	I_3		I_R
15	GND	GND	GND	V_R	GND					V_{CC}	I_4		I_R
16					GND				V_R	V_{CC}	I_9		I_R
17	V_F	V_R	V_R	V_R	GND					V_{CC}	I_1		$-I_F$
18	V_R	V_F	V_R	V_R	GND					V_{CC}	I_2		$-I_F$
19	V_R	V_R	V_F	V_R	GND					V_{CC}	I_3		$-I_F$
20	V_R	V_R	V_R	V_F	GND					V_{CC}	I_4		$-I_F$
21				GND	GND				V_F	V_{CC}	I_9		$-I_F$
22					GND		GND			V_{CC}	V_6	V_{OH1}	
23	GND				GND	I_{OL3}	GND	V_{OX}		V_{CC}	I_8		I_{OX}
24					GND					V_{PD}	I_{10}		I_{PD}
25	GND				GND				GND	V_{MAX}	I_{10}		I_{MAX}

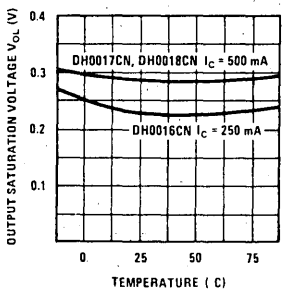
Forcing Functions

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{CC}	5.0	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	0.85	0.85	0.85	V
V_{IH}	1.9	1.8	1.6	V
V_R	4.5	4.5	4.5	V
V_F	0.45	0.45	0.45	V
V_{OX} (DH0016CN)		70	70	V
V_{OX} (DH0017CN)		50	50	V
V_{OX} (DH0018CN)		100	100	V
I_{OL1} (DH0017CN, DH0018CN)	500	500	500	mA
I_{OL1} (DH0016CN)	250	250	250	mA
I_{OL2}	16	16	16	mA
I_{OL3}		8.0		mA

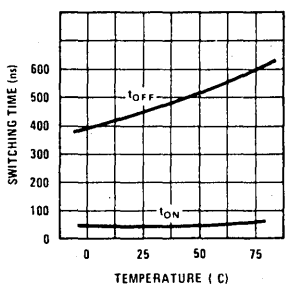
Test Limits

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{OL1}	0.6	0.6	0.6	V
V_{OL2}	0.45	0.45	0.45	V
V_{OH1}	1.95	1.85	1.65	V
I_R		60	60	μA
$-I_F$	1.6	1.6	1.6	mA
I_{OX}		5.0	200	μA
I_{PD}		12.2		mA
I_{MAX}		10		mA

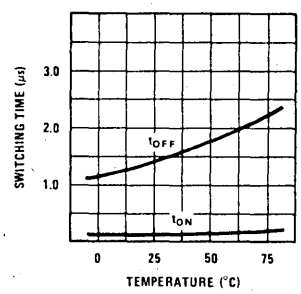
Typical Output Voltages vs Temperature



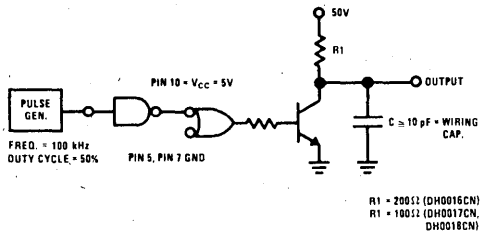
Typical Switching Times I_C = 250 mA
DH0016CN



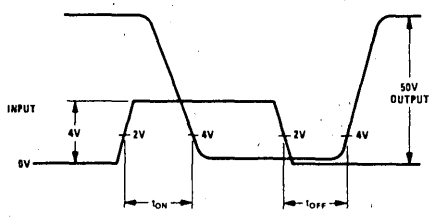
Typical Switching Times I_C = 500 mA
DH0017CN, DH0018CN



Switching Time Test Circuit



Switching Time Waveform



National Semiconductor

DH0028C/DH0028CN Hammer Driver

General Description

The DH0028C/DH0028CN is a high current hammer driver designed for utilization in a wide variety of printer applications. The device is capable of driving 6 amp pulsed loads at duty cycles up to 10% (1 ms ON/10 ms OFF). The input is DTL/TTL compatible and requires only a single voltage supply in the range of 10V to 45V.

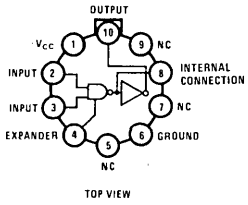
Features

- Low standby power: 45 mW at V_{CC} = 36V, 35 mW at V_{CC} = 28V.
- AND input with expander affords logic flexibility.
- Fast turn-on, typically 200 ns.

*Previously called NH0028C/NH0028CN

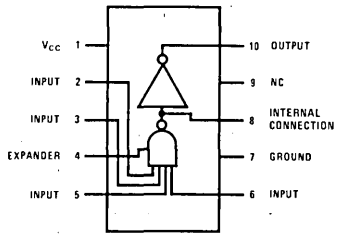
Connection Diagrams

Metal Can Package



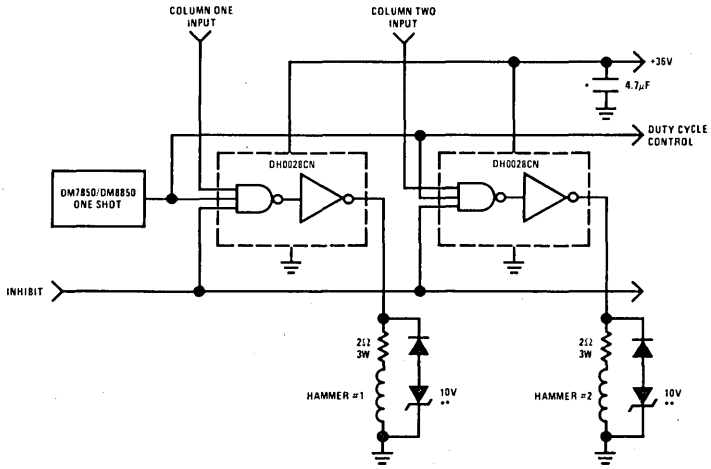
Order Number DH0028CH
See Package H10F

Molded Dual-In-Line Package



Order Number DH0028CN
See Package N10B

Typical Applications



*Use one decoupling capacitor per six hammer drivers for improved AC noise immunity.
**Zener is used to control the dynamics of the hammer.

Absolute Maximum Ratings

Continuous Supply Voltage	45V
Instantaneous Peak Supply Voltage (Pin 1 to Ground for 0.1 sec)	60V
Input Voltage	5.5V
Expander Input Current	5.0 mA
Peak Output Current (1 ms ON/10 ms OFF)	6.5A
Continuous Output Current DH0028C at 25°C	750 mA
DH0028CN at 25°C	1000 mA
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +175°C
Lead Soldering Temperature (10 sec)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 10V to 45V	2.0			V
Logical "0" Input Voltage	V_{CC} = 10V to 45V			0.8	V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0.4V		0.8	1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V		0.5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100.0	μA
Logical "1" Output Voltage	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 1.6A	43.0	43.5		V
	V_{CC} = 36V, V_{IN} = 2.0V, I_{OUT} = 5A (Note 2)	33.5	34.0		V
Logical "0" Output Voltage	V_{CC} = 45V, R_L = 1k, V_{IN} = 0.8V		.020	100	V
OFF Power Supply Current	V_{CC} = 45V, V_{IN} = 0.0V		1.6	2.0	mA
Rise Time (10% to 90%)	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		0.2		μs
Fall Time (90% to 10%)	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		3.0		μs
T_{ON}	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		0.4		μs
T_{OFF}	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5.0V peak, PRF = 1 kHz		7.0		μs

Note 1: These specifications apply for ambient temperatures from 0°C to 70°C unless otherwise specified. All typical values are for 25°C ambient.

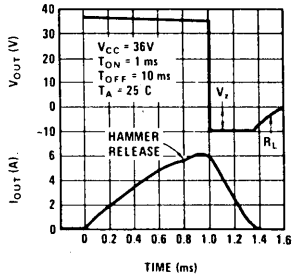
Note 2: Measurement made at 1 ms ON and 10 ms OFF.

Note 3: Power ratings for the DH0028C are based on a maximum junction temperature of 175°C and a thermal resistance of 210°C/W.

Note 4: Power ratings for the DH0028CN are based on a maximum junction temperature of 175°C and a thermal resistance of 150°C/W.

Typical Performance Characteristics

Waveforms for Typical Drum Printer Hammer



National Semiconductor

DH0034/DH0034C High Speed Dual Level Translator

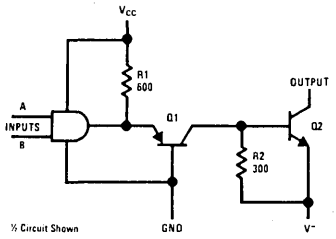
General Description

The DH0034/DH0034C is a high speed level translator suitable for interfacing to MOS or junction FET analog switches. It may also be used as a universal logic level shifter capable of accepting TTL/DTL input levels and shifting to CML, MOS, or SLT levels.

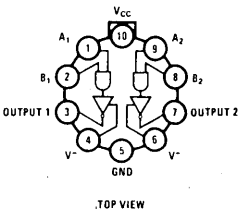
Features

- Fast switching, t_{pd0}: typically 15 ns; t_{pd1}: typically 35 ns
- Large output voltage range: 25V
- Input is TTL/DTL compatible
- Low output leakage: typically 0.1 μA

Schematic and Connection Diagrams

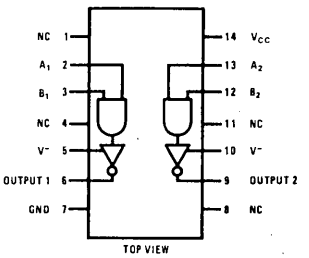


Metal Can Package



Order Number DH0034H
or DH0034CH
See Package H10F

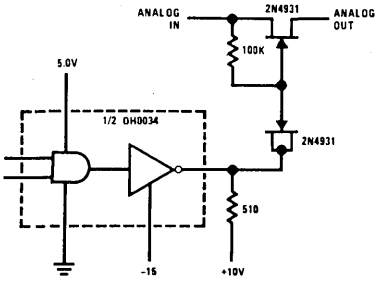
Dual-in-Line Package



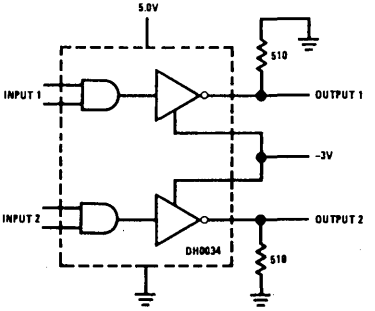
Order Number DH0034D
or DH0034CD
See Package D14D

Typical Applications

5 MHz Analog Switch



TTL to IBM (SLT) Logic Levels



10

Absolute Maximum Ratings

V_{CC} Supply Voltage	7.0V
Negative Supply Voltage	−30V
Positive Supply Voltage	+25V
Differential Supply Voltage	25V
Maximum Output Current	100mA
Input Voltage	+5.5V
Operating Temperature Range	
DH0034	−55°C to +125°C
DH0034C	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (See Notes 1 and 2)

Parameter	Conditions	DH0034			DH0034C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Logical "1" Input Voltage	$V_{CC}=4.5V$ $V_{CC}=4.75V$	2.0			2.0			V
Logical "0" Input Voltage	$V_{CC}=5.5V$ $V_{CC}=5.25V$			0.8			0.8	V
Logical "1" Input Current	$V_{CC}=5.5V$, $V_{IN}=2.4V$ $V_{CC}=5.25V$, $V_{IN}=2.4V$			40			40	μA
Logical "1" Input Current	$V_{CC}=5.5V$, $V_{IN}=5.5V$ $V_{CC}=5.25V$, $V_{IN}=5.5V$			1.0			1.0	mA
Logical "0" Input Current	$V_{CC}=5.5V$, $V_{IN}=0.4V$ $V_{CC}=5.25V$, $V_{IN}=0.4V$			−1.6			−1.6	mA
Power Supply Current Logic "0"	(Note 3) $V_{CC}=5.5V$, $V_{IN}=4.5V$ $V_{CC}=5.25V$, $V_{IN}=4.5V$		30	38		30	38	mA
Power Supply Current Logic "1"	(Note 3) $V_{CC}=5.5V$, $V_{IN}=0V$ $V_{CC}=5.25V$, $V_{IN}=0V$		37	48		37	48	mA
Logical "0" Output Voltage	$V_{CC}=4.5V$, $I_{OUT}=100mA$ $V_{CC}=4.5V$, $I_{OUT}=50mA$		$V^-+0.50$ $V^-+0.3$	 $V^-+0.50$		$V^-+0.50$ $V^-+0.3$	 $V^-+0.65$	V V
Output Leakage Current	$V_{CC}=5.5V$, $V_{IN}=0.8V$ $V^+-V^-=25V$		0.1	5.0		0.1	5.0	μA
Transition Time to Logical "0"	$V_{CC}=5.0V$, $V_3=0V$, $T_A=25°C$ $V^-=25V$, $R_L=510Ω$		15	25		15	35	ns
Transition Time to Logical "1"	$V_{CC}=5.0V$, $T_A=25°C$ $V^-=-25V$, $R_L=510Ω$		35	75		35	75	ns

Note 1: The specifications apply over the temperature range −55°C to +125°C for the DH0034 and 0°C to +85°C for the DH0034C with a 510Ω resistor connected between output and ground, and V^- connected to −25V, unless otherwise specified.

Note 2: All typical values are for $T_A=25°C$.

Note 3: Current measured is total drawn from V_{CC} supply.

Note 4: Power rating for the TO-5 metal can based on a maximum junction temperature of 175°C and $\theta_{JA}=210°C/W$.

Note 5: Power rating for the Cavity DIP based on a maximum junction temperature of 175°C and $\theta_{JA}=180°C/W$.

Theory of Operation

When both inputs of the DH0034 are raised to logic "1", the input AND gate is turned "on" allowing Q1's emitter to become forward biased. Q1 provides a level shift and constant output current. The collector current is essentially the same as the emitter which is given by $\frac{V_{CC} - V_{BE}}{R1}$. Approximately 7.0 mA flows out of Q1's collector.

About 2 mA of Q1's collector current is drawn off by pull down resistor, R2. The balance, 5 mA, is available as base drive to Q2 and to charge its associated Miller capacitance. The output is pulled to within a V_{SAT} of V^-. When either (or both) input to the DH0034 is lowered to logic "0," the AND gate output drops to 0.2V turning Q1 off. Deprived of base drive Q2 rapidly turns off causing the output to rise to the V_3 supply voltage. Since Q2's emitter operates between 0.6V and 0.2V, the speed of the DH0034 is greatly enhanced.

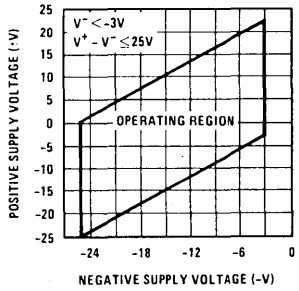
Applications Information

1. Paralleling the Outputs

The outputs of the DH0034 may be paralleled to increase output drive capability or to accomplish the "wire OR". In order to prevent current hogging by one output transistor or the other, resistors of 2 ohms/100 mA value should be inserted between the emitters of the output transistors and the minus supply.

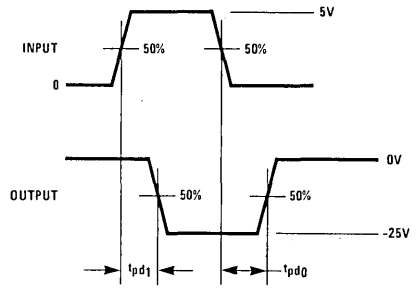
2. Recommended Output Voltage Swing

The graph shows boundary conditions which govern proper operation of the DH0034. **The range of operation for the negative supply is shown on the X axis and must be between −3V and −25V.** The allowable range for the positive supply is governed by the value chosen for V^-. V^+ may be selected by drawing a vertical line through the selected value for V^- and terminated by the boundaries of the operating region. For example, a value of V^- equal to −6V would dictate values of



V^+ between −5V and +19V. In general, it is desirable to maintain at least 5V difference between the supplies.

Switching Time Waveforms



National Semiconductor

DH0035/DH0035C PIN Diode Driver

General Description

The DH0035/DH0035C is a high speed digital driver designed to drive PIN diodes in RF modulators and switches. The device is used in conjunction with an input buffer such as the DM7830/DM8830 or DM5440/DM7440.

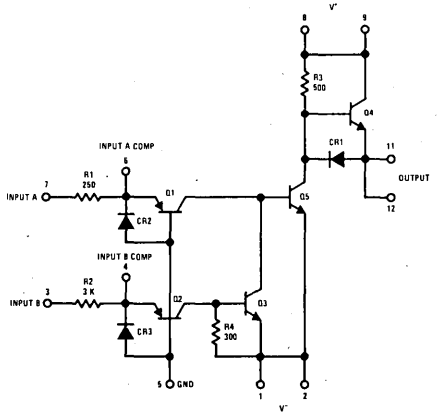
Features

- Large output voltage swing – 30V
- Peak output current in excess of 1 Amp
- Inputs TTL/DTL compatible
- Short propogation delay – 10 ns
- High repetition rate – 5 MHz

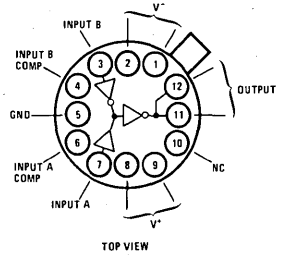
The DH0035/DH0035C is capable of driving a variety of PIN diode types including parallel, serial, anode grounded and cathode grounded. For additional information, see *AN-49 PIN Diode Drivers*.

The DH0035 is guaranteed over the temperature range −55°C to +125°C whereas the DH0035C is guaranteed from 0°C to 85°C.

Schematic and Connection Diagrams



Metal Can Package

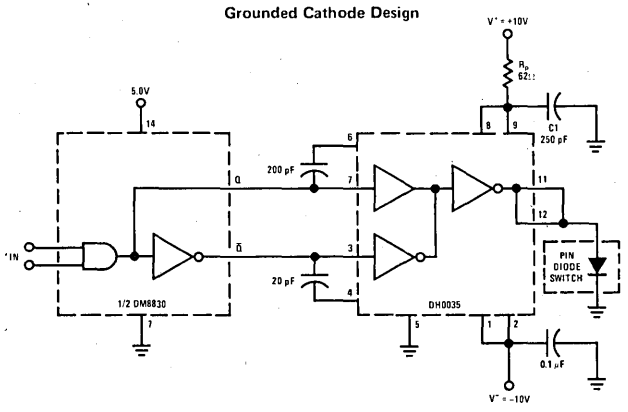


TOP VIEW

Order Number DH0035G or DH0035CG
See Package H12B

Typical Applications

Grounded Cathode Design



Note: Cathode grounded PIN diode: R_P = 62Ω limits diode forward current to 100 mA. Typical switching for HP3360-4A, RF turn-on 25 ns, turn-off 5 ns. C2 = 250 pF, R_P = 0Ω, C1 = 0.1F.

Absolute Maximum Ratings

V^- Supply Voltage Differential (Pin 5 to Pin 1 or 2)	40V
V^+ Supply Voltage Differential (Pin 1 or 2 to Pin 8 or 9)	30V
Input Current (Pin 3 or 7)	±75 mA
Peak Output Current	±1.0 Amps
Power Dissipation (Note 3)	1.5W

Storage Temperature Range	−65°C to +150°C
Operating Temperature Range DH0035	−55°C to +125°C
DH0035C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Logic "1" Threshold	V_{OUT} = −8V, R_L = 100Ω		1.0	2.0	V
Input Logic "0" Threshold	V_{OUT} = +8V, R_L = 100Ω	0.4	0.6		V
Positive Output Swing	I_{OUT} = 100 mA	7.0	+8.0		V
Negative Output Swing	I_{OUT} = −100 mA		−8.0	−7.0	V
Positive Short Circuit Current	V_{IN} = 0V, R_L = 0Ω (Pulse Test; Duty Cycle ≤ 3%)	400	800		mA
Negative Short Circuit Current	V_{IN} = 1.5V, I_{IN} = 50 mA, R_L = 0Ω (Pulse Test, Duty Cycle ≤ 3%)	800	1000		mA
Turn-On Delay	V_{IN} = 1.5V, V_{OUT} = −3V		10	15	ns
Turn-Off Delay	V_{IN} = 1.5V, V_{OUT} = +3V		15	30	ns
On Supply Current	V_{IN} = 1.5V		45	60	mA

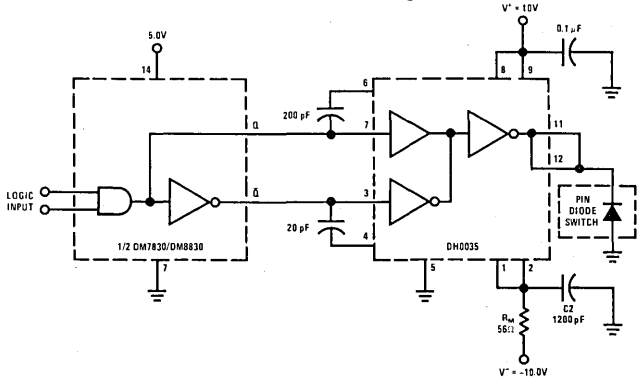
Note 1: Unless otherwise specified, these specifications apply for V^+ = 10.0V, V^- = −10.0V, pin 5 grounded, over the temperature range −55°C to +125°C for the DH0035, and 0°C to 85°C for the DH0035C.

Note 2: All typical values are for T_A = 25°C.

Note 3: Derate linearly at 10 mW/°C for ambient temperatures above 25°C.

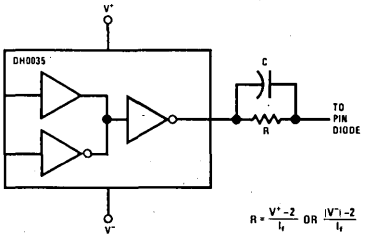
Typical Applications (Cont'd)

Grounded Anode Design



Note: Anode Grounded PIN diode: R_M = 56Ω limits diode forward current to 100 mA. Typical switching for HP33622A, RF turn-on 5 ns; turn-off 4 ns. C1 = 470 pF, C2 = 0.1 μF, R_M = 0Ω.

Alternate Current Limiting



National Semiconductor

DH0069 High Voltage Octal Driver for Electrostatic Printers

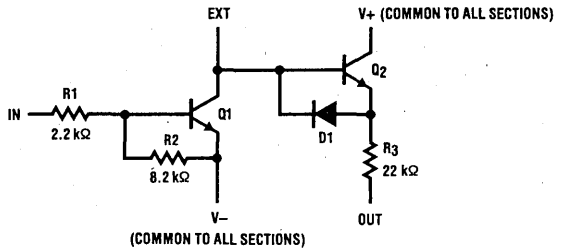
General Description

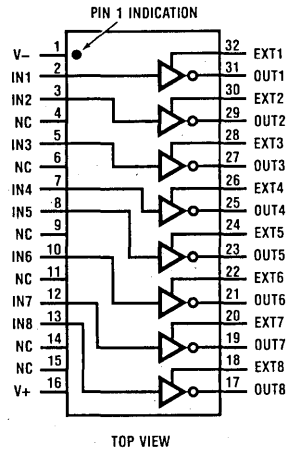
The DH0069 is an eight-channel, high-voltage driver capable of switching over 400V into capacitive loads such as stylus and segment drivers in electrostatic printers. Encased in a 32-pin dual-in-line package, the driver's inputs are TTL compatible and the output transistors are diode protected.

Features

- 8μs matched switching time
- 425V supply capability
- 8 drivers per package

Schematic and Connection Diagram





Order Number DH0069
See NS Package HY32A

Absolute Maximum Ratings (Note 1)

V^+	Supply Voltage	
	DH0069	425 V
V_{IN}	Input Voltage (Ref. V^-)	−6 to +18 V
P_D	Power Dissipation	
	$T_A \leq 25°C$	3.66 W
	Derate linearly at 35°C/W to 2.33W at 70°C	
	$T_C \leq 25°C$	6.25 W
	Derate linearly at 20°C/W to 4.0W at 70°C	
I_{OPK}	Peak Output Current	20 mA
	Short Circuit Duration	
	(R_{EXT} = 470 kΩ, V^+ = 425V, T_C = 25°C)	
	Any Single Output	10 Sec.
	All Outputs Simultaneously (1% Duty Cycle)	50 mS
T_A	Operating Temperature Range	0°C to 70°C
T_{STG}	Storage Temperature Range	−65°C to +150°C
	Lead Temperature (Soldering, 10 Sec.)	300°C

Electrical Characteristics R_{EXT} = 470 kΩ, T_A = 0°C to 70°C, V^+ = 400 V

DC Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.4	V
V_{OH}	High Level Output Voltage	V_{IN} = 0.4 V, R_L = 10 MΩ	380			V
V_{XSAT}	Saturation Voltage (All EXT Pins)	V_{IN} = 2.0 V, I_{EXT} = 2.0 mA (See Fig. 3)			2.0	V
	R_1		1.98	2.20	2.42	kΩ
	R_2		7.38	8.20	9.02	kΩ
	R_3		19.8	22.0	24.2	kΩ

AC Characteristics T_A = 25°C

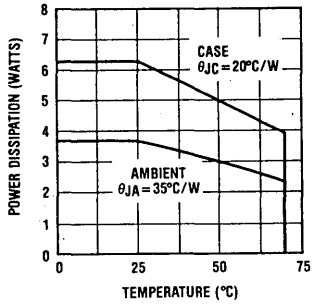
Parameter		Conditions (Note 2)		Min.	Typ.	Max.	Units
t_{PHL}	Propagation Delay High to Low Output	V_{IN} = 0.4 V to 2.0 V	C_L = 50 pF		4.0	10	μs
			C_L = 15 pF, R_L = 1 MΩ		1.8		μs
t_{PLH}	Propagation Delay Low to High Output	V_{IN} = 2.0 V to 0.4 V	C_L = 50 pF		14	24	μs
			C_L = 15 pF, R_L = 1 MΩ		12		μs
Δt_{PLH}	Differential Propagation Delay (Matching Between Sections)	C_L = 50 pF				8.0	μs

Note 1: Absolute maximum ratings are those values beyond which reliable operation cannot be guaranteed.

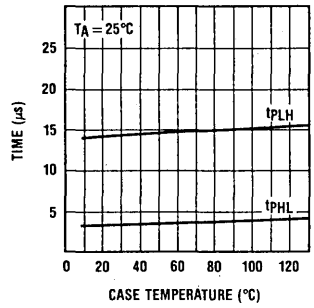
Note 2: C_L includes oscilloscope probe capacitance.

Typical Performance Characteristics and Applications

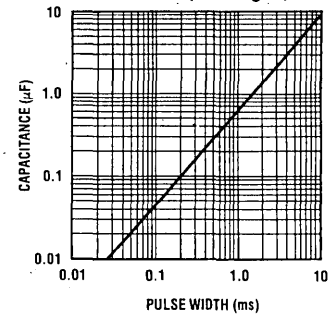
Maximum Power Dissipation



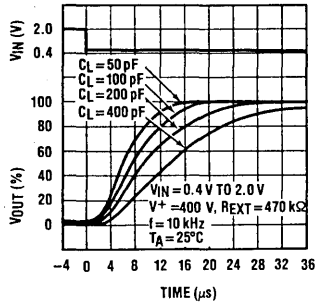
Switching Time Versus Temperature



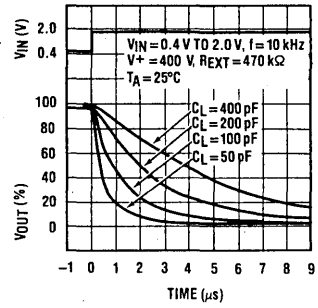
Recommended Coupling Capacitance Versus Pulse Width (See Fig. 1)



Response to Capacitive Loads (t_{PLH})



Response to Capacitive Loads (t_{PHL})



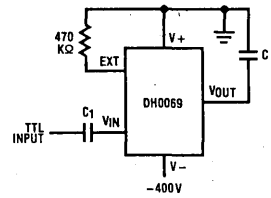
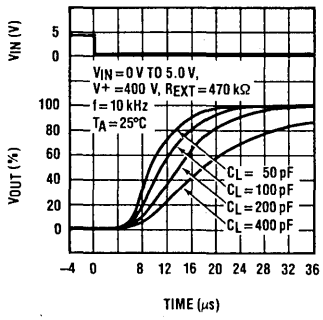
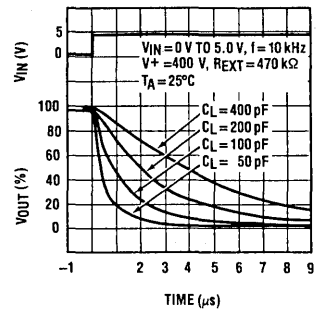


Figure 1. Capacitor Coupling Using a Negative Supply

Response to Capacitive Loads (t_{PLH})



Response to Capacitive Loads (t_{PHL})



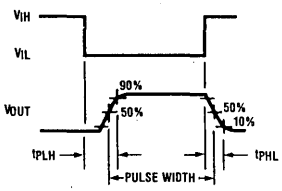


Figure 2. Waveforms

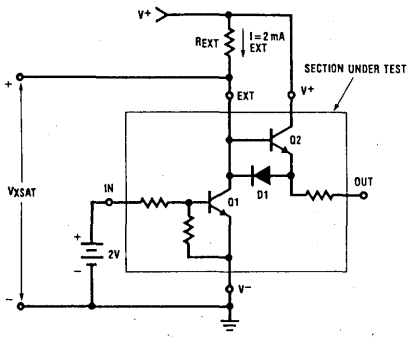


Figure 3. V_{XSAT} Test Circuit

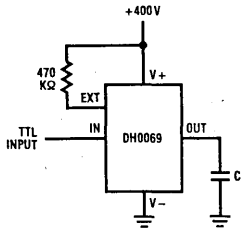


Figure 4. DH0069 Driving Capacitive Load

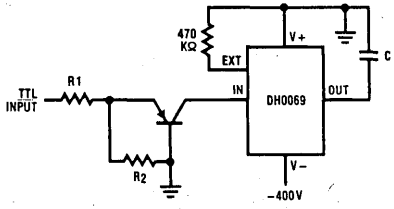


Figure 5. D.C. Coupled Driver Using a Negative Supply

Section 11

A/D Converters

Section 11. Analog-to-Digital Converters

Resolution (Bits)	Supplies (V)	Maximum Non-Linearity	Conversion Time	Part Number		Page Number
				−55°C to +125°C	−25°C to +85°C	
12	+5 to ±15	±½LSB	100μs	ADC1210	ADC1210C	11-14
12	+5 to ±15	±2LSB	100μs	ADC1211	ADC1211C	11-14
12	+5, ±15	±½LSB	25μs	—	ADC1280	11-4
12	+5, ±15	±2LSB	21μs	—	ADC1080	11-4

Note: See the Data Acquisition Handbook for National Semiconductor's complete line of converter products.

National Semiconductor

PRELIMINARY

ADC1080, ADC1280 12-Bit Successive Approximation A/D Converter

General Description

The ADC1080 and ADC1280 are complete successive approximation analog-to-digital converters that include an internal clock, reference and comparator.

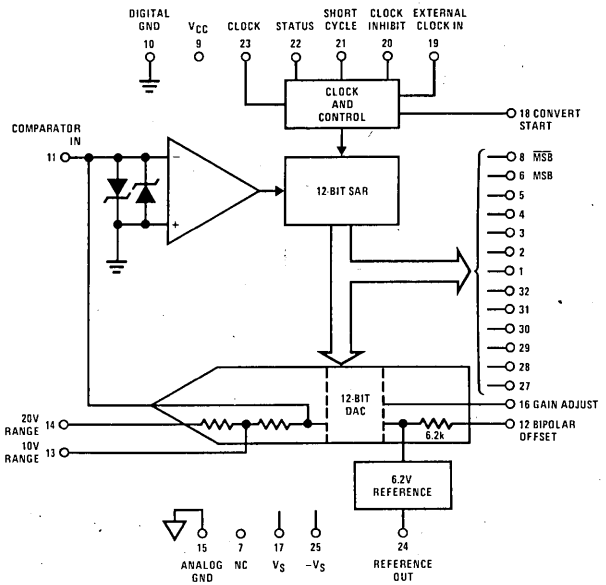
The design of the ADC1080 and ADC1280 includes scaling resistors that provide analog signal ranges of ±2.5V, ±5.0V, ±10V, 0V to 5V, or 0V to 10V. The 6.2V precision reference may be used for external applications. All digital signals are fully TTL compatible; output data may be read in both serial and parallel form.

The ADC1280 has a maximum linearity of 0.012% of FSR and the ADC1080 has a maximum linearity of 0.048% of FSR. Both grades are specified for use over the −25°C to +85°C temperature range and both are available in a 32-pin DIP.

Features

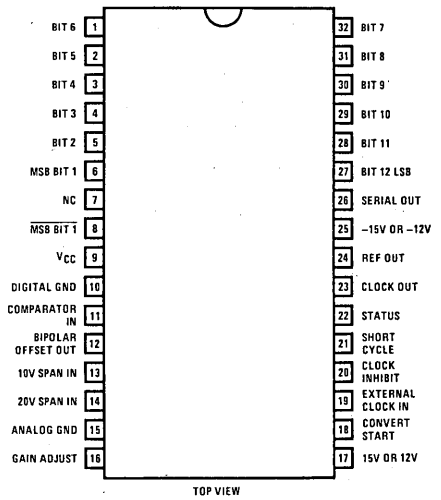
- Completely self-contained with internal reference, clock, and comparator
- High reliability exact replacement for ADC80
- ±1/2 LSB linearity for ADC1280
- Input voltage ranges of ±2.5V, ±5V, ±10V, 0V to 5V, and 0V to 10V
- 6.2V reference available for external use at 1.5 mA
- Conversion speed—22 μs
- Short cycle and external clock options for faster conversion time

Block Diagram



Connection Diagram

Dual-In-Line Package



Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	±18V	Operating Temperature Range	−55°C to +100°C
Logic Supply Voltage	7V	Storage Temperature Range	−65°C to +150°C
Reference Input Voltage (V_{REF})	0V, 18V	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$T_A = -25°C$ to $+85°C$, $V_S = \pm 11.4V$ to $\pm 16.00V$, $V_{CC} = 4.75V$ to $5.25V$ unless otherwise noted.

Parameter	Conditions	ADC1280 Min	ADC1280 Typ (Note 1)	ADC1280 Max	ADC1080 Min	ADC1080 Typ (Note 1)	ADC1080 Max	Units
CONVERTER CHARACTERISTICS								
Resolution		12			10			Bits
Linearity Error	$T_A = 25°C$			±0.012			±0.048	% FSR (Note 3)
Linearity Error Tempco				±3			±3	ppm of FSR/°C
Differential Linearity Error			±1/2			±1/2		LSB
No Missing Codes	(Note 2)	12			10			Bits
Full-Scale (Gain) Error	$T_A = 25°C$ (Note 4)		±0.1			±0.1		% FSR
Zero-Scale (Offset) Error	$T_A = 25°C$ (Note 4) Unipolar		±0.05			±0.05		%FSR
	$T_A = 25°C$ (Note 4) Bipolar		±0.1			±0.1		%FSR
Full-Scale (Gain) Tempco				±30			±30	ppm/°C
Zero-Scale (Offset) Tempco	Unipolar			±3			±3	ppm of FSR/°C
	Bipolar			±15			±15	ppm of FSR/°C
Analog Input Voltage Range	Unipolar	0V to 5V, 0V to 10V						V
	Bipolar	±2.5V, ±5V, ±10V						V
Input Impedance (Direct Input)	0V to 5V, ±2.5V		2.5k			2.5k		Ω
	0V to 10V, ±5V		5k			5k		Ω
	±10V		10k			10k		Ω
REFERENCE CHARACTERISTICS								
Reference Voltage		6.07	6.2	6.33	6.07	6.2	6.33	V
Tempco of Drift			10	20		10	20	ppm/°C
External Use Current				1.5			1.5	mA
Output Impedance			0.05	1.0		0.05	1.0	Ω
DIGITAL AND DC CHARACTERISTICS								
Logic 1 Input Voltage (Bit Off)	Incl Ext Clock Input	2.0			2.0			V
Logic 0 Input Voltage (Bit On)	Incl Ext Clock Input			0.8			0.8	V
Logic 1 Input Current	Incl Ext Clock Input, $V_{IN} = 2.5V$		0.05	1		0.05	1	μA
Logic 0 Input Current	Incl Ext Clock Input, $V_{IN} = 0V$			−100			−100	μA
Logic 0 Output Voltage	$I_{OUT} = 3.2$ mA			0.4			0.4	V
Logic 1 Output Voltage	$I_O = 360\ \mu A$	2.4			2.4			V
Short Circuit Output Current	$V_{CC} = Max$	−18		−57	−18		−57	mA
Power Supply Current	$T_A = 25°C$ I^+		16			16		mA
	$T_A = 25°C$ I^-		12			12		mA
	$T_A = 25°C$ I_{CC}		92			92		mA
Power Supply Sensitivity	V_S		0.003			0.003		FSR/% V_S
	V_{CC}		0.0015			0.0015		FSR/% V_{CC}

Electrical Characteristics (Continued)

$T_A = -25°C$ to $+85°C$, $V_S = \pm 11.4V$ to $\pm 16.00V$, $V_{CC} = 4.75V$ to $5.25V$ unless otherwise noted.

Parameter	Conditions		ADC1280			ADC1080			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
AC CHARACTERISTICS									
Conversion Time	$T_A = 25°C$	Internal Clock		22	25			21	μs
		External Clock		16	18			12	
Clock Frequency	Internal			575			575		kHz
Convert Command			100			100			ns

Note 1: All typical values are for $T_A = 25°C$.

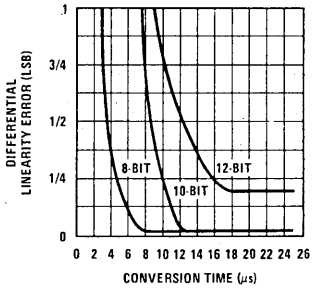
Note 2: Guarantees that for increasing analog voltage, the digital code increases. This specification guarantees monotonicity.

Note 3: FSR means "full-scale range" and is 20V for ±10V range, 10V for ±5V range.

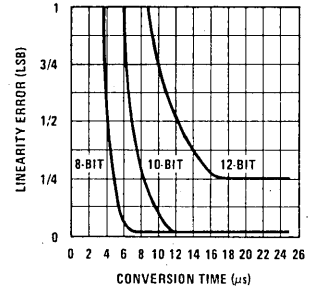
Note 4: Externally adjustable to zero.

Typical Performance Curves

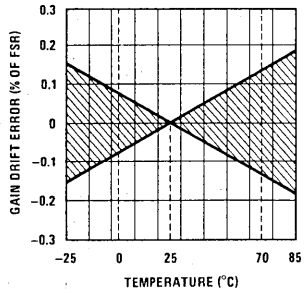
Linearity Error vs Conversion Time (Normalized)



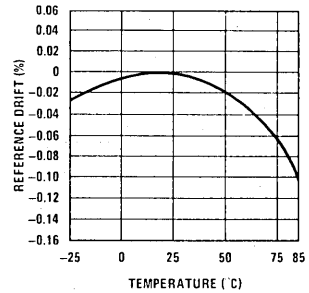
Differential Linearity Error vs Conversion Time (Normalized)



Maximum Gain Drift Error—% of FSR vs Temperature



Reference Drift—% Error vs Temperature



1.0 Definition of Terms and Applications

The accuracy of an A/D converter is described by the transfer function shown in *Figure 1.* There is an inherent quantization uncertainty of ± 1/2 LSB associated with the resolution.

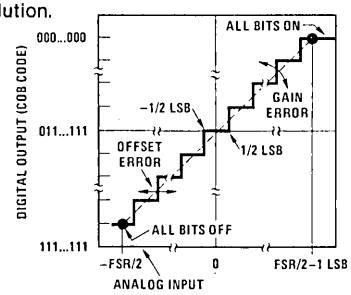


FIGURE 1. Transfer Characteristics for an Ideal Bipolar A/D

The remaining errors in the A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error, and power supply rejection. The matching and tracking errors in the ADC1080 and ADC1280 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ± 0.1% FSR for gain and ± 0.05% FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in *Figures 2 and 3.* Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full-scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size *(Figure 1).*

Monotonic behavior requires that the differential linearity error be less than 1 LSB; however, a monotonic converter can have missing codes.

There are three types of drift error over temperature: offset, gain, and linearity. Offset drift causes a shift of the transfer characteristics left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full-scale point.

1.1 Gain and Offset Error

Initial gain and offset errors are factory trimmed to ± 0.1% of FSR (± 0.05% for unipolar offset) at 25°C.

Gain and offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC1080 and ADC1280 as shown in *Figures 2 and 3.* Multiturn potentiometers with 100 ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10 kΩ to 100 kΩ. All resistors should be 20% or better. Pin 16 (gain adjust) may be left open if no external adjustment is required.

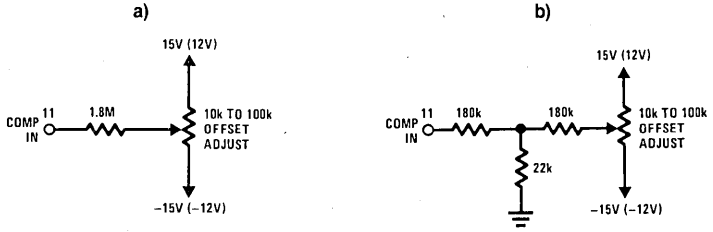


FIGURE 2. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment

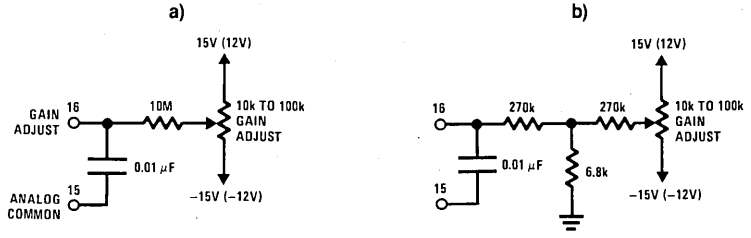


FIGURE 3. Two Methods of Connecting Optional Gain Adjust with a 0.6% Range of Adjustment

Adjustment Procedure

Offset—Connect the offset potentiometer as shown in *Figure 2*. Sweep the input through the end point transition voltage that should cause an output transition to all ones.

Adjust the offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

Gain—Connect the gain adjust potentiometer as shown in *Figure 3*. Sweep the input through the end point transition voltage that should cause an output transition to all zeros.

Adjust the gain potentiometer until the actual end point transition voltage occurs E_{IN}^{ON}. Table I details the transition voltage levels required.

1.2 Accuracy Drift vs Temperature

Three major drift parameters degrade A/D converter accuracy over temperature: they are gain, offset and linearity drift. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\in g^2 + \in o^2 + \in e^2}$$

where $\in g$ = gain drift error (ppm/°C)

$\in o$ = offset drift error (ppm of FSR/°C)

$\in e$ = linearity error (ppm of FSR/°C)

For *unipolar* operation, the total RSS drift is ±30.3 ppm/°C and for *bipolar* operation, the total RSS drift is ±33.7 ppm/°C.

1.3 Accuracy vs Speed

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC1080 and ADC1280 are shown in *Figures 3 and 4.*

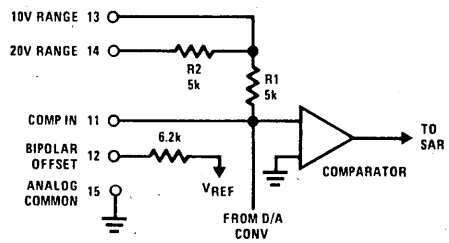


FIGURE 4. Input Scaling Circuit

The ADC1080 and ADC1280 conversion speeds are specified for a maximum linearity error of ± 1/2 LSB and a differential linearity error of ± 1/2 LSB with the internal clock. Faster conversion speeds up to 23 μs for 12 bits, 12 μs for 10 bits, and 6 μs for 8 bits are possible with an external clock.

1.4 Power Supply Sensitivity

Changes in the DC power supplies will affect the accuracy of the ADC1080 and ADC1280. Normally, regulated power supplies with 1% or less ripple are recommended.

1.5 Layout Precautions

Analog and digital commons are not connected internally in the ADC1080 and ADC1280, but should be connected together as close to the unit as possible, preferably to a large ground plane under the A/D. If these grounds must be run separately, use a wide conductor pattern between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

1.6 Input Scaling

The ADC1080 and ADC1280 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table I. See *Figure 4* for circuit details.

TABLE I. INPUT SCALING CONNECTIONS

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
± 10V	COB or CTC	11	Input Signal	14
± 5V	COB or CTC	11	Open	13
± 2.5V	COB or CTC	11	Pin 11	13
0V to 5V	CSB	15	Pin 11	13
0V to 10V	CSB	15	Open	13

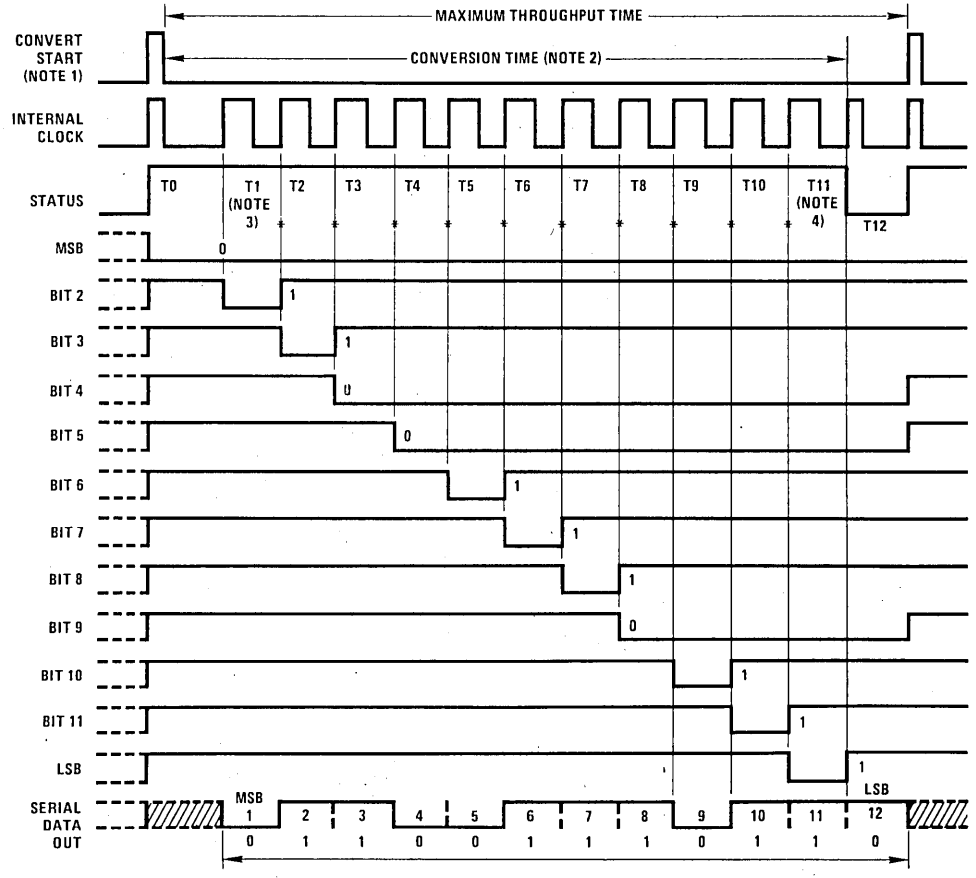
2.0 Functional Description

On receipt of a CONVERT START command, the ADC1080 and ADC1280 convert the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

2.1 Timing

The Timing Diagram is shown in *Figure 5*. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t0, B1 is reset and B2-B12 are set unconditionally. At t1 the bit 1 decision is made (keep) and bit 2 is unconditionally reset. At t2, the bit 2 decision is made (keep) and bit 3 is reset unconditionally. This sequence continues until the bit 12 (LSB) decision (keep) is made at t12. After a 40 ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic 0 state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see *Figure 5*).



Note 1: The convert start pulse width is 100 ns min and must remain low during a conversion. The conversion is initiated by the rising edge of the convert command.

Note 2: 25 μs for 12 bits and 21 μs for 10 bits (max).

Note 3: MSB decision

Note 4: LSB decision 40 ns prior to the status going low.

*Bit decisions

FIGURE 5. Timing Diagram (Binary Code 011001110110)

Incorporation of this 40 ns delay guarantees that the parallel (and serial) data are valid at the Logic 1 to Logic 0 transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

2.2 Digital Output Data

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether bit 1 (pin 6) or its logical inverse bit 1 (pin 8) is used as the MSB. Parallel data becomes valid approximately 40 ns before the STATUS flag returns to Logic 0, permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200 ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in *Figure 5.* There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in *Figure 5.* The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

2.3 Short Cycle Input

A short cycle input, pin 21, permits the timing cycle shown in *Figure 5* to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 21 is connected to 5V (pin 9). When 10-bit resolution is desired, pin 21 is connected to bit 11 output pin 28. The conversion cycle then terminates, and the STATUS flag resets after the bit 10 decision (t10 + 40 ns in the Timing Diagram of *Figure 5*). Short cycle pin connections and associated maximum 12-bit, 10-bit and 8-bit conversion times are summarized in Table II.

TABLE II. SHORT CYCLE CONNECTIONS

Connect Short Cycle Pin 21 To Pin	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
9	12	0.024	25	t12 + 40 ns
28	10	0.100	21	t10 + 40 ns
30	8	0.390	17	t8 + 40 ns

2.4 Control Modes

The timing sequence of the ADC1080 and ADC1280 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in *Figures 6-9.*

2.5 Calibration

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in *Figures 10 and 11*, are used for device calibration. To prevent interaction of these two adjustments, zero is always adjusted first and then gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and − FS for bipolar input ranges). Gain is adjusted with the analog input near the most postive end of the analog range.

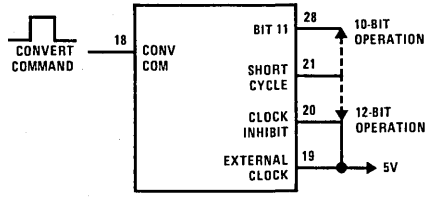


FIGURE 6. Internal Clock—Normal Operating Mode. Conversion Initiated by the Rising Edge of the Convert Command. The Internal Clock Runs Only During Conversion.

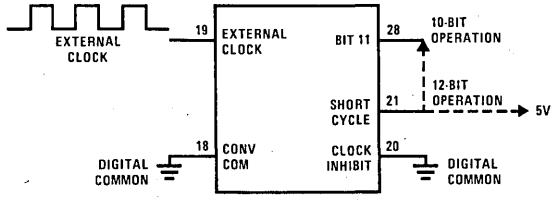


FIGURE 7. Continuous Conversion with External Clock. Conversion is Initiated by 14th Clock Pulse. Clock Runs Continuously.

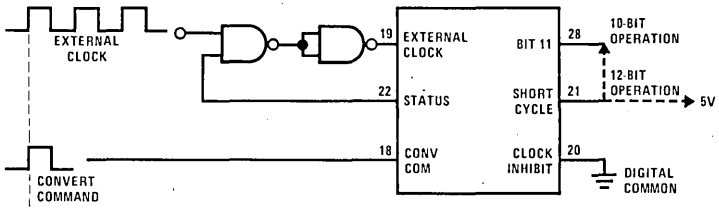


FIGURE 8. Continuous External Clock. Conversion Initiated by Rising Edge of Convert Command. The Convert Command Must be Synchronized with Clock.

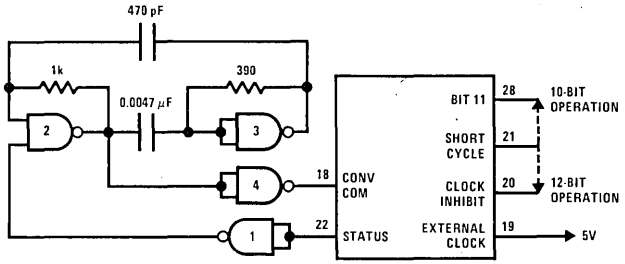


FIGURE 9. Continuous Conversion with Internal Clock. Conversion is Initiated by the 14th Clock Pulse. Clock Runs Continuously. The Oscillator Formed by Gates 2 and 3 Insures that the Conversion Process will Start When Logic Power is First Turned On.

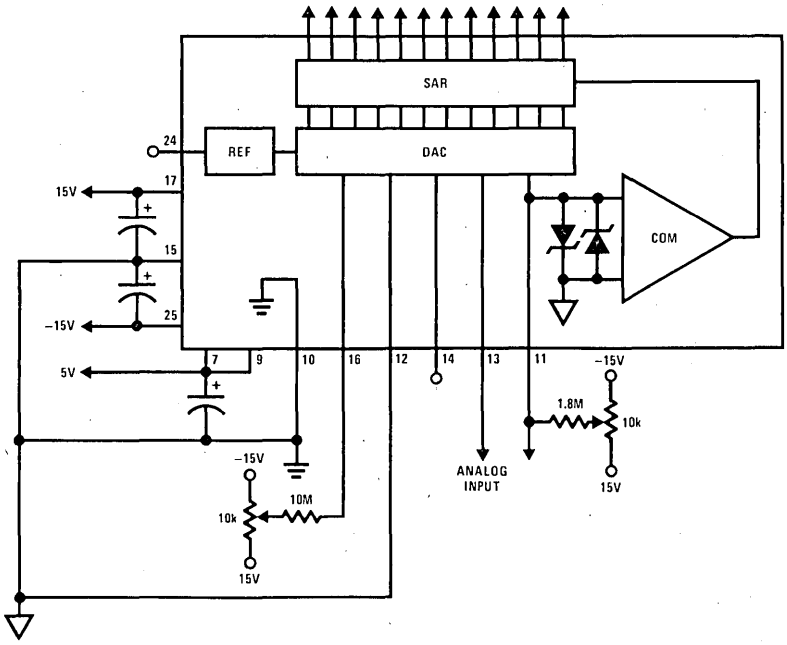


FIGURE 10. Analog and Power Connections for Unipolar 0V–10V Input Range

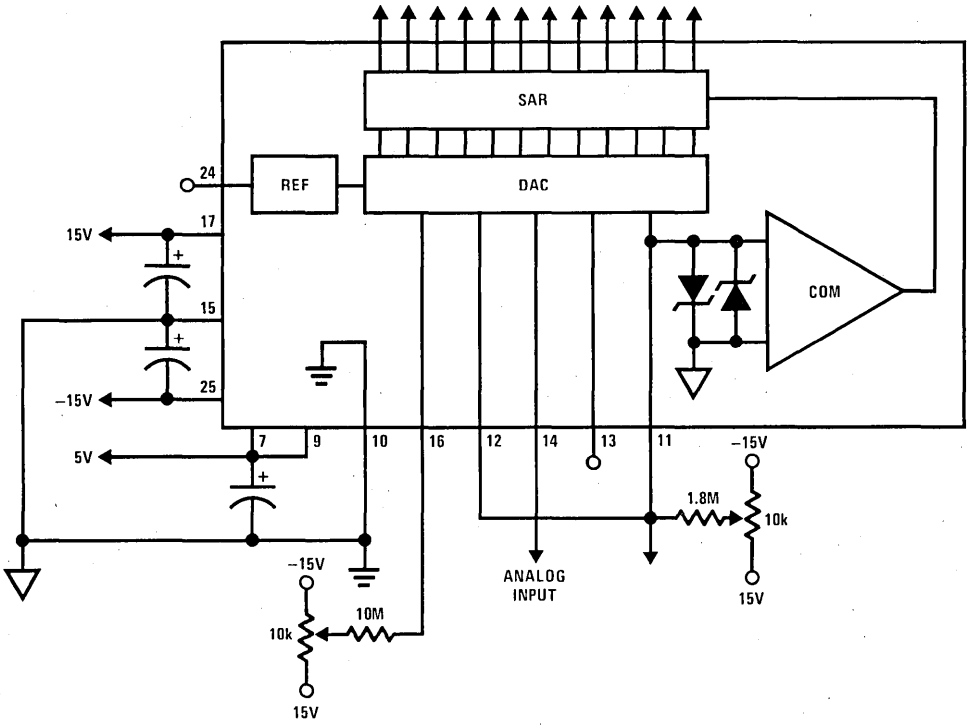


FIGURE 11. Analog and Power Connections for Bipolar ±10V Input Range

0V to 10V Range: Set analog input to +1 LSB = +0.0024V. Adjust zero for digital output = 1 1 1 1 1 1 1 1 1 1 1 1 0. Zero is now calibrated. Set analog input to +FSR −2 LSB = +9.9952V. Adjust gain for 0 0 0 0 0 0 0 0 0 0 0 0 1 digital output code; full-scale (gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 0 1 1 1 1 1 1 1 1 1 1 1.

−10V to +10V Range: Set analog input to −9.9951V; adjust zero for 1 1 1 1 1 1 1 1 1 1 1 0 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust gain for 0 0 0 0 0 0 0 0 0 0 0 0 1 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0 1 1 1 1 1 1 1 1 1 1 1.

Other Ranges: Representative digital coding for 0V to 10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0V to 5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0V to 10V and −10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4 LSB using the static adjustment procedure described in paragraph 1.1. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level.

TABLE III. INPUT VOLTAGES AND CODE DEFINITIONS

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	± 10V	± 5V	± 2.5V	0V to 20V	0V to 10V	0V to 5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13 mV	39.06 mV	19.53 mV	78.13 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	19.53 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	4.88 mV	2.44 mV	1.22 mV
Transition Values							
MSB LSB							
0 0 0...0 0 0****	+ Full-Scale	10V − 3/2 LSB	5V − 3/2 LSB	2.5V − 3/2 LSB	20V − 3/2 LSB	10V − 3/2 LSB	5V − 3/2 LSB
0 1 1...1 1 1	Mid-Scale	0	0	0	10V	5V	2.5V
1 1 1...1 1 0	− Full-Scale	−10V + 1/2 LSB	−5V + 1/2 LSB	−2.5V + 1/2 LSB	0 + 1/2 LSB	0 + 1/2 LSB	0 + 1/2 LSB

*COB = Complementary Offset Binary.

**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.

***CSB = Complementary Straight Binary.

****Voltages given are the nominal value for transition to the code specified.

Ordering Information

Temperature Range		−25°C to +85°C
Linearity (Accuracy)	0.012%	*ADC1280HCD ADC80AG-12 ADC80AGZ-12
	0.048%	*ADC1080HCD ADC80AG-10 ADC80AGZ-10
Package		D32B

*Devices may be ordered by either part number

Contact National Semiconductor Corp., Product Marketing Group for Package and Ordering Information

National Semiconductor

ADC1210, ADC1211 12-Bit CMOS A/D Converters

General Description

The ADC1210, ADC1211 are low power, medium speed, 12-bit successive approximation, analog-to-digital converters. The devices are complete converters requiring only the application of a reference voltage and a clock for operation. Included within the device are the successive approximation logic, CMOS analog switches, precision laser trimmed thin film R-2R ladder network and FET input comparator.

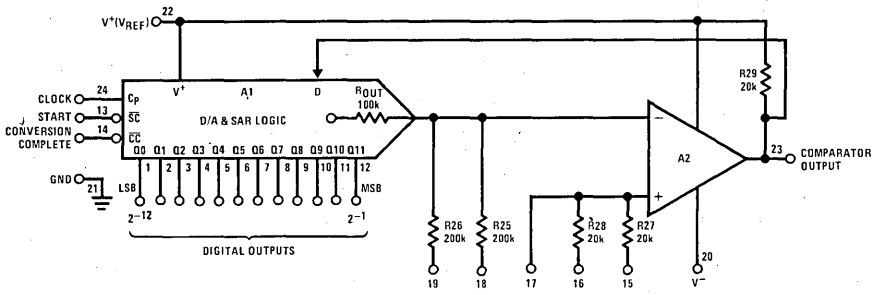
The ADC1210 offers 12-bit resolution and 12-bit accuracy, and the ADC1211 offers 12-bit resolution with 10-bit accuracy. The inverted binary outputs are directly compatible with CMOS logic. The ADC1210, ADC1211 will operate over a wide supply range, convert both bipolar and unipolar analog inputs, and operate in either a continuous conversion mode or logic-controlled START-STOP conversion mode. The devices are capable of making a 12-bit conversion in 100 μs typ, and can be connected to convert 10 bits in 30 μs.

Both devices are available in military and industrial temperature ranges.

Features

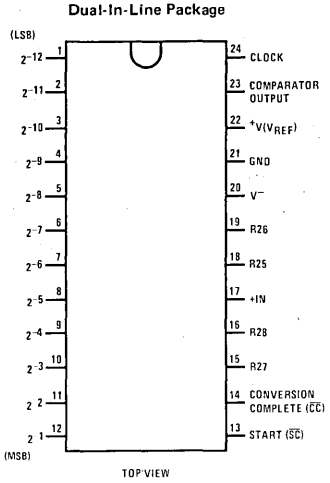
- 12-bit resolution
- ±1/2 LSB linearity
- Single +5V to ±15V supply range
- 100 μs 12-bit, 30 μs 10-bit conversion rate
- CMOS compatible outputs
- Bipolar or unipolar analog inputs
- 200 kΩ analog input impedance
- Low cost

Block Diagram



Connection Diagram

Dual-In-Line Package



Order Number ADC1210HCD, ADC1211HCD, ADC1210HD or ADC1211HD
See NS Package D24D

Absolute Maximum Ratings

Maximum Reference Supply Voltage (V^+)	16V
Maximum Negative Supply Voltage (V^-)	−20V
Voltage At Any Logic Pin	$V^+ + 0.3V$
Analog Input Voltage	±15V
Maximum Digital Output Current	±10 mA
Maximum Comparator Output Current	50 mA
Comparator Output Short-Circuit Duration	5 Seconds
Power Dissipation	See Curves
Operating Temperature Range	
ADC1210HD, ADC1211HD	−55°C to +125°C
ADC1210HCD, ADC1211HCD	−25°C to + 85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Notes 1 and 2)

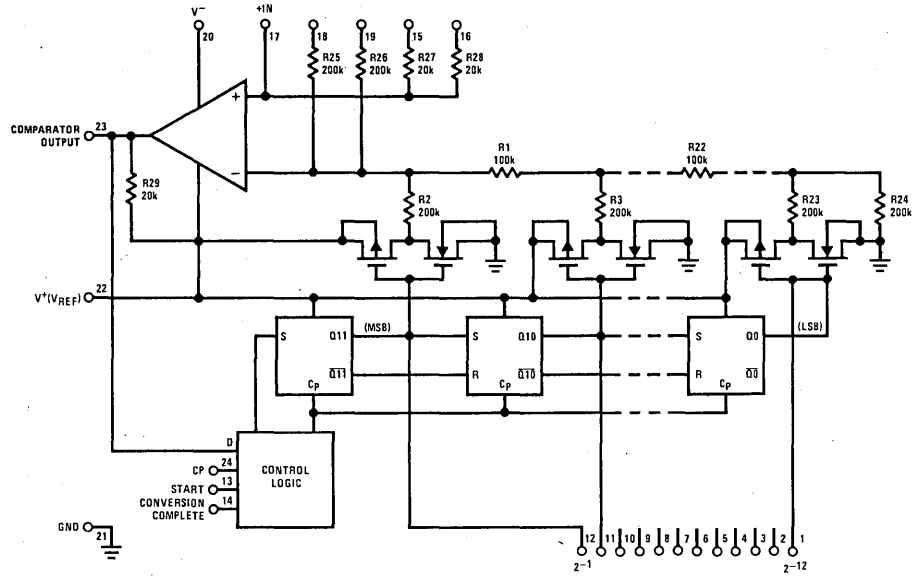
PARAMETER	CONDITIONS	ADC1210			ADC1211			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		12			12			Bits
Linearity Error	(Note 3)							
	f_{CLK} = 65 kHz, T_A = 25°C			±0.0122			±0.0488	% FS
	f_{CLK} = 65 kHz			±0.0244				% FS
Full Scale Error	T_A = 25°C, Unadjusted			0.1			0.25	% FS
Zero Scale Error	T_A = 25°C, Unadjusted			0.1			0.25	% FS
Quantization Error				±1/2			±1/2	LSB
Input Resistor Values	R27, R28		20			20		kΩ
Input Resistor Values	R25, R26		200			200		kΩ
Input Resistor Ratios	R25/R26, R27/R28			0.1			0.1	%
Logic "1" Input Voltage		8			8			V
Logic "0" Input Voltage				2			2	V
Logic "1" Input Current	V_{IN} = 10.24V			1			1	μA
Logic "0" Input Current	V_{IN} = 0V			−1			−1	μA
Logic "1" Output Voltage	$I_{OUT} \leq -1$ μA	9.2			9.2			V
Logic "0" Output Voltage	$I_{OUT} \leq 1$ μA			0.5			0.5	V
Positive Supply Current	V^+ = 15V, f_{CLK} = 65 kHz, T_A = 25°C		5	8		5	8	mA
Negative Supply Current	V^- = −15V, T_A = 25°C		4	6		4	6	mA

AC Electrical Characteristics T_A = 25°C, (Notes 1 and 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time			100	200	μs
Maximum Clock Frequency			130	65	kHz
Clock Pulse Width		100	50		ns
Propagation Delay From Clock to Data Output (Q0 to Q11)	$t_r \leq t_f \leq 10$ ns		60	150	ns
Propagation Delay From Clock to Conversion Complete	$t_r \leq t_f \leq 10$ ns		60	150	ns
Clock Rise and Fall Time				5	μs
Input Capacitance			10		pF
Start Conversion Set-Up Time		30			ns

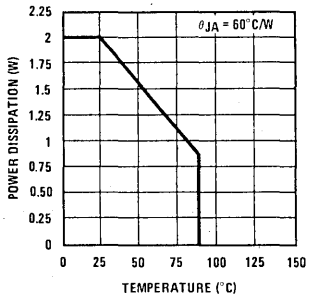
Note 1: Unless otherwise noted, these specifications apply for V^+ = 10.240V, V^- = −15V, over the temperature range −55°C to +125°C for the ADC1210HD,ADC1211HD, and −25°C to +85°C for the ADC1210HCD, ADC1211HCD.
Note 2: All typical values are for T_A = 25°C.
Note 3: Unless otherwise noted, this specification applies over the temperature range −25°C to +85°C. Provision is made to adjust zero scale error to 0V and full-scale to 10.2375V during testing. Standard linearity test circuit is shown in *Figure 5a.*

Schematic Diagram

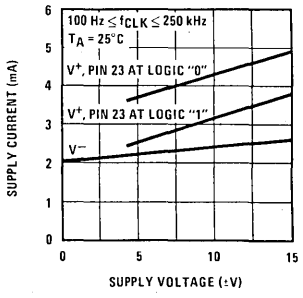


Note: 3 bits shown for clarity

Power Dissipation vs Temperature



Supply Current vs Supply Voltage



1.0 THEORY OF OPERATION

The ADC1210, ADC1211 are successive approximation analog-to-digital converters, i.e., the conversion takes place 1 bit at a time by comparing the output of the internal D/A to the (unknown) input voltage. The START input (pin 13), when taken low, causes the register to reset synchronously on the next CLOCK low-to-high transition. The MSB, Q11 is set to the low state, and the remaining bits, Q0 through Q10, will be set to the high state. The register will remain in this state until the $\overline{SC}$ input is taken high. When START goes high, the conversion will begin on the low-to-high transition of the CLOCK pulse. Q11 will then assume the state of pin 23. If pin 23 is high, Q11 will be high; if pin 23 is low, Q11 will remain low. At the same time, the next bit, Q10 is set low. All remaining bits, Q0–Q9 will remain unchanged (high). This process will continue until the LSB (Q0) is found. When the conversion process is completed, it is indicated by CONVERSION COMPLETE ($\overline{CC}$) (pin 14) going low. The logic levels at the data output pins (pins 1–12) are the complemented-binary representation of the converted analog signal with Q11 being the MSB and Q0 being the LSB. The register will remain in the above state until the $\overline{SC}$ is again taken low.

An application example is shown in *Figure 1*. In this case, a 0 to −10.2375V input is being converted using the ADC1210 with V^+ = 10.240V, V^- = −15V. *Figure 1b* is the timing diagram for full scale input. *Figure 1c* is the timing diagram for zero scale input, *Figure 1d* is the timing diagram for −3.4125V input (010101010101 = output).

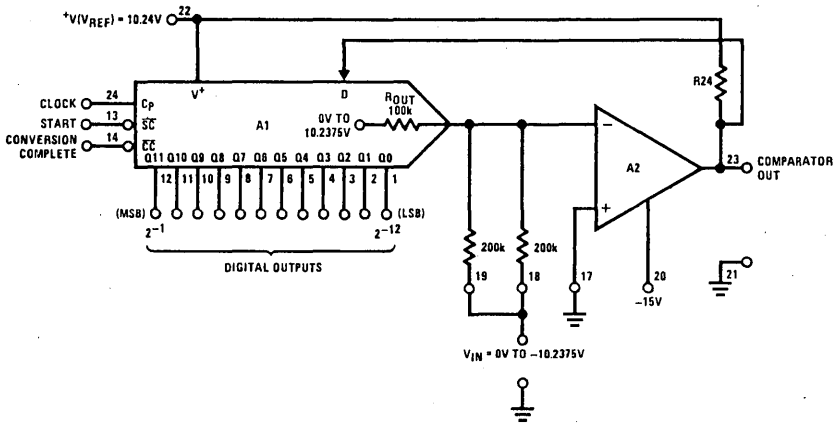


FIGURE 1a. ADC1210 Connected for 0V to −10.2375V (Natural Binary Output)

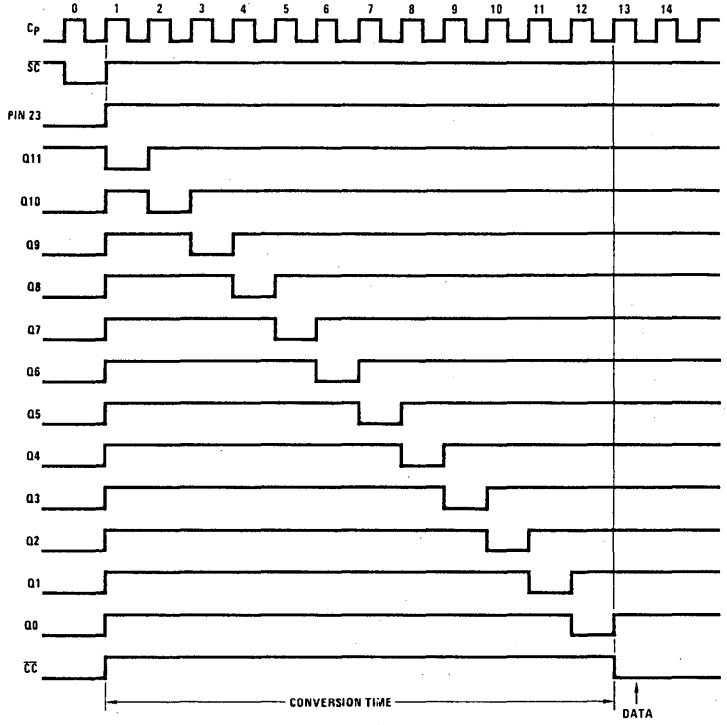


FIGURE 1b. Timing Diagram for V_{IN} = Full Scale Input

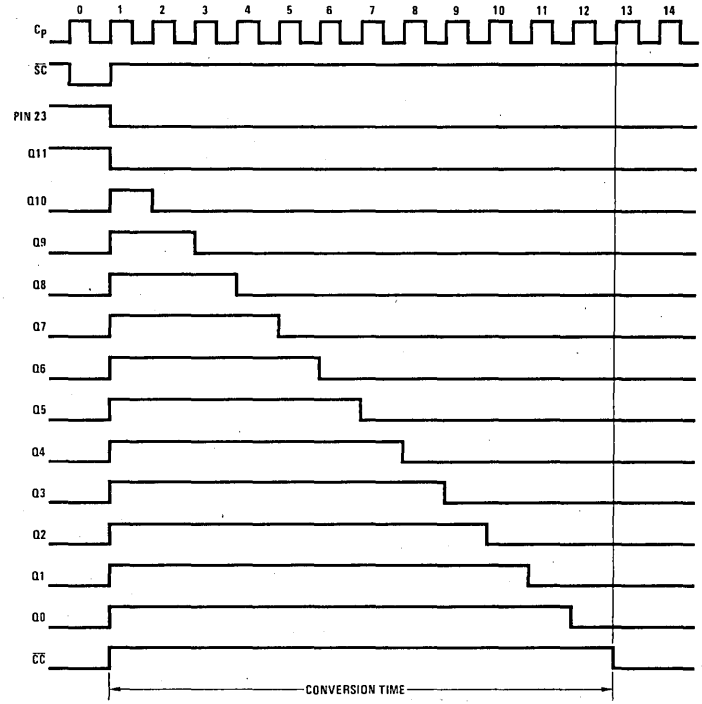


FIGURE 1c. Timing Diagram for V_{IN} = Zero Scale

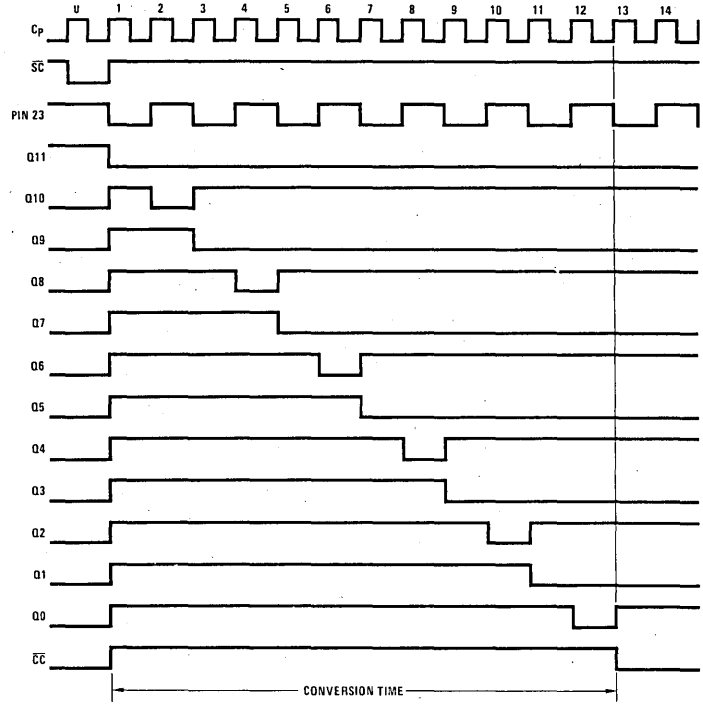


FIGURE 1d. Timing Diagram for V_{IN} = −3.4125V (010101010101)

TABLE I. Pin Assignments and Explanations

PIN NUMBER	MNEMONIC	FUNCTION
1–12	Q11–Q0	Digital (data) output pins. This information is a parallel 12-bit complemented binary representation of the converted analog signal. All data is valid when "Conversion Complete" goes low. Logic levels are ground and V^+.
13	$\overline{SC}$	Start Conversion is a logic input which causes synchronous reset of the successive approximation register and initiates conversion. Logic levels are ground and V^+.
14	$\overline{CC}$	"Conversion Complete" is a digital output signal which indicates the status of the converter. When $\overline{CC}$ is high, conversion is taking place, when low conversion is completed. Logic levels are ground and V^+.
15, 16	R27, R28	R27 and R28 are two application resistors connected to the comparator non-inverting input. The resistors may be used in various modes of operation. Their nominal values are 20 kΩ each. See Applications section.
17	+IN	Non-inverting input of the analog comparator. This node is used in various configurations and for compensation of the loop. See Applications section.
18, 19	R25, R26	R25 and R26 are two application resistors that are tied internally to the inverting input of the comparator. Their nominal values are 200 kΩ each. See Applications section. The R-2R ladder network will have the same temperature coefficient as these resistors.
20	V^-	Negative supply voltage for bias of the analog comparator. Optionally may be grounded or operated with voltages to −20V.
21	GND	Ground for both digital and analog signals.
22	V^+(VREF)	V^+ sets both maximum full scale and input and output logic levels.
23	CO	Comparator output.
24	Cp	Clock is an input which causes the successive approximation (shift) register to advance through the conversion sequence. Logic levels are ground and V^+.

2.0 APPLICATIONS

2.1 Power Supply Considerations and Decoupling

Pin 22 is both the positive supply and voltage reference input to the ADC1210, ADC1211. The magnitude of V^+ determines the input logic "1" threshold and the output voltage from the CMOS SAR. The device will operate over a range of V^+ from 5V to 15V. However, in order to preserve 12-bit accuracy, V^+ should be well regulated (0.01%) and isolated from external switching transients. It is therefore recommended that pin 22 be decoupled with a 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic disc capacitor.

The V^- supply (pin 20) provides negative bias for the FET comparator. Although pin 20 may be grounded in some applications, it must be at least 2V more negative than the most negative analog input signal. When a negative supply is used, pin 20 should also be bypassed with 4.7 μF in parallel with 0.1 μF.

Grounding and circuit layout are extremely important in preserving 12-bit accuracy. The user is advised to employ separate digital and analog returns, and to make these PC board traces as "heavy" as practical.

2.2 Short Cycle for Improved Conversion Time (Figure 2)

The ADC1210, ADC1211 counting sequence may be truncated to decrease conversion time. For example, when using the ADC1211, 2 clock intervals may be "saved" if 10-bit conversion accuracy is taking place. The Q2 output should be "OR'd" with CONVERSION COMPLETE ($\overline{CC}$) in order to ensure that the register does not lock-up upon power turn-on.

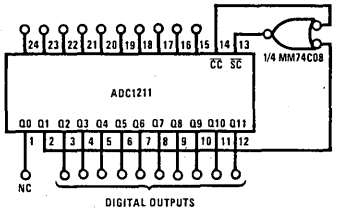


FIGURE 2. Short Cycling the ADC1211 to Improve 10-Bit Conversion Time (Continuous Conversion)

2.3 Logic Compatibility

The ADC1210, ADC1211 is intended to interface with CMOS logic levels: i.e., the logic inputs and outputs are directly compatible with series 54C/74C and CD4000 family of logic components. The outputs of the ADC1210, ADC1211 will not drive LPTTL, TTL or PMOS logic directly without degrading accuracy. Various recommended interface techniques are shown in *Figures 3 and 4.*

2.4 Operating Configurations

Several recommended operating configurations are shown in *Figure 5.*

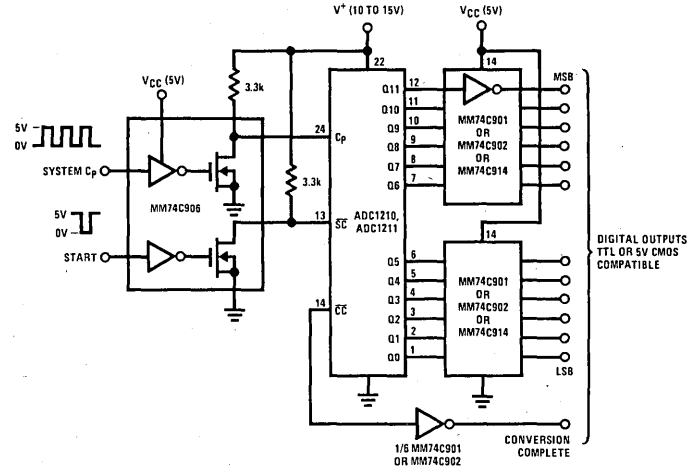


FIGURE 3. Interfacing an ADC1210, ADC1211 Running on $V^+ > V_{CC}$. Example: $V^+ = 10.24V$, System $V_{CC} = 5V$

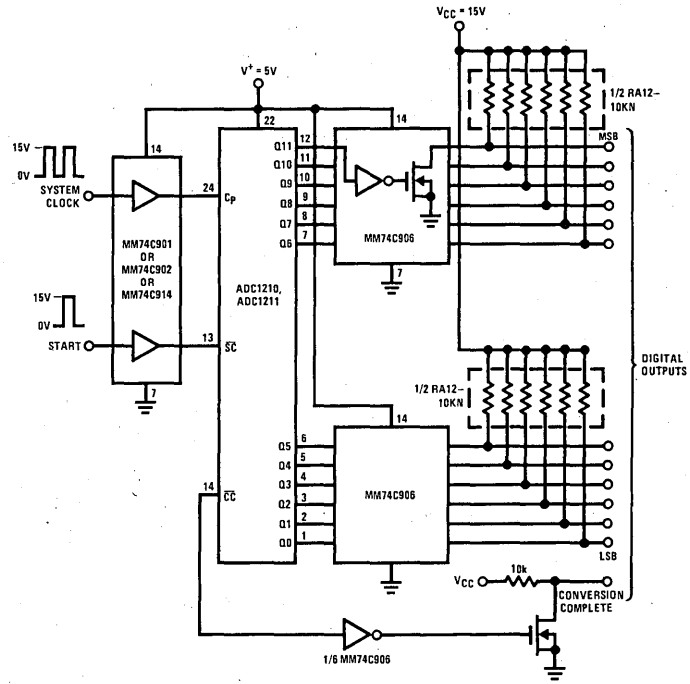
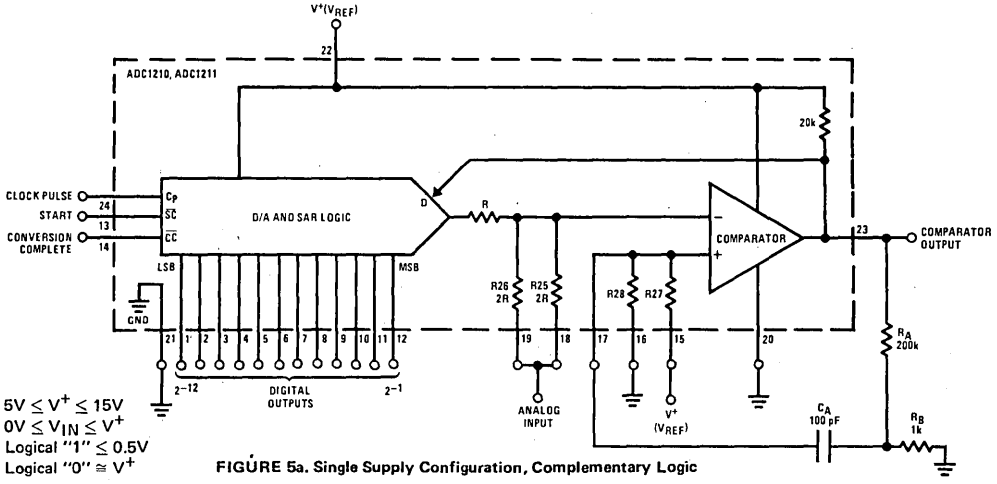


FIGURE 4. Interfacing an ADC1210, ADC1211 Running on $V^+ < V_{CC}$. Example: $V^+ = 5V$, $V_{CC} = 15V$

2.5 Offset and Full Scale Adjust

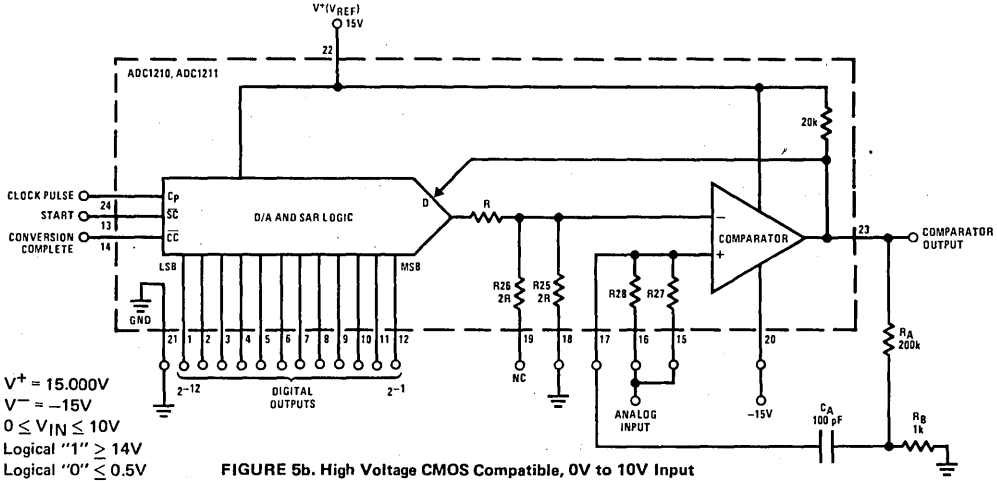
A variety of techniques may be employed to adjust Offset and Full Scale on the ADC1210, ADC1211. A straight-forward Full Scale Adjust is to incrementally vary V^+ (V_{REF}) to match the analog input voltage. A recommended technique is shown in *Figure 6*. An LM199 and low drift op amp (e.g., the LH0044) are used to provide the precision reference. The ADC1210, ADC1211 is put in the continuous convert mode by shorting pins 13 and 14. An analog voltage equal to V_{REF} minus 1 1/2 LSB (10.23625V) is applied to pins 18 and 19, and R1 is adjusted until the LSB flickers equally between logic "1" and logic "0" (all other outputs must be stable logic "0"). Offset Null is accomplished by then applying an analog input voltage equal to 1/2 LSB at pins 18 and 19. R2 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other bits are stable). In the circuit of *Figure 6*, the ADC1210, ADC1211 is configured for Complementary Binary logic and the values shown are for $V^+ = 10.240V$, $V_{FS} = 10.2375V$, LSB = 2.5 mV.

An alternate technique is shown in *Figure 7*. In this instance, an LH0071 is used to provide the reference voltage. An analog input voltage equal to V_{REF} minus 1 1/2 LSB (10.23625V) is applied to pins 18 and 19.



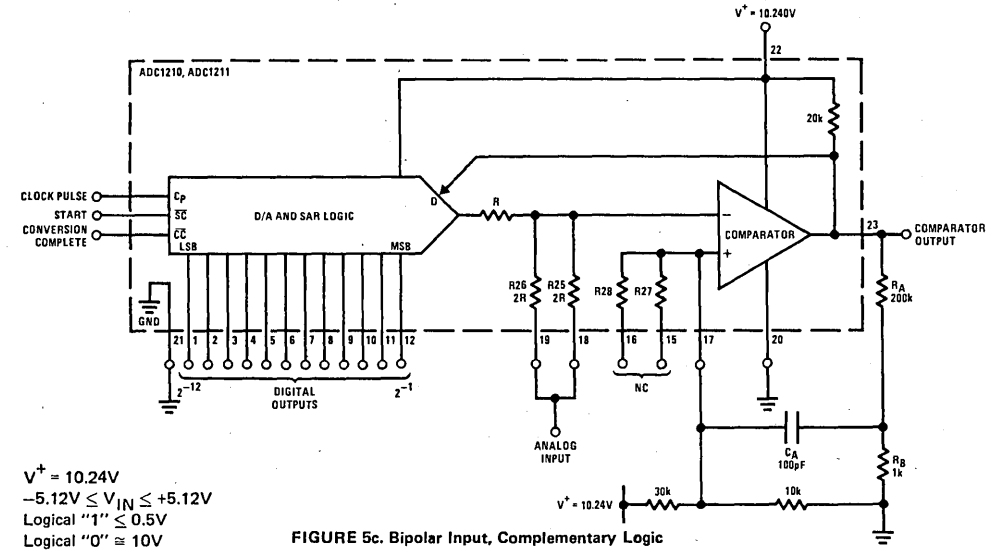
$5V \leq V^+ \leq 15V$
$0V \leq V_{IN} \leq V^+$
Logical "1" $\leq 0.5V$
Logical "0" $\cong V^+$

FIGURE 5a. Single Supply Configuration, Complementary Logic



$V^+ = 15.000V$
$V^- = -15V$
$0 \leq V_{IN} \leq 10V$
Logical "1" $\geq 14V$
Logical "0" $\leq 0.5V$

FIGURE 5b. High Voltage CMOS Compatible, 0V to 10V Input



$V^+ = 10.24V$
$-5.12V \leq V_{IN} \leq +5.12V$
Logical "1" $\leq 0.5V$
Logical "0" $\cong 10V$

FIGURE 5c. Bipolar Input, Complementary Logic

Applications Information (Continued)

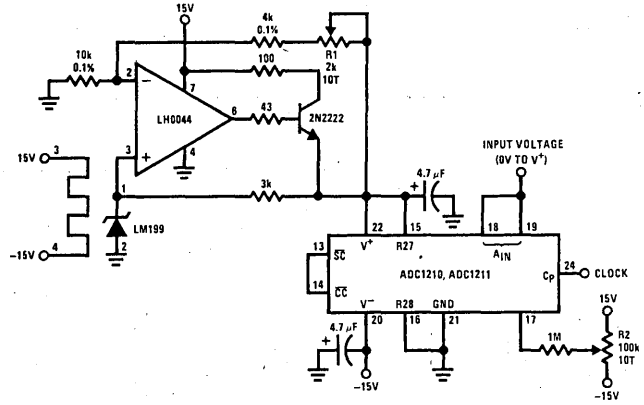


FIGURE 6. Offset and Full Scale Adjustment for Complementary Binary

R1 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other outputs must be a stable logic "0"). For Offset Null, an analog voltage equal to 1/2 LSB (1.25 mV) is then applied to pins 18 and 19, and R2, is adjusted until the LSB output flickers equally between logic "1" and "0".

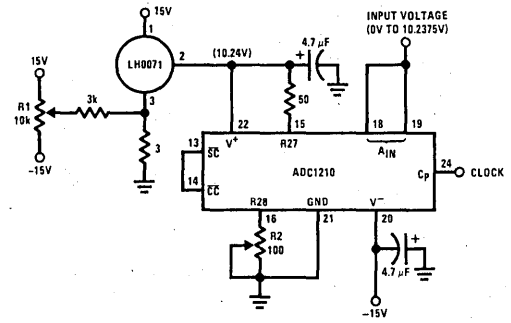


FIGURE 7. Offset and Full-Scale Adjustment Technique Using LH0071

In both techniques shown, adjusting the Full-Scale first and then Offset minimizes adjustment interaction. At least one iteration is recommended as a self-check.

2.6 Start Pulse Considerations

To assure reliable conversion accuracy, the $\overline{\text{START}}$ ($\overline{\text{SC}}$) pulse applied to pin 13 of the ADC1210 should be synchronized to the conversion clock. One simple way to do that is the circuit shown in *Figure 8.* Note that once a conversion cycle is initiated, the $\overline{\text{START}}$ signal cannot effect the conversion operation until it is completed.

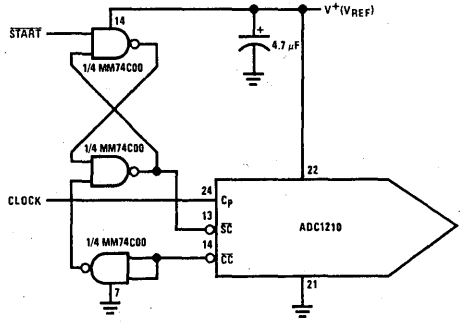


FIGURE 8. Synchronizing the $\overline{\text{START}}$ Pulse

The circuit insures that in no case can the ADC1210 make an error in the Most Significant Bit (MSB) decision. Without the circuit, it is possible for energy from the trailing edge of an asynchronous $\overline{\text{START}}$ pulse to be coupled into the ADC1210's comparator. If the analog input is near half-scale, the charge injected can force an error in the MSB decision. The circuit allows one clock period for this energy to dissipate before the decision is recorded.

2.7 ADC1210 Conversion at 26 μs

The ADC1210 can run at 500 kHz clock frequency, or 12-bit conversion time of 26 μs *(Figure 9)*. The comparator output is clamped low until the successive approximation register (SAR) is ready to strobe in the data at the rising edge of the conversion clock. Comparator oscillation is suppressed and kept from influencing the conversion decisions, eliminating the need for the AC hysteresis circuit above clock frequency of 65 kHz that is recommended.

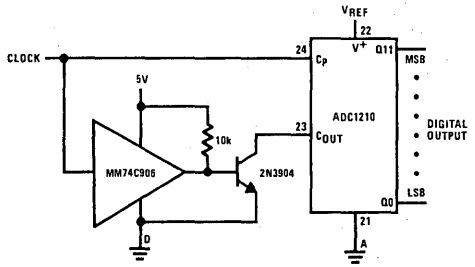


FIGURE 9. Conversion at 26 μs

A complementary phased clock is required. The positive phase is used to clock the converter SAR as is normally the case. The same signal is buffered and inverted by the transistor. The open collector is wire-ORed to the output of the comparator. During the first half of the clock cycle (50% duty cycle), the comparator output is clamped and disabled, though its internal operation is still in normal working order. The last half cycle of the clock unclamps the comparator output. Thus, the output is permitted to slew to the final logic state just before the decision is logged into the SAR. The MM74C906 buffer (or with two inverting buffers) provides adequate propogation delay such that the comparator output data is held long enough to resolve any internal logic set-up time requirements.

The 500 kHz clock implies that the absolute minimum amount of time for the comparator output is *unclamped* is 1 μs. Therefore, if the clock is not 50% duty cycle, this 1 μs requirement must be observed.

3.0 DEFINITION OF TERMS

Resolution: The Resolution of an A/D is an expression of the smallest change in input which will increment (or decrement) the output from one code to the next adjacent code. It is defined in number of bits, or 1 part in 2^n. The ADC1210 and ADC1211 have a resolution of 12 bits or 1 part in 4,096 (0.0244%).

Quantization Uncertainty: Quantization Uncertainty is a direct consequence of the resolution of the converter. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an inherent conversion error even for a perfect A/D. As an example, the transfer characteristic of a perfect 3-bit A/D is shown in *Figure 10.*

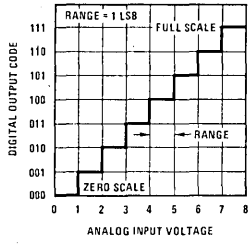


FIGURE 10. Quantization Uncertainty of a Perfect 3-Bit A/D

As can be seen, all input voltages between 0V and 1V are represented by an output code of 000. All input voltages between 1V and 2V are represented by an output code of 001, etc. If the midpoint of the range is assumed to be the nominal value (e.g., 0.5V), there is an Uncertainty of ±1/2 LSB. It is common practice to offset the converter 1/2 LSB in order to reduce the Uncertainty to ±1/2 LSB is shown in *Figure 11*, rather than +1, −0 shown in *Figure 10*. Quantization Uncertainty can only be reduced by increasing Resolution. It is expressed as ±1/2 LSB or as an error percentage of full scale (±0.0122% FS for the ADC1210).

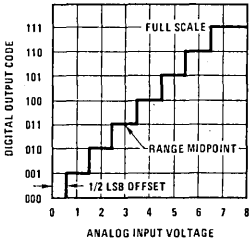


FIGURE 11. Transfer Characteristic Offset 1/2 LSB to Minimize Quantizing Uncertainty

Linearity Error: Linearity Error is the maximum deviation from a straight line passing through the end points of the A/D transfer characteristic. It is measured after calibrating Zero and Full Scale Error. The Linearity Error of the ADC1210 is guaranteed to be less than ±1/2 LSB or ±0.0122% of FS and ±0.0488% of FS for the AD1211. Linearity is a performance characteristic intrinsic to the device and cannot be externally adjusted.

Zero Scale Error (or Offset): Zero Scale Error is a measure of the difference between the output of an ideal and the actual A/D for zero input voltage. As shown in *Figure 12*, the effect of Zero Scale Error is to shift the transfer characteristic to the right or left along the abscissa. Any voltage more negative than the LSB transition gives an output code of 000. In practice, therefore, the voltage at which the 000 to 001 transition takes place is ascertained, this input voltage's departure from the ideal value is defined as the Zero Scale Error (Offset) and is expressed as a percentage of FS. In the example of *Figure 12*, the offset is 2 LSB's or 0.286% of FS.

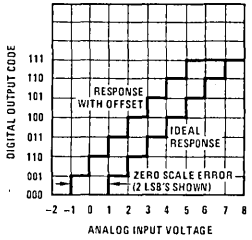


FIGURE 12. A/D Transfer Characteristic with Offset

The Zero Scale Error of the ADC1210, ADC1211 is caused primarily by offset voltage in the comparator. Because it is common practice to offset the A/D 1/2 LSB to minimize Quantization Error, the offsetting techniques described in the Applications Section may be used to null Zero Scale Error and accomplish the 1/2 LSB offset at the same time.

Full Scale Error (or Gain Error): Full Scale Error is a measure of the difference between the output of an ideal A/D converter and the actual A/D for an input voltage equal to full scale. As shown in *Figure 13*, the Full Scale Error effect is to rotate the transfer characteristic angularly about the origin. Any voltage more positive than the Full Scale transition gives an output code of 111. In practice, therefore, the voltage at which the transition from 111 to 110 occurs is ascertained. The input voltage's departure from the ideal value is defined as Full Scale Error and is expressed as a percentage of FS. In the example of *Figure 13*, Full Scale Error is 1 1/2 LSB's, or 0.214% of FS.

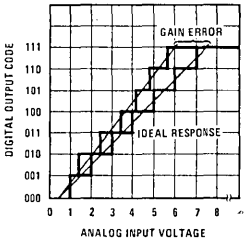


FIGURE 13. Full Scale (Gain Error)

Full Scale Error of the ADC1210, ADC1211 is due primarily to mismatch in the R-2R ladder equivalent output impedance and input resistors R25, R26, R27, and R28. The gain error may be adjusted to zero as outlined in section 2.5.

Monotonicity and Missing Codes: Monotonicity is a property of a D/A which requires an increasing or constant output voltage for an increasing digital input code. Monotonicity of a D/A converter does not, in itself, guarantee that an A/D built with that D/A will not have missing codes. However, the ADC1210 and ADC1211 are guaranteed to have no missing codes.

Conversion Time: The ADC1210, ADC1211 are successive approximation A/D converters requiring 13 clock intervals for a conversion to specified accuracy for the ADC1210 and 11 clocks for the ADC1211. There is a trade-off between accuracy and clock frequency due to settling time of the ladder and propagation delay through the comparator. By modifying the hysteresis network around the comparator, conversions with 10-bit accuracy can be made in 30 μs. Replace R_A, R_B and C_A in *Figure 5* with a 10 MΩ resistor between pin 23 (Comparator Output) and pin 17 (+ IN), and increase the clock rate to 366 kHz.

In order to prevent errors during conversion, the analog input voltage should not be allowed to change by more than $\pm$1/2 LSB. This places a maximum slew rate of 12.5 μV/μs on the analog input voltage. The usual solution to this restriction is to place a Sample and Hold in front of the A/D. For additional application information, refer to application note AN245.

DM2502, DM2503, DM2504 Successive Approximation Registers

General Description

The DM2502, DM2503 and DM2504 are 8-bit and 12-bit TTL registers designed for use in successive approximation A/D converters. These devices contain all the logic and control circuits necessary in combination with a D/A converter to perform successive approximation analog-to-digital conversions.

The DM2502 has 8 bits with serial capability and is not expandable.

The DM2503 has 8 bits and is expandable without serial capability.

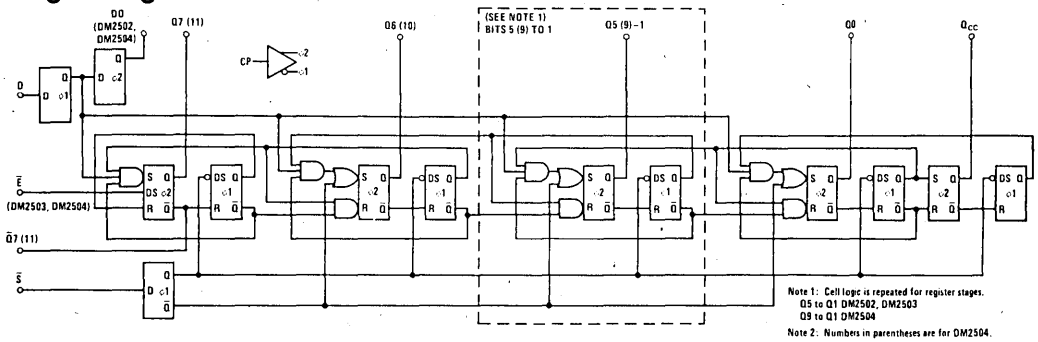
The DM2504 has 12 bits with serial capability and expandability.

All three devices are available in ceramic DIP, ceramic flatpak, and molded Epoxy-B DIPs. The DM2502, DM2503 and DM2504 operate over −55°C to +125°C; the DM2502C, DM2503C and DM2504C operate over 0°C to +70°C.

Features

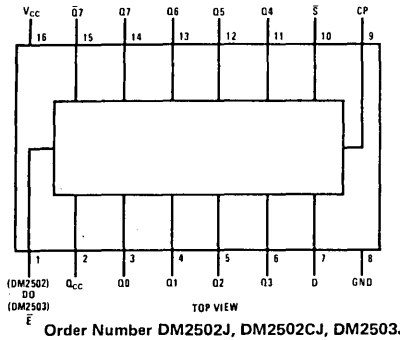
- Complete logic for successive approximation A/D converters
- 8-bit and 12-bit registers
- Capable of short cycle or expanded operation
- Continuous or start-stop operation
- Compatible with D/A converters using any logic code
- Active low or active high logic outputs
- Use as general purpose serial-to-parallel converter or ring counter

Logic Diagram



Connection Diagrams (Dual-In-Line and Flat Packages)

DM2502, DM2503

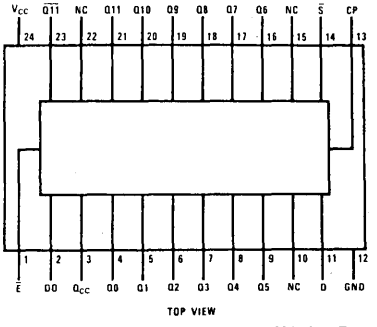


Order Number DM2502J, DM2502CJ, DM2503J, or DM2503CJ
See NS Package J16A

Order Number DM2502CN or DM2503CN
See NS Package N16A

Order Number DM2502W, DM2502CW, DM2503W, or DM2503CW
See NS Package W16A

DM2504



Order Number DM2504F or DM2504CF
See NS Package F24A

Order Number DM2504J or DM2504CJ
See NS Package J24A

Order Number DM2504CN
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DM2502C, DM2503C, DM2504C	4.75	5.25	V
DM2502, DM2503, DM2504	4.5	5.5	V
Temperature, T_A			
DM2502C, DM2503C, DM2504C	0	+70	°C
DM2502, DM2503, DM2504	−55	+125	°C

Electrical Characteristics (Notes 2 and 3) $V_{CC} = 5.0V$, $T_A = 25°C$, $C_L = 15pF$, unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage (V_{IH})	V_{CC} = Min	2.0			V
Logical "1" Input Current (I_{IH})	V_{CC} = Max				
CP Input	V_{IH} = 2.4V		6	40	μA
D, $\overline{E}$, $\overline{S}$ Inputs	V_{IH} = 2.4V		6	80	μA
All Inputs	V_{IH} = 5.5V			1.0	mA
Logical "0" Input Voltage (V_{IL})	V_{CC} = Min			0.8	V
Logical "0" Input Current (I_{IL})	V_{CC} = Max				
CP, $\overline{S}$ Inputs	V_{IL} = 0.4V		−1.0	−1.6	mA
D, $\overline{E}$ Inputs	V_{IL} = 0.4V		−1.0	−3.2	mA
Logical "1" Output Voltage (V_{OH})	V_{CC} = Min, I_{OH} = −0.48 mA	2.4	3.6		V
Output Short Circuit Current (Note 4) (I_{OS})	V_{CC} = Max; V_{OUT} = 0.0V; Output High; CP, D, $\overline{S}$, High; $\overline{E}$ Low	−10	−20	−45	mA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, I_{OL} = 9.6 mA		0.2	0.4	V
Supply Current (I_{CC})	V_{CC} = Max, All Outputs Low				
DM2502C			65	95	mA
DM2502			65	85	mA
DM2503C			60	90	mA
DM2503			60	80	mA
DM2504C			90	124	mA
DM2504			90	110	mA
Propagation Delay to a Logical "0" From CP to Any Output (t_{pd0})		10	18	28	ns
Propagation Delay to a Logical "0" From $\overline{E}$ to Q7 (Q11) Output (t_{pd0})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		16	24	ns
Propagation Delay to a Logical "1" From CP to Any Output (t_{pd1})		10	26	38	ns
Propagation Delay to a Logical "1" From $\overline{E}$ to Q7 (Q11) Output (t_{pd1})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		13	19	ns
Set-Up Time Data Input ($t_{s(D)}$)		−10	4	8	ns
Set-Up Time Start Input ($t_{s(\overline{S})}$)		0	9	16	ns
Minimum Low CP Width (t_{PWL})			30	42	ns
Minimum High CP Width (t_{PWH})			17	24	ns
Maximum Clock Frequency (f_{MAX})		15	21		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM2502, DM2503 and DM2504, and across the 0°C to +70°C range for the DM2502C, DM2503C and DM2504C. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Application Information

OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the DM2502 and DM2504 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7 (11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ signal must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7 (11) register bit and the Q6 (10) register bit is set to a low ready for the next clock cycle. On the next clock low-to-high transition data enters the Q6 (10) register bit and Q5 (9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The DM2502, DM2503 and DM2504 have a specially tailored two-phase clock generator to provide non-overlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

LOGIC CODES

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator 1/2 full range + 1/2 LSB and using the complement of the MSB ($\overline{Q7}$ or $\overline{Q11}$) with a binary D/A converter. Offset binary is used in the same manner but with the MSB (Q7 or Q11). BCD D/A converters can be used with the addition of illegal code suppression logic.

ACTIVE HIGH OR ACTIVE LOW LOGIC

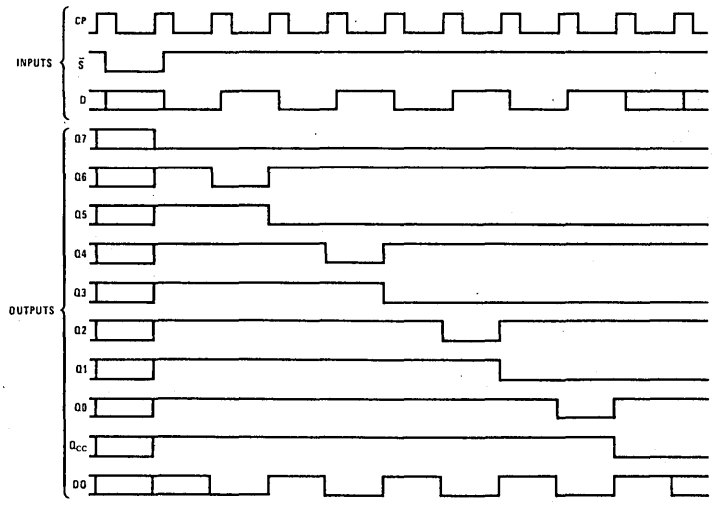
The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

EXPANDED OPERATION

An active low enable input, $\overline{E}$, on the DM2503 and DM2504 allows registers to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start signal resets the register, the $\overline{E}$ signal goes high, forcing the Q7 (11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

Timing Diagram

DM2502, DM2503



Application Information (Cont'd)

SHORT CYCLE

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather than the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

COMPARATOR BIAS

To minimize the digital error below ±1/2 LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased +1/2 LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased −1/2 LSB.

Definition of Terms

CP: The clock input of the register.

D: The serial data input of the register.

DO: The serial data out. (The D input delayed one bit).

$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7 (11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).

Q_i i = 7 (11) to 0: The outputs of the register.

Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.

Q7 (11): The true output of the MSB of the register.

$\overline{Q7}$ (11): The complement output of the MSB of the register.

$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7 (11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

Truth Table

DM2502, DM2503

TIME	INPUTS			OUTPUTS[1]									
t_n	D	$\overline{S}$	$\overline{E}$[2]	DO[3]	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

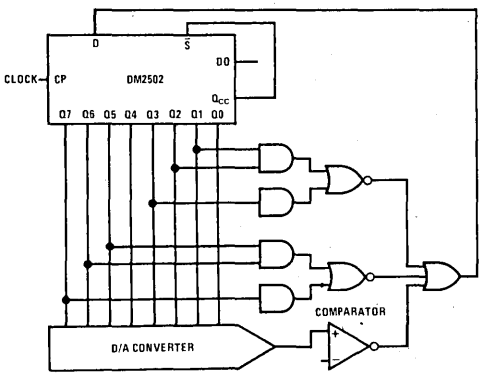
Note 1: Truth table for DM2504 is extended to include 12 outputs.

Note 2: Truth table for DM2502 does not include $\overline{E}$ column or last line in truth table shown.

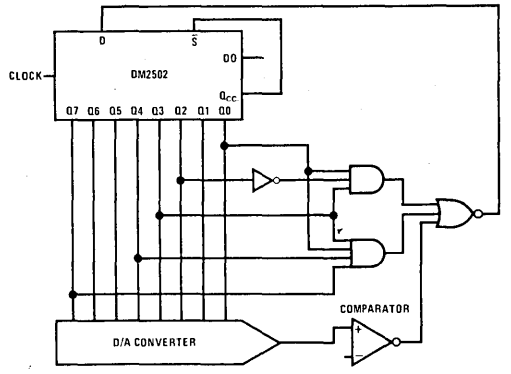
Note 3: Truth table for DM2503 does not include D0 column.

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
NC = No Change

Typical Applications



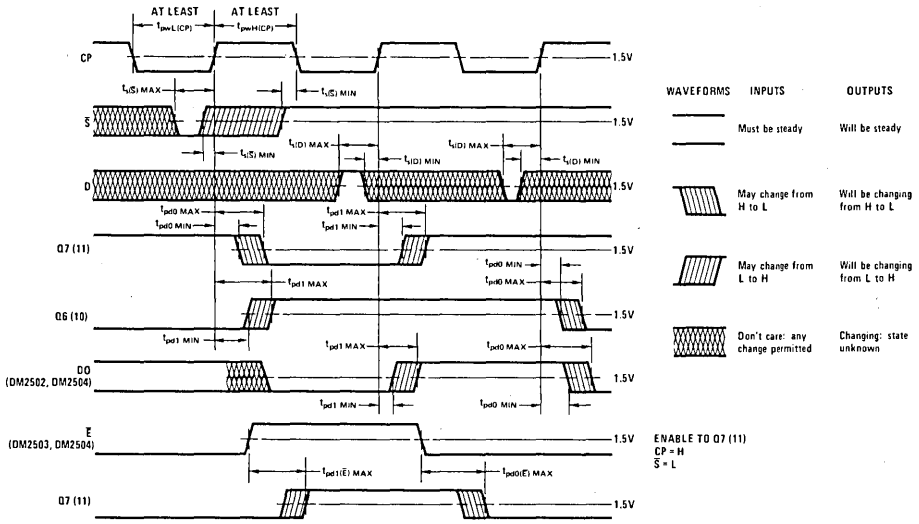
Active High



Active Low

BCD Illegal Code Suppression

Switching Time Waveforms



National Semiconductor

MM54C905/MM74C905 12-Bit Successive Approximation Register

General Description

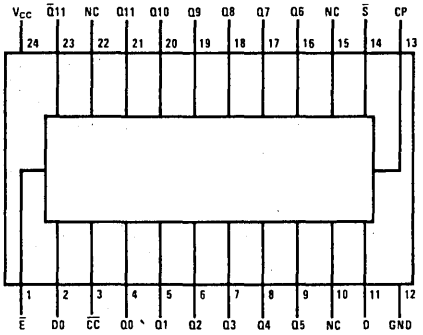
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

Connection Diagram

Dual-In-Line Package



Order Numbers
MM54C905D
MM74C905D
See Package D24A

Order Number
MM74C905N
See Package N24A

Truth Table

TIME	INPUTS			OUTPUTS												
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level L = Low level X = Don't care NC = No change

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C905	−55°C to +125°C
MM74C905	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA			0.5	V
	V_{CC} = 10V, I_O = 10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C905	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C905	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C905	V_{CC} = 4.5V			0.8	V
MM74C905	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C905	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C905	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C905	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C905	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA
Q11–Q0 Outputs	V_{CC} = 10V ±5%				
R_{SOURCE}	V_{OUT} = V_{CC} − 0.3V, T_A = 25°C	150		350	Ω
R_{SINK}	V_{CC} = 10V ±5%, V_{OUT} = 0.3V, T_A = 25°C	80		230	Ω

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time From Clock Input To Outputs (Q0–Q11) ($t_{pd(Q)}$)	$V_{CC} = 5.0V$		200	350	ns
	$V_{CC} = 10V$		80	150	ns
Propagation Delay Time From Clock Input To D_O ($t_{pd(D_O)}$)	$V_{CC} = 5.0V$		180	325	ns
	$V_{CC} = 10V$		70	125	ns
Propagation Delay Time From Register Enable ($\overline{E}$) To Output (Q11) ($t_{pd(\overline{E})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	150	ns
Propagation Delay Time From Clock To $\overline{CC}$ ($t_{pd(\overline{CC})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	0.50	ns
Data Input Set-Up Time (t_{DS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Start Input Set-Up Time (t_{SS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Minimum Clock Pulse Width (t_{PWL}, t_{PWH})	$V_{CC} = 5.0V$	250	125		ns
	$V_{CC} = 10V$	100	50		ns
Maximum Clock Rise and Fall Time (t_r, t_f)	$V_{CC} = 5.0V$			15	μs
	$V_{CC} = 10V$			5	μs
Maximum Clock Frequency (f_{MAX})	$V_{CC} = 5.0V$	2	4		MHz
	$V_{CC} = 10V$	5	10		MHz
Clock Input Capacitance (C_{CLK})	Clock Input (Note 2)		10		pF
Input Capacitance (C_{IN})	Any Other Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{PD})	(Note 3)		100		pF

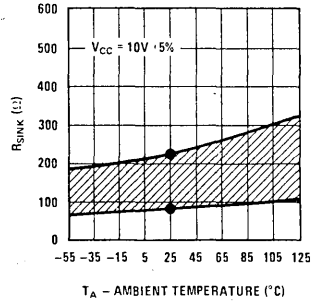
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

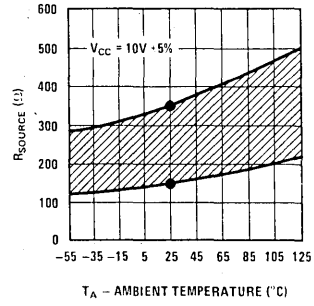
Typical Performance Characteristics

R_{SINK} vs Temperature



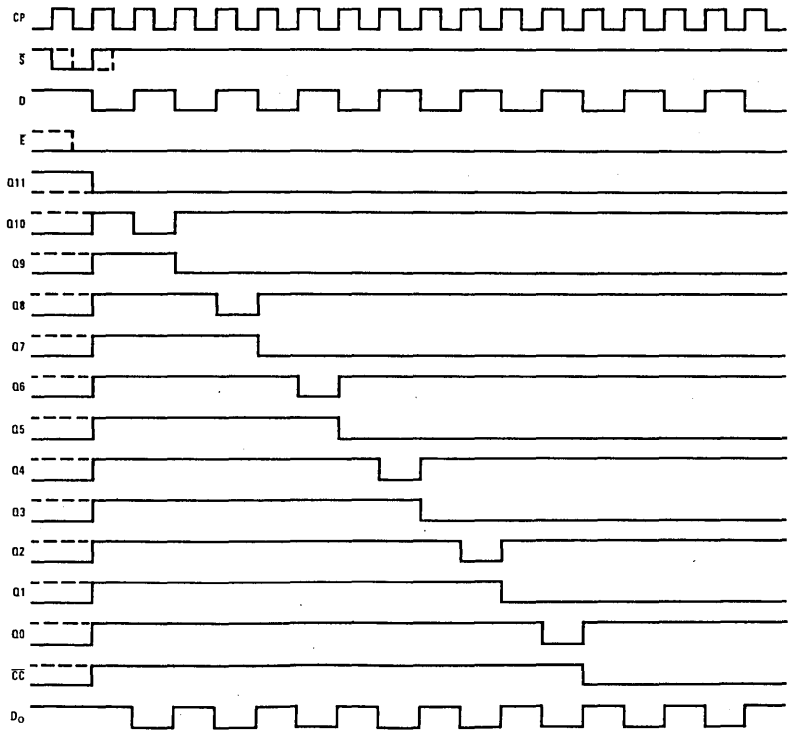
● These points are guaranteed by automatic testing.

R_{SOURCE} vs Temperature

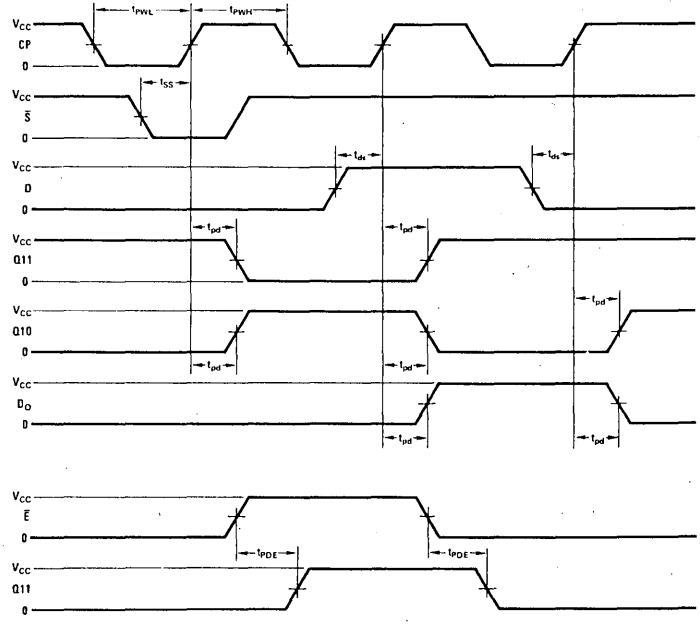


● These points are guaranteed by automatic testing.

Timing Diagram



Switching Time Waveforms



USER NOTES FOR A/D CONVERSION

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of ±1/2 LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased −1/2 LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range +1/2 LSB and using the complement of the MSB Q11 as the sign bit.

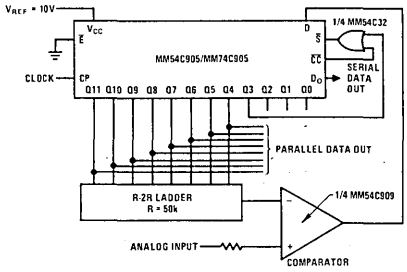
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

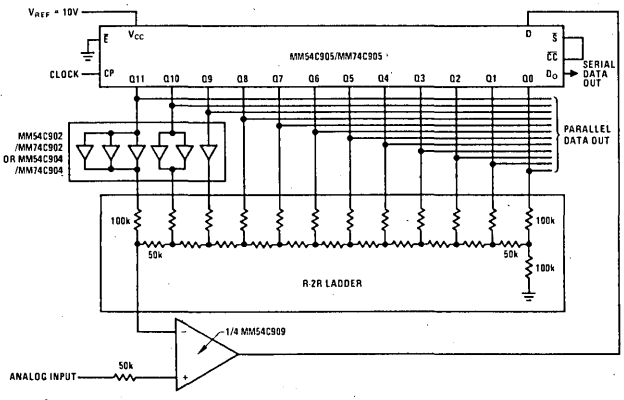
The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for V_{CC} = 10V or higher. In order to drive the 12-bit 50k/100k ladder network and have the ±1/2 LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as buffers, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

Typical Applications

12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode



12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly



Definition of Terms

CP: Register *clock* input.

$\overline{CC}$: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

$\overline{Q11}$: Complement of register MSB output.

Qi (i = 0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

Section 12

D/A Converters

Section 12. Digital-to-Analog Converters

Resolution (Bits)	NSC Part No.	Alternate Source Part No.	Non-Linearity @ 25°C (Max.) (%)	Internal Reference	Output Op Amp	Supplies (V)	Temp. Ranges Available (°C)	Comments	Page
12	DAC1200	—	±0.0122	•	•	+5, ±15	−25 to +85, −55 to +125		12-4
12	DAC1201	—	±0.0488	•	•	+5, ±15			12-4
12	DAC1242	—	±0.0244	•	•	+5, +12		4-20mA Current Sink	12-10
12	DAC1243	—	±0.0244	•	•	+5, +12		4-20mA Current Source	12-10
12	DAC1280	—	±0.0244	•	•	+5, ±15	0 to 70		12-12
12	DAC1280A	DAC80-CBI-V	±0.0122	•	•	±12 to ±15	0 to 70		12-12
12	DAC1285	DAC85-CBI-V	±0.0122	•	•	+5, ±15	−25 to +85, −55 to +125		12-20
12	DAC1285A	DAC85LD-CBI-V, DAC87-CBI-V	±0.0122	•	•	±12 to ±15	−25 to +85 −55 to +125		12-20

National Semiconductor

DAC1200, DAC1201 12-Bit Digital-to-Analog Converters

General Description

The DAC1200 series of D/A converters is a family of precision low-cost converter building blocks intended to fulfill a wide range of industrial and military D/A applications. These devices are complete functional blocks requiring only application of power for operation. The design combines a precision 12-bit weighted current source (12 current switches and 12-bit thin-film resistor network), a rapid-settling operational amplifier, and 10.24V buffered reference.

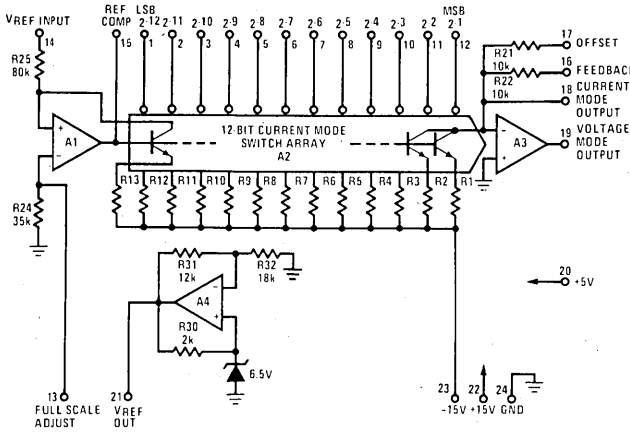
Input coding is complementary binary. In all instances, a logic "low" ($\leq$ 0.8V) turns a given bit ON, and a logic "high" ($\geq$ 2.0V) turns the bit OFF. Output format may be programmed for bipolar (±10V) or unipolar (0 to 10V) operation using internally supplied thin-film resistor pin strap options. Current mode operation is also available from 0 to 2 mA.

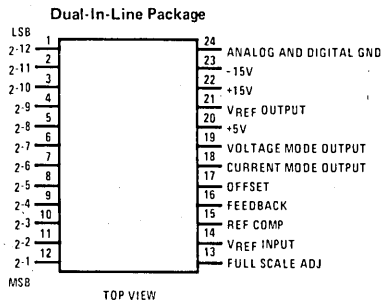
The entire series is available in hermetically sealed 24-lead DIP.

Features

- Circuit completely self-contained
- Both current and voltage-mode outputs
- Standard power supplies: ±15V and +5V
- Internal buffered reference: 10.24V
- 0 to 2 mA, ±10V or 0 to 10V output by strapping internal resistors; other scales by external resistors
- ±1/2 LSB linearity
- Fast settling time: 1.5 μs in current mode
  2.5 μs in voltage mode
- High slew rate: 15 V/μs
- TTL and CMOS compatible complementary binary input logic
- 12 bit linearity
- Standard 0.6" 24-pin DIP package

Block and Connection Diagrams





Order Number DAC1200HD, DAC1200HCD, DAC1201HD or DAC1201HCD
See NS Package D24G

Absolute Maximum Ratings

Supply Voltage (V^+ & V^-)	±18 V
Logic Supply Voltage (V_{CC})	+10 V
Logic Input Voltage	−0.7 V to +18 V
Reference Input Voltage	−0 V, +18 V
Power Dissipation	(see graphs)
Short Circuit Duration (pins 18, 19 & 21)	Continuous
Operating Temperature Range	
DAC1200HD, DAC1201HD	−55°C to +125°C
DAC1200HCD, DAC1201HCD	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec.)	300°C

DC Electrical Characteristics DAC1200,1201 Binary D/A (Notes 1, 2)

PARAMETER	CONDITIONS	DAC1200/1200C			DAC1201/1201C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		12			12			Bits
Linearity Error (Note 3)	$T_A = 25°C$			±0.0122			±0.0488	% FS
				±0.0244			±0.0976	% FS
Offset Voltage	$T_A = 25°C$		1	5		1	10	mV
				10			15	mV
Voltage Mode Full-Scale Error (Note 3)	$V_{REF} = 10.240V$		0.01	0.1		0.02	0.2	% FS
Voltage Mode Full-Scale Error	Pin 21 connected to Pin 14, $T_A = 25°C$		0.1	0.6		0.1	0.7	% FS
Monotonicity (Notes 3, 4)		Guaranteed over the temperature range						
Voltage Mode Power Supply Sensitivity	$\Delta V^+ = \pm 2V$, $T_A = 25°C$		0.002	0.02		0.002	0.02	% FS/V
	$\Delta V^- = \pm 2V$, $V_{REF} = 10.240V$		0.002	0.02		0.002	0.02	% FS/V
	$\Delta V_{CC} = \pm 1V$		0.002	0.02		0.002	0.02	% FS/V
Output Voltage Range	$R_L = 5k$	±10.5	±12		±10.5	±12		V
Voltage Mode Output Short Circuit Current Limit	$T_A = 25°C$		20	50		20	50	mA
Current Mode Voltage Compliance	(Note 5)	±2.5			±2.5			V
Current Mode Output Impedance			15			15		kΩ
Reference Voltage	$0mA \leq I_{REF} \leq 2mA$, $T_A = 25°C$	10.190	10.240	10.290	10.190	10.240	10.290	V
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8	V
Logic "1" Input Current (Bit OFF)	$V_{IN} = 2.5V$		1	10		1	10	μA
Logic "0" Input Current (Bit ON)	$V_{IN} = 0V$		-10	-100		-10	-100	μA
Power Supply Current I^+	$V^+ = 15.0V$		10	15		10	15	mA
Power Supply Current I^-	$V^- = -15.0V$, $T_A = 25°C$		25	30		25	30	mA
Power Supply Current I_{CC}	$V_{CC} = 5.0V$		20	25		20	25	mA

AC Electrical Characteristics DAC1200,1201

PARAMETER	CONDITIONS ($T_A = 25°C$)	MIN	TYP	MAX	UNITS
Voltage Mode ±1 LSB Settling Time (Note 5)	DAC1200, $V_\epsilon \leq 1.25$ mV		1.5	3.0	μs
	DAC1201, $V_\epsilon \leq 5.0$ mV		1	3.0	μs
Voltage Mode Full-Scale Change Settling Time (Note 5)	DAC1200, $V_\epsilon \leq 1.25$ mV		2.5	5.0	μs
	DAC1201, $V_\epsilon \leq 5.0$ mV		2.0	5.0	μs
Current Mode Full-Scale Settling Time	$R_L = 1k\Omega$, $C_L \leq 20pF$, $0 \leq \Delta I_{OUT} \leq 2mA$		1.5		μs
Voltage Mode Slew Rate	$-10V \leq \Delta V_{OUT} \leq +10V$		15		V/μs

Note 1: Unless otherwise noted, these specifications apply for $V^+ = 15.0V$, $V^- = -15.0V$, and $V_{CC} = 5.0V$ over the temperature range −55°C to +125°C for the DAC1200HD/1201HD and −25°C to +85°C for the DAC1200HCD/1201HCD.

Note 2: All typical values are for $T_A = 25°C$.

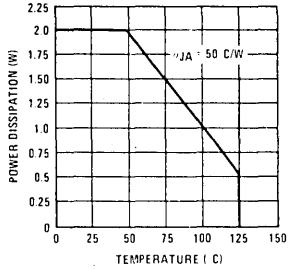
Note 3: Unless otherwise noted, this specification applies for $V_{REF} = 10.24V$, and over the temperature range −25°C to +85°C. Testing conditions include adjustment of offset to 0V and full-scale to 10.2375V.

Note 4: The DAC1200 is tested for monotonicity by stimulating all bits; the DAC1201 is tested for monotonicity by stimulating only the 10 MSBs and holding the 2 LSBs at 2.0V (i.e., 2 LSBs are OFF).

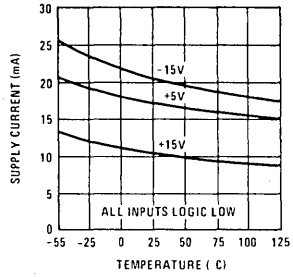
Note 5: Not tested — guaranteed by design.

Typical Performance Characteristics

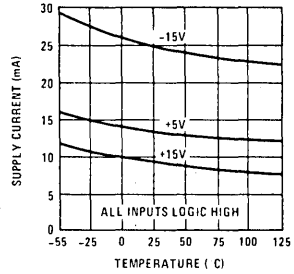
Maximum Power Dissipation

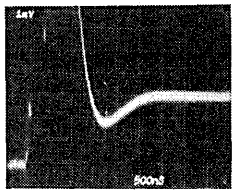


Supply Current vs Temperature

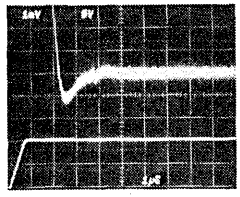


Supply Current vs Temperature

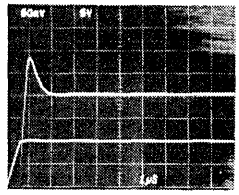




1 LSB Transition
1011 . . . 1 → 1100 . . . 0
V_O = 0, 10V
C_F = 30pF
T_A = 25°C



10V Full Scale Settling Time



10V Full Scale Pulse Response

Applications Information

1. Introduction

The DAC1200 series D/A converters are designed to minimize adjustments and user-supplied external components. For example, included in the package are a buffered reference, offset nulled output amplifier, and application resistors as well as the basic 12-bit current mode D/A.

However, the DAC1200 series is a sophisticated building block. **Its principles of operation and the following applications information should be read before applying power to the device.**

The user is referred to National Semiconductor Application Notes AN-156 and AN-157 for additional information.

2. Power Supply Selection & Decoupling

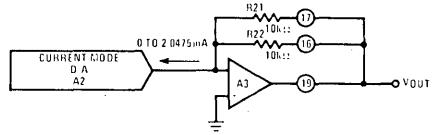
Selection of power supplies is important in applications requiring 0.01% accuracy. The ±15V supplies should be well regulated (±15V ± 0.1%) with less than 0.5mVrms of output noise and hum.

To realize the full speed capability of the device, all three power supply leads should be bypassed with 1μF tantalum electrolytic capacitors in shunt with 0.01μF ceramic disc capacitors no farther than ½ inch from the device package.

3. Unipolar and Bipolar Operation

The DAC1200 series D/A's may be configured for either unipolar or bipolar operation using resistors provided with the device. Figure 1A illustrates the proper connection for unipolar operation.

Bipolar operation is accomplished by offsetting the output amplifier A3 as shown in Figure 2A.



$$^{*}V_{OUT} = (I_{ZERO} \text{ to } I_{FULLSCALE})\left(\frac{R21 \cdot R22}{R21 + R22}\right)$$

= (0mA to 2.0475mA)(5kΩ)

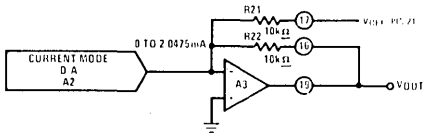
= 0V to +10.2375V

*Values shown are for V_{REF} = 10.240V.

1 LSB Voltage Step = $\frac{10.240V}{4096}$ = 2.5mV.

1 LSB Current Step = $\frac{2.5mV}{5.0k\Omega}$ = 0.5μA

FIGURE 1A. DAC1200/DAC1201 Unipolar Operation



$$*V_{OUT} = (0 \text{ to } 2.0475mA)R22 - \frac{V_{REF}}{R22} R21$$

$$= (0 \text{ to } 2.0475mA)R22 - V_{REF},\ R21 \equiv R22$$

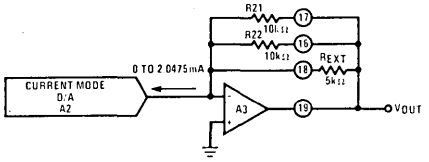
$$= -10.240 \text{ to } +10.235V$$

*Values shown are for $V_{REF} = 10.240V$

1 LSB = 5mV.

FIGURE 2A. DAC1200/DAC1201 Bipolar Operation

External resistors may be used to achieve alternate zero and full-scale voltages. It is advantageous to utilize R21 and R22 even in these applications since they are closely matched in TCR and temperature to the internal array. Figure 3 illustrates the recommended circuit for zero to 5V operation. R_{EXT} should be of metal film or wire-wound construction with a TCR of less than 10ppm/°C.



$$R_{TOTAL} = (R21) \| (R22) \| (R_{EXT}) = \frac{V_{FULLSCALE}}{2.0475mA} = 2.5k\Omega.$$

FIGURE 3. DAC1200 0 to 5.120V Operation

4. Offset and Full-Scale Adjust

If higher precision is required in the zero and full-scale, external adjustments may be made. The circuit of figure 4 illustrates the recommended circuit to adjust offset and full-scale of the DAC1200 series. The circuit will work equally well for unipolar or bipolar operation.

In bipolar operation, the offset is adjusted at minus full-scale; in the unipolar case at zero scale.

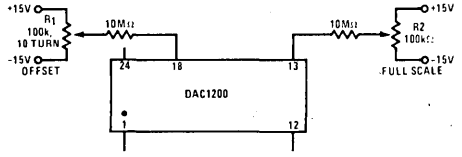


FIGURE 4. Offset & Full-Scale Adjust

For the values shown in figure 4, R1 will allow a ±7mV offset adjustment for the unipolar case and ±15mV for the bipolar case. R2 will allow a ±50mV adjustment of full scale.

5. Current Mode Operation

Access to the summing junction of A3 affords current mode operation either with a resistive load or to drive a fast-settling external operational amplifier. The loop around A3 should not be closed in current mode operation. There is a ±2.5V maximum compliance voltage at A2's output (pin 18) which restricts the maximum size of the load resistor; i.e., $R_L \times I_{FULLSCALE} \leq 2.5V$.

Note: $I_{FULLSCALE} \approx 2$ mA.

6. Settling Time & Glitch Minimization

The settling time of the DAC1200 series and the glitch which occurs between major input code changes may be improved by placing a 10 to 30pF capacitor between pins 18 (current-mode output) and 19 (voltage mode output). The capacitor is used to cancel output capacitance of the current mode D/A and stray capacitance at pin 18.

7. Current Output Boosting

The DAC1200 series may be operated as a "power D/A" by including a current buffer such as the LH0002 or LH0063 in the loop with A3 as shown in figure 5.

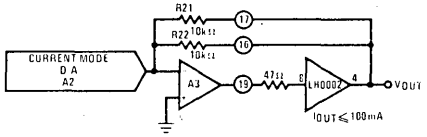


FIGURE 5. Current Boosted Output

8. Logic Input Coding

The sense of the logic inputs to the DAC1200 series is complementary; i.e., a given bit is turned ON by an active "low" input. Table I summarizes input status for the unipolar and bipolar complementary binary and BCD codes.

Other input codes may also be used. For example, the twos complement code, which is used extensively in computer and microprocessor applications, may be converted to the DAC1200 complementary bipolar format by inverting all bits except the MSB. The inversion may be accomplished in the microprocessor by software control, or by hardware using standard hex-inverters.

9. Reference Voltage

External reference voltages may be used with the DAC1200 series. Voltages other than 10.240 or 10.000V in the range of +5.0V to 11V will work satisfactorily for voltage mode operation. Full-scale voltage is always $V_{REF} - 1$ LSB where 1 LSB = $V_{REF}/4096$. Full-scale current may be predicted by:

$$I_{FULLSCALE} = (V_{REF})(0.19995117)mA$$

CODE TYPE	(Note 8) INPUT CODE MSB LSB	OUTPUT STATE	OUTPUT VOLTAGE V_{REF} = 10.240V	OUTPUT CURRENT
Unipolar Complementary Binary	0000 0000 0000	Full-Scale	+10.2375V	2.0475mA
	1111 1111 1110	1 LSB ON	+2.500mV	0.500μA
	1111 1111 1111	Zero Scale	Zero	Zero
Bipolar Complementary Binary	0000 0000 0000	Full-Scale	+10.235V	+1.0235mA
	0111 1111 1111	Half Full-Scale	-0.000V	0.000mA
	1111 1111 1110	1 LSB ON	-10.235V	-1.0235mA
	1111 1111 1111	Zero Scale	-10.240V	-1.0240mA

Note 8: Logic input sense is such that an active low ($V_{IN} \leq 0.8V$) turns a given bit ON and is represented as a logic "0" in the table.

Definition of Terms

Resolution

Resolution is defined as the reciprocal of the number of discrete steps in the D/A output (as designed). It is directly related to the number of switches or bits within the D/A. For example, the DAC1200 has 2^{12} or 4096 steps. Resolution may therefore be expressed variously as 12 bits, as 1 part in 2^{12}, as 1 part in 4096, or as a percentage (1/4096 x 100 = 0.0244%).

Linearity Error

Linearity error is the maximum deviation from a straight line passing through the endpoints of the D/A transfer characteristic. It is measured after calibrating for zero and full-scale. The linearity error of the DAC1200 series is guaranteed to be less than ±½ LSB or 0.0122% of F.S. for the DAC1200/1200C and ±0.0488% of F.S. for the DAC1201/DAC1201C. Linearity error is a design parameter intrinsic to the device and cannot be externally adjusted.

Offset Voltage

Offset voltage is an output voltage other than zero volts for unipolar operation (and other than minus full-scale for bipolar operation) with all bits turned OFF. In the DAC1200 series this error resides primarily in the output amplifier, A3. Offset voltage is adjustable to zero as discussed in the applications section.

Power Supply Sensitivity

Power supply sensitivity is a measure of the effect of power supply changes on the D/A full-scale output.

Settling Time

Two settling time parameters are specified for the DAC1200 series. Full-scale settling time requires a zero to full-scale or full-scale to zero output change. One LSB settling time requires one LSB output change. In both instances, settling time is the time required from a code transition until the D/A output reaches within ±½ LSB of final output value.

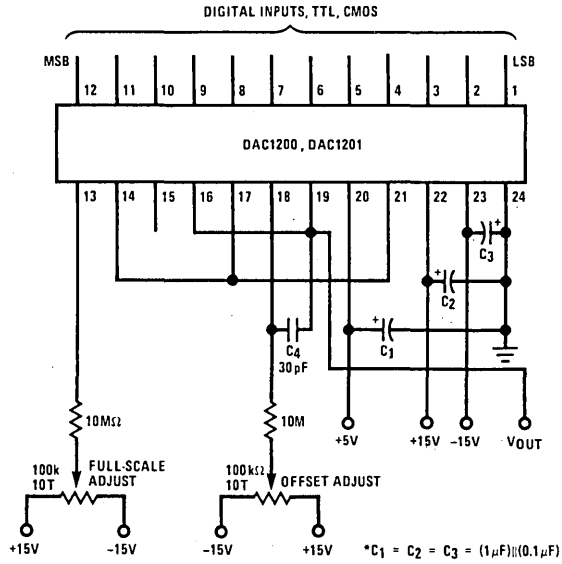
Monotonicity

Monotonicity is a characteristic of the D/A which requires a non-negative output step for an increasing input digital code. Monotonicity, therefore, demands no back steps or changes in sign of the slope of the D/A transfer characteristic.

Full-Scale Error

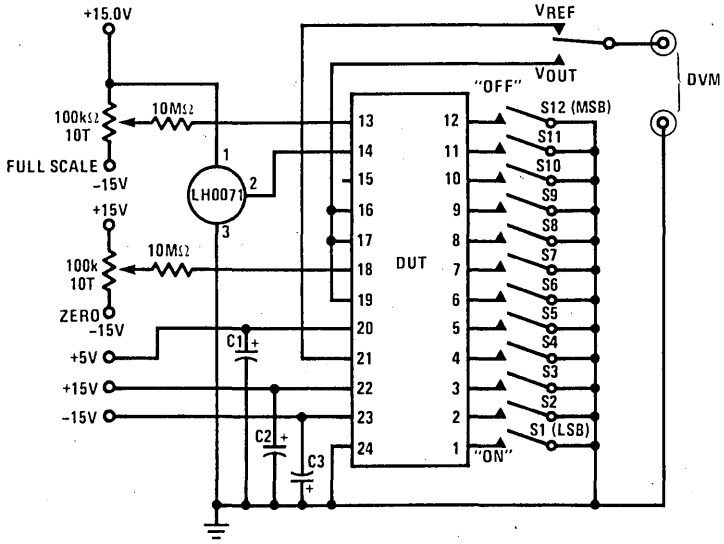
Full-scale error is a measure of the output error between an ideal D/A and the actual device output. Ideally, for the DAC1200 full-scale is V_{REF} – 1 LSB. For V_{REF} = 10.240V and unipolar operation, $V_{FULLSCALE}$ = 10.240V – 2.5mV = 10.2375V. Departures from this value include internal gain, scaling, and reference errors. Full-scale error is adjustable to zero as discussed in the **Applications** section.

Typical Application



20 Volt Full-Scale Complementary D/A

DC Test Circuit



C1 = C2 = C3 = 4.7μF (solid tantalum) in parallel with a 0.01μF ceramic disc

Ordering Information

PART NUMBER	PACKAGE	25°C LINEARITY ERROR	OPERATING TEMPERATURE RANGE
DAC1200HD	Ceramic DIP	0.01%	−55°C to +125°C
DAC1201HD	Ceramic DIP	0.05%	−55°C to +125°C
DAC1200HCD	Ceramic DIP	0.01%	−25°C to +85°C
DAC1201HCD	Ceramic DIP	0.05%	−25°C to +85°C

National Semiconductor

PRELIMINARY

DAC1242/DAC1243 Process Control DACs

General Description

The DAC1242/1243 are 12-bit digital-to-analog converters with 4-20mA current loop output. The DAC1242 is a current-sinking device, while the DAC1243 provides true current sourcing into a ground referenced load. The digital input registers are similar to an INS8255, allowing direct TTL interfacing to a variety of 8-bit microprocessors (8080, 8085, 8048, 8070, 8073, NSC800, Z80, et al). Interfacing to other microprocessor families or larger computers requires only 1 or 2 TTL packages. The device occupies 4 contiguous bytes of I/O or address space.

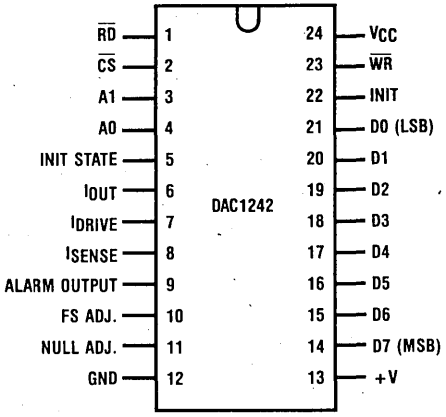
The converters produce a 4-20mA output current proportional to the digital input word with 12-bit resolution, guaranteed monotonicity, and <½LSB non- linearity; a 10-bit guaranteed part is also available. Null and span are internally calibrated to allow use of an external 100Ω, 1% current-sensing resistor with guaranteed null <4mA and full scale >20mA. Null and full-scale may be externally trimmed by the user.

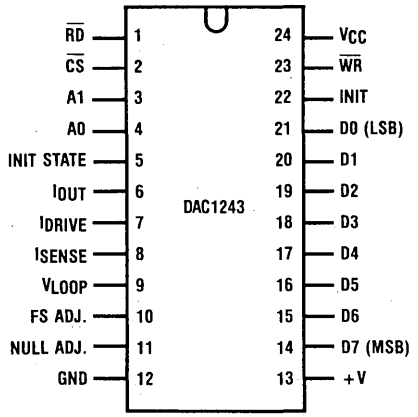
The devices are fully self-contained except for one external current sense resistor (some applications will utilize an external transistor for improved power dissipation). The package is a standard 24-pin ceramic DIP.

Features

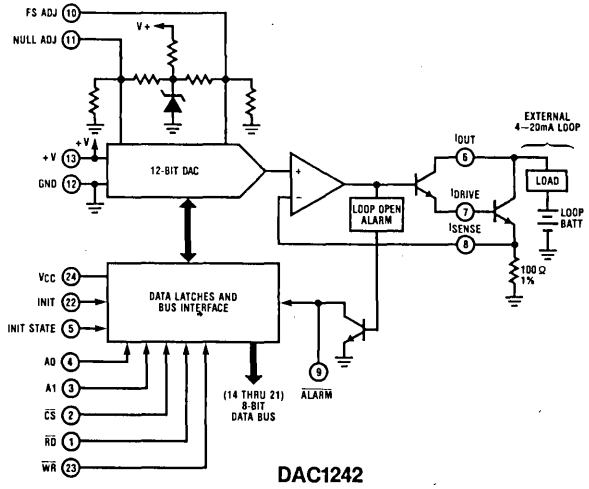
- 4-20mA current-loop output
- 12-bit resolution
- Monotonicity guaranteed
- Open loop alarm
- Data readback capability
- Initialize to zero or full-scale
- Internal reference
- Simple microprocessor interface
- Internal calibration
- No negative supply needed
- Standard 24-pin DIP
- Current sinking output (DAC1242)
- 12 to 60V loop supply (DAC1242)
- Open loop alarm available at pin (DAC1242)
- Simple 1-5V voltage output (DAC1243)
- Current sourcing output (DAC1243)
- 12 to 44V loop supply (DAC1243)

Connection Diagrams—Top Views

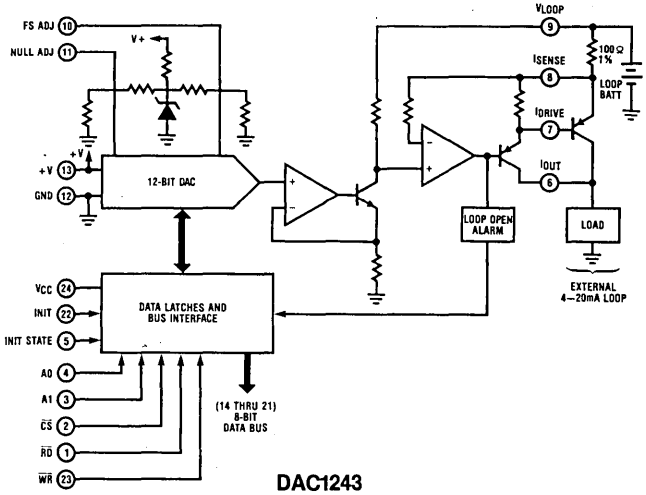




Equivalent Circuits



DAC1242



DAC1243

Command/Data Information

							DATA*							
							MSB							LSB
	INIT	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Initialize	1	X	X	X	X	X	X	X	X	X	X	X	X	X
Write Control Word	0	0	1	0	1	1	1	0	0	0	1	0	0	1
Write Low Data Byte	0	0	1	0	0	0	D	D	D	D	X	X	X	X
Write High Data Byte	0	0	1	0	0	1	D	D	D	D	D	D	D	D
Read Low Data Byte	0	0	0	1	0	0	F	F	F	F	X	X	X	X
Read High Data Byte	0	0	0	1	0	1	F	F	F	F	F	F	F	F
Read Loop-Open Alarm	0	0	0	1	1	0	F	X	X	X	X	X	X	X
Chip De-Select	0	1	X	X	X	X	X	X	X	X	X	X	X	X
	0	X	1	1	X	X	X	X	X	X	X	X	X	X

*Positive Logic, e.g., 0 = Low, 1 = High; X = Don't Care; D = Data to DAC; F = Data from DAC

National Semiconductor

DAC1280A, DAC1280 12-Bit Digital-to-Analog Converters

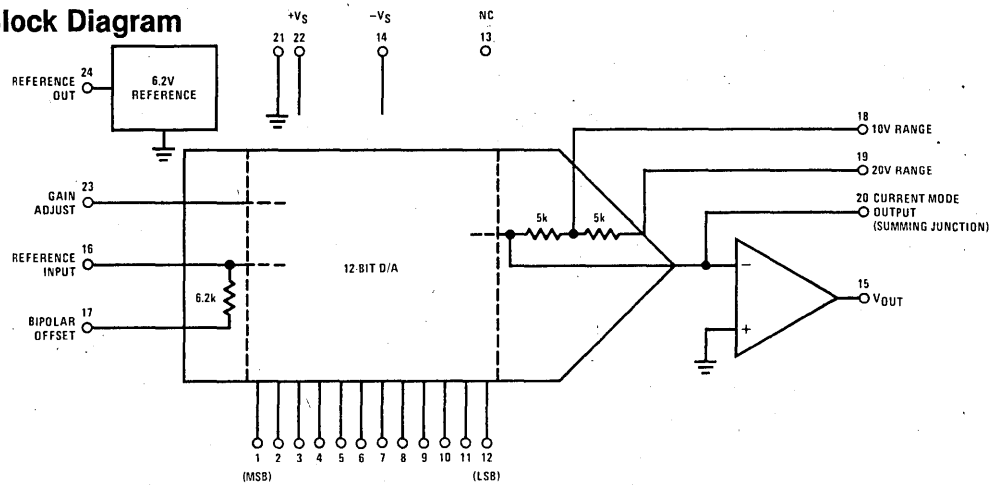
General Description

The DAC1280 series is a family of precision, low cost, fully self-contained digital-to-analog converters. The devices include 12 precision current switches, a 12-bit thin film resistor network, output amplifier, buffered internal reference, and several precision resistors, which allow the user to tailor his system needs to accommodate a variety of bipolar and unipolar output voltage and current ranges. Logic inputs are TTL, DTL and CMOS compatible, and are complementary binary (CBI) format. In all instances, a logic low ($\leq$0.8V) turns a given bit ON, and a logic high ($\geq$2V) turns a given bit OFF. Internally supplied resistor options provide low drift bipolar output voltage ranges of $\pm$2.5V, $\pm$5V, $\pm$10V, and unipolar ranges of 0V to 5V or 0V to 10V. Current mode output is 0 mA to 2 mA.

Features

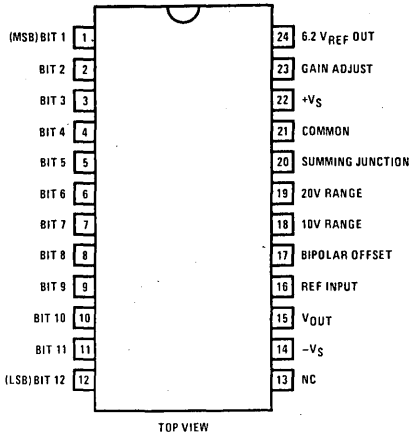
- Completely self-contained with internal reference and output amplifier
- High reliability exact replacement for DAC80-CBI-V or DAC80Z-CBI-V
- $\pm$1/2 LSB linearity max over 0°C to 70°C temperature range for DAC1280A
- $\pm$2.5V, $\pm$5V, $\pm$10V, 0V to 5V, 0V to 10V voltage outputs
- 0 mA to 2 mA current output
- Fast settling time: 300 ns current mode; 2.5 μs voltage mode
- Standard 24-pin IC package
- Low cost
- TTL CMOS compatible binary input logic over temperature

Block Diagram



Connection Diagram

Dual-In-Line Package



Order Number DAC 1280ADC
See NS Package D24G

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	± 18V	Short-Circuit Duration (Pins 15, 20 and 24)	Continuous
Current Output (Pin 20) Voltage Compliance	± 10V	Operating Temperature Range	0°C to +70°C
Logic Input Voltage	−0.7V, 10V	Storage Temperature Range	−65°C to +150°C
Reference Input Voltage (V_{REF})	0V, 18V	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$T_A = 0°C$ to 70°C, $V_S = \pm 11.4V$ to $\pm 15.75V$ for DAC1280A, $V_S = \pm 15V$ for DAC1280 unless otherwise noted.

Parameter	Conditions	DAC1280A			DAC1280			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
CONVERTER CHARACTERISTICS								
Resolution		12			12			Bits
Linearity Error	$T_A = 25°C$		± 1/4	± 1/2		± 1/4	± 1	LSB
				± 1/2			± 2	
Differential Non-Linearity			± 1/2	± 3/4		± 1/2		
Monotonicity		12			11	12		Bits
Full-Scale (Gain) Error	$T_A = 25°C$ (Note 2)		± 0.1	± 0.3		± 0.1		% FSR (Note 3)
Zero-Scale (Offset) Error	$T_A = 25°C$ (Note 2)		± 0.02	± 0.15		± 0.02		
Full-Scale (Gain) Tempco	Internal Reference		± 15	± 30		± 15		ppm/°C
	External Constant Reference		± 5	± 7		± 5		
Zero-Scale (Offset) Tempco	Unipolar		± 1	± 3		± 1		ppm FSR/°C
	Bipolar		± 3	± 10		± 3		
Total Bipolar Tempco (Note 4)	Includes Gain, Offset, and Linearity		± 10	± 20		± 10		
Total Error (Note 5)	Unipolar		± 0.08	± 0.15		± 0.08		% FSR
	Bipolar		± 0.06	± 0.10		± 0.06		
Output Voltage Range	Using Internally Supplied Resistors (Note 6)	± 2.5V, ± 5V, ± 10V, 0V to 5V, 0V to 10V						V
Output Voltage Swing	$R_L \geq 5$ kΩ, Pin 15	± 10			± 10			
Output Short Circuit Current	Pin 15	± 5	± 25	± 50	± 5	± 25	± 50	mA
Output Resistance	Pin 15, Closed Loop		0.05			0.05		Ω
Current Mode Output Range	Unipolar, Pin 20		0 to −2			0 to −2		mA
	Bipolar, Pin 20		± 1.0			± 1.0		
Current Mode Compliance				± 2.5			± 2.5	V
Current Mode Output Impedance	Unipolar		2			2		kΩ
	Bipolar		1.5			1.5		
REFERENCE CHARACTERISTICS								
Reference Voltage	$I_{REF} \leq 2$ mA, $T_A = 25°C$	6.07	6.2	6.33		6.2		V
Tempco of Drift			± 10	± 20		± 10		ppm/°C
External Use Current				2.5			2.5	mA
Output Resistance			0.05	1.0		0.05	1.0	Ω

Electrical Characteristics (Continued)

$T_A = 0°C$ to $70°C$, $V_S = \pm 11.4V$ to $\pm 15.75V$ for DAC1280A, $V_S = \pm 15V$ for DAC1280 unless otherwise noted.

Parameter	Conditions	DAC1280A			DAC1280			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
DIGITAL AND DC CHARACTERISTICS								
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8	V
Logic "1" Input Current	$V_{IN} = 2.5V$		0.05	1		0.05	1	μA
Logic "0" Input Current	$V_{IN} = 0V$			−100			−100	μA
Power Supply Current	I^+, $T_A = 25°C$		10	18		10		mA
	I^-, $T_A = 25°C$		25	30		25		mA
Power Supply Sensitivity			0.001	0.002		0.001		%FSR/%V
AC CHARACTERISTICS								
Voltage Mode Settling Time	1 LSB Change		400			400		ns
	FSR Change 10V		2.5			2.5		μs
	FSR Change 20V		4			4		μs
Voltage Mode Slew Rate	$T_A = 25°C$	10	15			15		V/μs
Current Mode Settling Time	10Ω to 100Ω Load		300			300		ns

Note 1: All typical values are for $T_A = 25°C$.

Note 2: Externally adjustable to zero.

Note 3: FSR means "full-scale range" and is 20V for ± 10V range, 10V for ±5V, etc.

Note 4: See paragraph 2.0 for definition.

Note 5: With gain and offset errors adjusted to zero at 25°C

Note 6: $\pm V_S$ must have absolute value 2V greater than V_{OUT}. Output voltage ranges −10V to +10V and 0V to +10V are not recommended with V_S less than 12V.

1.0 Definition of Terms

1.1 Accuracy

Accuracy of a D/A converter is the difference between the actual analog output that is measured when a given digital code is applied and the analog output that is expected with that code applied to the converter. Accuracy errors can be specified by the three parameters of gain or full-scale error, zero-scale or offset error, and linearity error.

1.2 Linearity Error

Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

1.3 Differential Linearity Error and Monotonicity

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ± 1/2 LSB means that the output voltage step sizes can range from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next. Monotonicity is guaranteed in the DAC1280A and DAC1280 to ensure that the analog output will not decrease with increasing input digital codes.

1.4 Gain Tempco

Gain tempco is a measure of the change in the full-scale range output over temperature expressed in parts per million per °C (ppm/°C).

1.5 Offset Tempco

Offset tempco is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, 25°C and 70°C. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This offset change is expressed in parts per million of full-scale range per °C (ppm of FSR/°C).

1.6 Settling Time

Settling time for each DAC1280A or DAC1280 is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input *(Figures 1 and 2).*

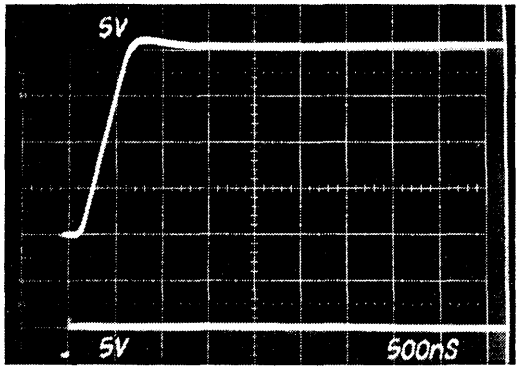


FIGURE 1. Voltage Mode Settling Time-FSR Change

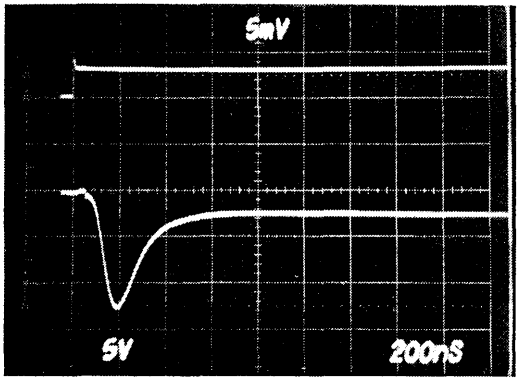


FIGURE 2. Voltage Mode Settling Time-1 LSB Change

Voltage Output. Three settling times are specified to ±0.01% of full-scale range (FSR); two for maximum full-scale range changes of 20V, 10V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output. Settling time is specified to ±0.01% of FSR. This is given with a range of resistive loads: 10Ω to 100Ω.

1.7 Compliance

Compliance voltage is the maximum voltage swing allowed on the current output pin (pin 20). Note that the absolute current offset error with any DAC will be increased by an amount given by V_{OUT}/R_{OUT}. In many situations this will be a significant error term if the voltage on the current output pin is allowed to exceed a few millivolts.

1.8 Power Supply Sensitivity

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

1.9 Reference Supply

The DAC1280A and DAC1280 are supplied with an internal 6.2V reference voltage supply. This voltage (pin 24) is accurate to ±2% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5 mA. All gain adjustments should be made under constant load conditions.

2.0 Analyzing Device Accuracy Over the Temperature Range

For the purposes of temperature drift analysis, the major device components are shown in *Figure 3.* The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient, which is specified as ±20 ppm/°C maximum for the DAC1280A. The input reference current to the DAC, I_{REF}, is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC}, which is a function of the digital input code, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain TC. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

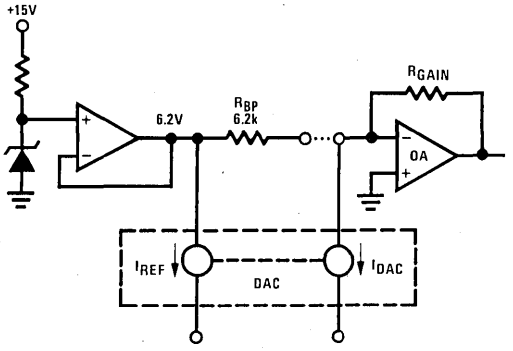


FIGURE 3. Bipolar Configuration

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full-scale. A specification for total error over temperature assumes that both the zero and full-scale points have been trimmed for zero error at 25°C. Total error is normally expressed as a percentage of the full-scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

2.1 Monotonicity and Linearity

The initial linearity error and the differential linearity error guarantee monotonic performance over the range of 0°C to 70°C. It can therefore be assumed that linearity errors are insignificant in computation of total temperature errors.

2.2 Unipolar Errors

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift, which comes from leakage currents and drift in the output amplifier, causes a linear shift in the transfer curve as shown in *Figure 4*. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in R_{GAIN} relative to the DAC resistors.

2.3 Bipolar Range Errors

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to the summing node of the output amplifier (see *Figure 3*) to generate a current which exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in *Figure 6*. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift. Gain drift in the DAC also contributes to bipolar offset drift, as well as full-scale drift. In the bipolar ranges, full-scale is defined as the total range from $-V_{FS}$ to $+V_{FS}$.

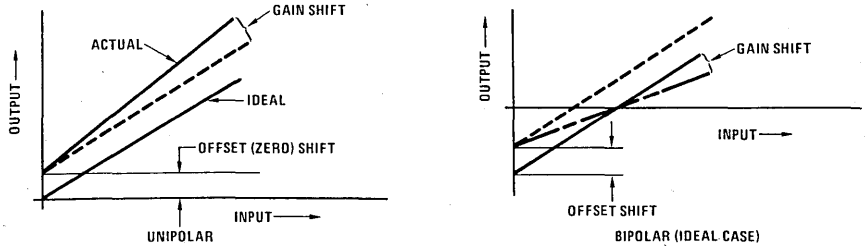


FIGURE 4. Unipolar and Bipolar Drifts

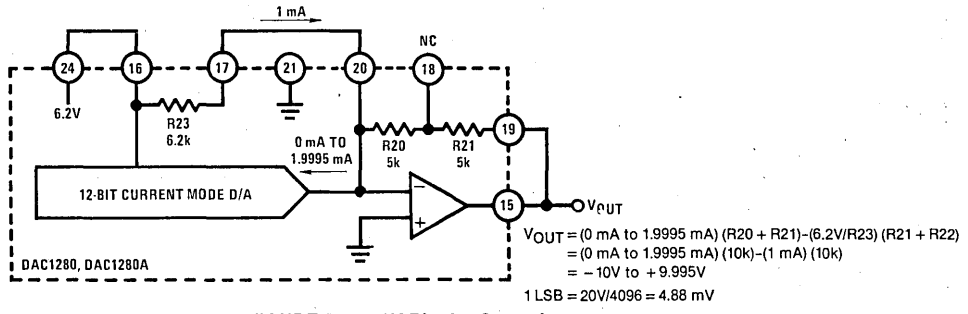


FIGURE 5. ±10V Bipolar Operation

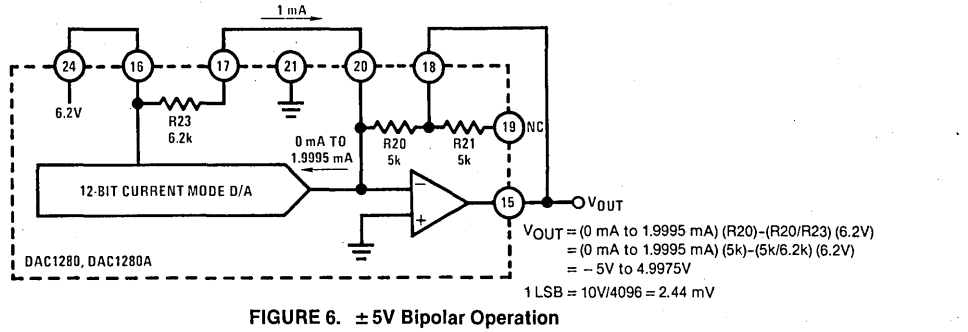


FIGURE 6. ±5V Bipolar Operation

3.0 Applications and Functional Description

3.1 Voltage Mode Operation

The DAC1280A and DAC1280 D/As provide internal scaling resistors which permit a wide range of bipolar and unipolar output configurations. Bipolar output formats of ±2.5V, ±5V, ±10V and unipolar formats of 0V to 5V and 0V to 10V are possible using resistor strap options included within the device. Table I and *Figures 5, 6 and 7* summarize the proper pin connections required for these formats.

3.2 Current Mode Operation

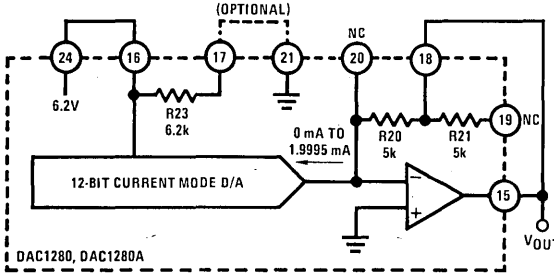
Current mode applications which make use of an external op amp, comparator, or a resistive load are possible with the DAC1280 series using pin 20. When an external op amp is used, the internal scaling resistors should be utilized to minimize full-scale drift. Configurations shown in Table I apply directly. *Figure 8* shows one application using an external fast operational amplifier.

Current mode operation into a resistive load or open circuit must account for the DACs nominal output resistance of 2k at pin 20. With this in mind, the output will swing 0V to −4V open circuit and about −1.5V to +1.5V with the bipolar offset resistor connected. An external load resistor may be used as part of the load, but there will be an error due to temperature coefficients mistracking.

TABLE I. Output Voltage/Current Ranges for DAC1280 Series

Output Voltage Range	Digital Input Code	Connect Pin 15 to	Connect Pin 16 to	Connect Pin 17 to	Connect Pin 19 to
±10V	Complementary Offset Binary	19	24	20	15
±5V	Complementary Offset Binary	18	24	20	NC
±2.5V	Complementary Offset Binary	18	24	20	20
10V	Complementary Binary	18	24	21*	NC
5V	Complementary Binary	18	24	21*	20
±1 mA	Complementary Offset Binary	NC	24	20	NC
−2 mA	Complementary Binary	NC	24	21*	NC

*Optional, no connection necessary



V_{OUT} = (0 mA to 1.9995 mA) (R20)
= (0 mA to 1.9995 mA) (5k)
= 0V to 9.9976V

1 LSB = 2.44 mV

FIGURE 7. 10V Unipolar Operation

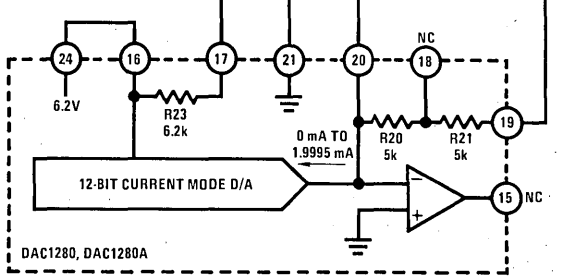


FIGURE 8. ±10V Bipolar Operation with External Operational Amplifier

3.3 Offset and Full-Scale Adjust

The DAC1280 series may be offset and full-scale adjusted using the circuit shown in *Figure 9*. Offset voltage should be adjusted first. A logic "1" (≥ 2V) should be applied to all logic inputs. In bipolar mode, the offset is adjusted to equal minus full-scale. In unipolar mode, the offset is adjusted to read 0V at the output. Full-scale is then adjusted by applying a logic "0" (≤ 0.8V) to all inputs for operation. The range of R1 and R2 shown in *Figure 9* is approximately ± 0.2% of full-scale for the values shown.

A 30 second "warm-up" period should be allowed (after power turn-on) before making the above adjustments.

3.4 Logic Input Coding

The logic inputs to the DAC1280 series are complementary; i.e., a given bit is turned ON by an active low input. Table II summarizes input status for unipolar and bipolar codes.

3.5 Reference Supply

The DAC1280 series is supplied with an internal 6.2V reference regulator (pin 24). In order to obtain the specified unadjusted performance, the reference output (pin 24) should be connected to the reference input (pin 16). An external reference voltage may be used with the DAC1280 series if provision is made to calibrate full-scale as shown in *Figure 9*. Since the reference is buffered, it may be used externally at currents up to 2.5 mA.

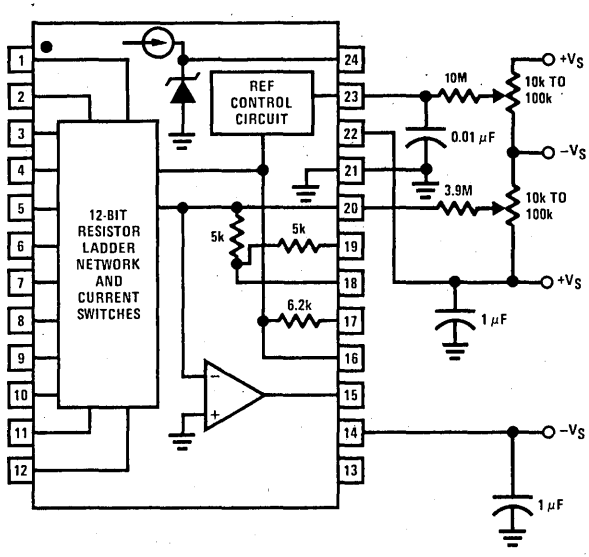


FIGURE 9. External Adjustment and Voltage Supply Connection Diagram

TABLE II

Code Type	Input Code (Note 7) MSB LSB	Output State	Unipolar Output Ranges		
			0V to 10V	0V to 5V	0 mA-2 mA 0 mA-1.25 mA
Unipolar	0 0 0 0 0 0 0 0 0 0 0 0	Full-Scale	9.9976V	4.9988V	−1.9995 mA
Complementary	1 1 1 1 1 1 1 1 1 1 1 0	1 LSB ON	0.0024V	0.0012V	−0.0005 mA
Binary	1 1 1 1 1 1 1 1 1 1 1 1	Zero-Scale	0.0000V	0.0000V	0.0000 mA

Code Type	Input Code (Note 7) MSB LSB	Output State	Bipolar Output Voltage Ranges			
			± 10V	± 5V	± 2.5V	± 1 mA
Bipolar	0 0 0 0 0 0 0 0 0 0 0 0	Full-Scale	9.9951V	4.9976V	2.4988V	−0.9995 mA
Complementary	0 1 1 1 1 1 1 1 1 1 1 1	Half-Scale	0.0000V	0.0000V	0.0000V	0.0000 mA
Binary	1 1 1 1 1 1 1 1 1 1 1 0	1 LSB ON	−9.9951V	−4.9976V	−2.4988V	0.9995 mA
	1 1 1 1 1 1 1 1 1 1 1 1	Zero-Scale	−10.0000V	−5.0000V	−2.5000V	1.0000 mA

Note 7: Logic input sense is such that an active low ($V_{IN} \leq 0.8V$) turns a given bit ON and is represented as a logic "0" in the table.

3.6 Logic Input Compatibility

The design of the current mode switches in the DAC1280 series gives the device true TTL compatibility. It is TTL compatible over the entire operating temperature range and is independent of the reference voltage and V_{CC}. Furthermore, since the input breakdown ratings are in excess of 10V, the DAC1280 series may be driven directly from high (or low) voltage CMOS.

3.7 ±12 Volt Supply Operation

The DAC1280A will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges −10V to +10V and 0V to 10V not be used with the DAC1280A if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{SUPPLY}| - |V_{OUT}\ \text{maximum}| < 2.0V$.

3.8 Power Supply Connections

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams *(Figure 5)*. These capacitors (1 μF electrolytic recommended) should be located close to the DAC1280A or DAC1280. Electrolytic capacitors, if used, should be paralleled with 0.01 μF ceramic capacitors for optimum high frequency performance.

National Semiconductor

DAC1285A, DAC1285 (DAC85, DAC87) 12-Bit Digital-to-Analog Converters

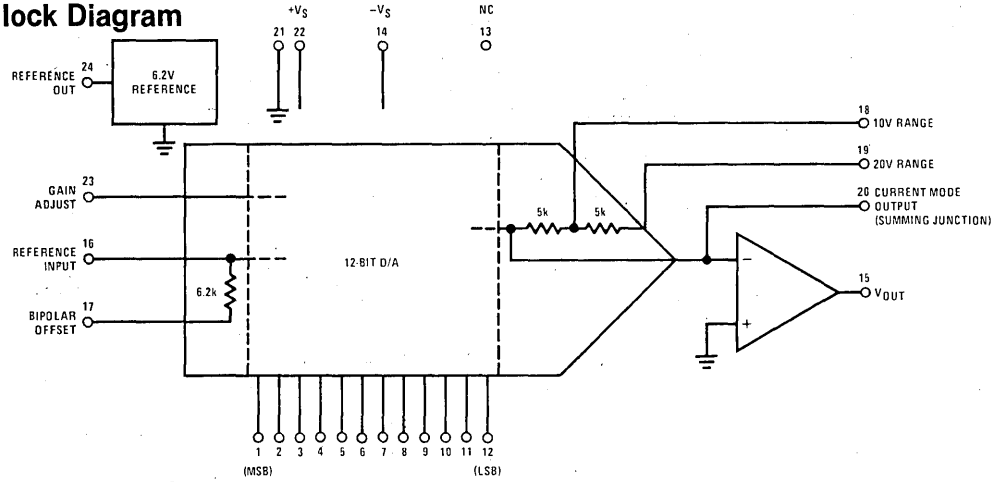
General Description

The DAC1285 series is a family of precision, low cost, fully self-contained digital-to-analog converters. The devices include 12 precision current switches, a 12-bit thin film resistor network, output amplifier, buffered internal reference, and several precision resistors, which allow the user to tailor his system needs to accommodate a variety of bipolar and unipolar output voltage and current ranges. Logic inputs are TTL, DTL and CMOS compatible, and are complementary binary (CBI) format. In all instances, a logic low ($\leq$0.8V) turns a given bit ON, and a logic high ($\geq$ 2V) turns a given bit OFF. Internally supplied resistor options provide low drift bipolar output voltage ranges of $\pm$ 2.5V, $\pm$ 5V, $\pm$ 10V, and unipolar ranges of 0V to 5V or 0V to 10V. Current mode output is 0 mA to 2 mA.

Features

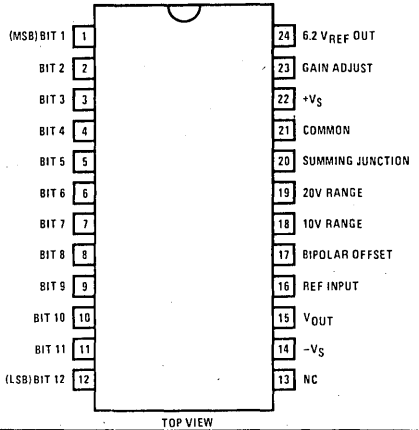
- Completely self-contained with internal reference and output amplifier
- High reliability exact replacement for DAC85-CBI-V, DAC85LD-CBI-V, and DAC87-CBI-V
- $\pm$ 1/2 LSB linearity max over temperature range
- $\pm$ 2.5V, $\pm$ 5V, $\pm$ 10V, 0V to 5V, 0V to 10V voltage outputs
- 0 mA to 2 mA current output
- Fast settling time: 300 ns current mode; 2.5 μs voltage mode
- Hermetic 24-pin IC package
- Low cost
- TTL CMOS compatible binary input logic over temperature
- Parameters guaranteed over operating temperature range $-25°C$ to $+85°C$ or $-55°C$ to $+125°C$

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number
DAC1285ACD, DAC85LD-CB1-V,
DAC1285HCD, DAC85-CB1-V,
DAC1285AD, DAC87-CB1-V
See NS Package D24G

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	± 18V
Current Output (Pin 20) Compliance	± 10V
Logic Input Voltage	−0.7V, 10V
Reference Input Voltage (V_{REF})	0V, 18V
Short-Circuit Duration (Pins 15, 20 and 24)	Continuous

Operating Temperature Range	
DAC1285A	−55°C to +125°C
DAC1285AC	−25°C to +85°C
DAC1285HC	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$T_A = -55°C$ to $+125°C$ for DAC1285A and $-25°C$ to $+85°C$ for DAC1285AC and DAC1285HC, $V_S = \pm 11.4V$ to $\pm 15.75V$ for DAC1285A and DAC1285AC and $V_S = \pm 15V$ for DAC1285HC unless otherwise noted.

Parameter	Conditions	DAC1285A			DAC1285AC			DAC1285HC			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
CONVERTER CHARACTERISTICS											
Resolution		12			12			12			Bits
Linearity Error	$T_A = 25°C$		± 1/4	± 1/2		± 1/4	± 1/2		± 1/4	± 1/2	LSB
				± 3/4			± 1/2			± 1/2	
Differential Non-Linearity	$T_A = 25°C$		± 1/2	± 3/4		± 1/2			± 1/2		
				± 1							
Monotonicity		12			12			12			Bits
Full-Scale (Gain) Error	$T_A = 25°C$ (Note 2)		± 0.1	± 0.2		± 0.1			± 0.1		% FSR (Note 3)
Zero-Scale (Offset) Error	$T_A = 25°C$ (Note 2)		± 0.02	± 0.1		± 0.02			± 0.02		
Full-Scale (Gain) Tempco	With Internal Reference		± 10	± 20		± 10			± 15	± 30	ppm/°C
	Without Internal Reference		± 5	± 10		± 5	± 10		± 5	± 20	
Zero-Scale (Offset) Tempco	Unipolar		± 1	± 3		± 1			± 1		ppm FSR/°C
	Bipolar		± 3	± 10		± 3	± 5		± 3	± 10	
Total Bipolar Tempco (Note 4)	Includes Gain, Offset, and Linearity		± 10	± 30		± 10			± 10		
Total Error (Note 5)	Unipolar		± 0.08	± 0.3		± 0.08			± 0.08		% FSR
	Bipolar		± 0.06	± 0.24		± 0.06			± 0.06		
Output Voltage Range	Using Internally Supplied Resistors (Note 6)	± 2.5V, ± 5V, ± 10V, 0V to 5V, 0V to 10V									V
Output Voltage Swing	$R_L \geq 5$ kΩ, Pin 15	± 10			± 10			± 10			
Output Short Circuit Current	Pin 15	± 5	± 25	± 50	± 5	± 25	± 50	± 5	± 25	± 50	mA
Output Impedance	Pin 15, Closed Loop		0.05			0.05			0.05		Ω
Current Mode Output Range	Unipolar, Pin 20		0 to −2			0 to −2			0 to −2		mA
	Bipolar, Pin 20		± 1.0			± 1.0			± 1.0		
Current Mode Compliance				± 2.5			± 2.5			± 2.5	V
Current Mode Output Impedance	Unipolar		2			2			2		kΩ
	Bipolar		1.5			1.5			1.5		
REFERENCE CHARACTERISTICS											
Reference Voltage	$I_{REF} \leq 2$ mA, $T_A = 25°C$	6.07	6.2	6.33	6.07	6.2	6.33		6.2		V
Tempco of Drift			± 5	± 10		± 10	± 20		± 10	± 20	ppm/°C
External Use Current				2.5			2.5			2.5	mA
Output Impedance			0.05	1.0		0.05	1.0		0.05	1.0	Ω

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Electrical Characteristics (Continued)

$T_A = -55°C$ to $+125°C$ for DAC1285A and $-25°C$ to $+85°C$ for DAC1285AC and DAC1285HC, $V_S = \pm 11.4V$ to $\pm 15.75V$ for DAC1285A and DAC1285AC and $V_S = \pm 15V$ for DAC1285HC unless otherwise noted.

Parameter	Conditions	DAC1285A, DAC1285AC			DAC1285HC			Units
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
DIGITAL AND DC CHARACTERISTICS								
Logic "1" Input Voltage (Bit OFF)		2.0			2.0			V
Logic "0" Input Voltage (Bit ON)				0.8			0.8	V
Logic "1" Input Current	$V_{IN} = 2.5V$		0.05	1		0.05	1	μA
Logic "0" Input Current	$V_{IN} = 0V$			−100			−100	μA
Power Supply Current	I^+, $T_A = 25°C$		10	18		10		mA
	I^-, $T_A = 25°C$		25	30		25		mA
Power Supply Sensitivity			0.001	0.002		0.001		% FSR/%V
AC CHARACTERISTICS								
Voltage Mode Settling Time	1 LSB Change		400			400		ns
	FSR Change 10V		2.5			2.5		μs
	FSR Change 20V		4			4		μs
Voltage Mode Slew Rate	$T_A = 25°C$	10	30			30		V/μs
Current Mode Settling Time	10Ω to 100Ω Load		300			300		ns

Note 1: All typical values are for $T_A = 25°C$.

Note 2: Externally adjustable to zero.

Note 3: FSR means "full-scale range" and is 20V for ± 10V range, 10V for ± 5V, etc.

Note 4: See paragraph 2.0 for definition.

Note 5: With gain and offset errors adjusted to zero at 25°C

Note 6: $\pm V_S$ must have absolute value 2V greater than V_{OUT}. Output voltage ranges −10V to +10V and 0V to +10V are not recommended with V_S less than ± 12V.

1.0 Definition of Terms

1.1 Accuracy

Accuracy of a D/A converter is the difference between the actual analog output that is measured when a given digital code is applied and the analog output that is expected with that code applied to the converter. Accuracy errors can be specified by the three parameters of gain or full-scale error, zero-scale or offset error, and linearity error.

1.2 Linearity Error

Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

1.3 Differential Linearity Error and Monotonicity

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ± 1/2 LSB means that the output voltage step sizes can range from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next. 12-bit monotonicity is guaranteed to ensure that the analog output will not decrease with increasing input digital codes.

1.4 Gain Tempco

Gain tempco is a measure of the change in the full-scale range output over temperature expressed in parts per million per °C (ppm/°C).

1.5 Offset Tempco

Offset tempco is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at low and high temperature. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This offset change is expressed in parts per million of full-scale range per °C (ppm of FSR/°C).

1.6 Settling Time

Settling time for each DAC1285 series part is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input *(Figures 1 and 2)*.

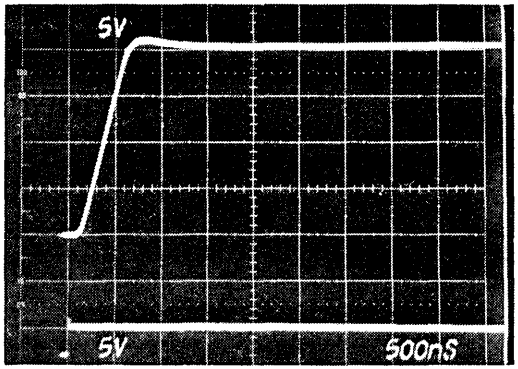


FIGURE 1. Voltage Mode Settling Time-FSR Change

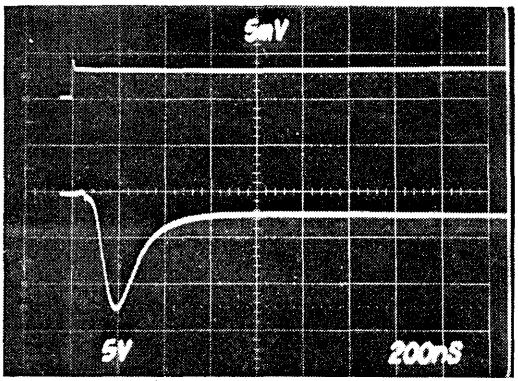


FIGURE 2. Voltage Mode Settling Time-1 LSB Change

Voltage Output. Three settling times are specified to ±0.01% of full-scale range (FSR); two for maximum full-scale range changes of 20V, 10V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output. Settling time is specified to ±0.01% of FSR. This is given with a range of resistive loads: 10Ω to 100Ω.

1.7 Compliance

Compliance voltage is the maximum voltage swing allowed on the current output pin (pin 20). Note that the absolute current offset error with any DAC will be increased by an amount given by V_{OUT}/R_{OUT}. In many situations this will be a significant error term if the voltage on the current output pin is allowed to exceed a few millivolts.

1.8 Power Supply Sensitivity

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

1.9 Reference Supply

The DAC1285 series are supplied with an internal 6.2V reference voltage supply. This voltage (pin 24) is accurate to ±2% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5 mA. All gain adjustments should be made under constant load conditions.

2.0 Analyzing Device Accuracy Over the Temperature Range

For the purposes of temperature drift analysis, the major device components are shown in *Figure 3*. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient, which is specified as a maximum. The input reference current to the DAC, I_{REF}, is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC}, which is a function of the digital input code, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain TC. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

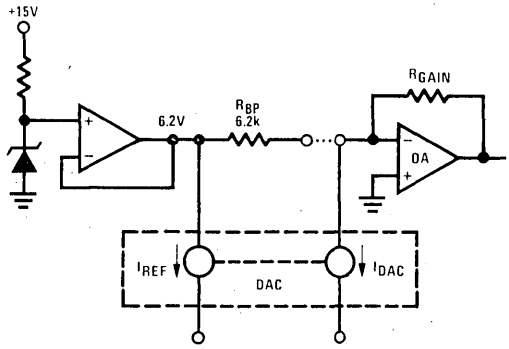


FIGURE 3. Bipolar Configuration

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full-scale. A specification for total error over temperature assumes that both the zero and full-scale points have been trimmed for zero error at 25°C. Total error is normally expressed as a percentage of the full-scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

2.1 Monotonicity and Linearity

The initial linearity error and the differential linearity error guarantee monotonic performance over the operating temperature range. It can therefore be assumed that linearity errors are insignificant in computation of total temperature errors.

2.2 Unipolar Errors

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift, which comes from leakage currents and drift in the output amplifier, causes a linear shift in the transfer curve as shown in *Figure 4*. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in R_{GAIN} relative to the DAC resistors.

2.3 Bipolar Range Errors

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to the summing node of the output amplifier (see *Figure 3*) to generate a current which exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in *Figure 6*. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift. Gain drift in the DAC also contributes to bipolar offset drift, as well as full-scale drift. In the bipolar ranges, full-scale is defined as the total range from $-V_{FS}$ to $+V_{FS}$.

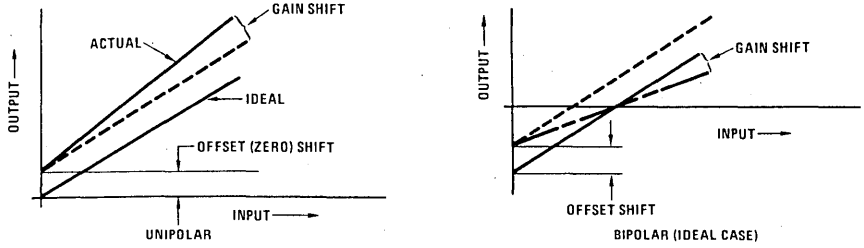


FIGURE 4. Unipolar and Bipolar Drifts

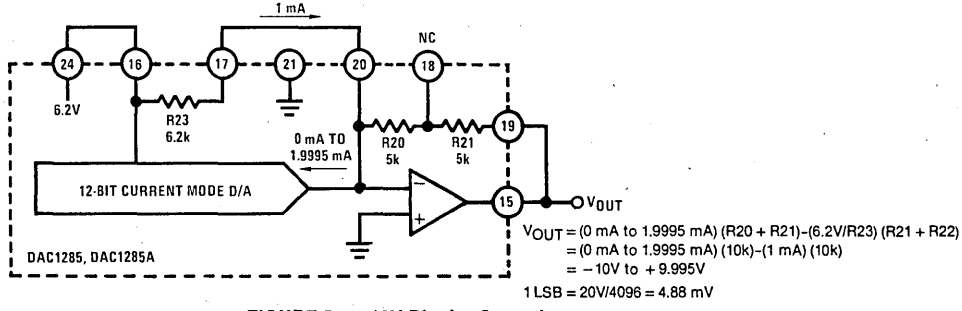


FIGURE 5. ±10V Bipolar Operation

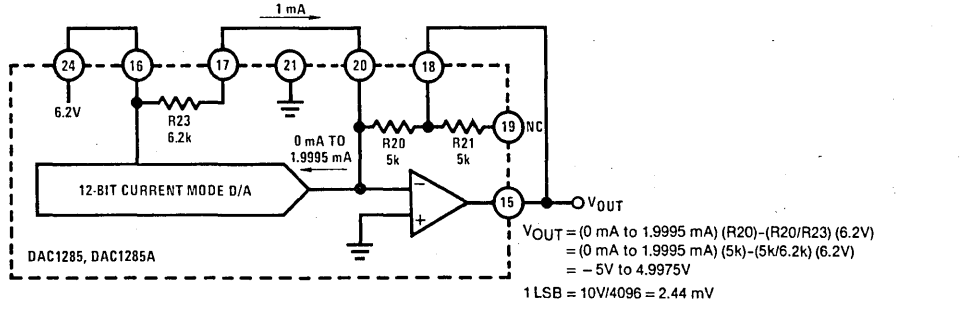


FIGURE 6. ±5V Bipolar Operation

3.0 Applications and Functional Description

3.1 Voltage Mode Operation

These D/As provide internal scaling resistors which permit a wide range of bipolar and unipolar output configurations. Bipolar output formats of ± 2.5V, ± 5V, ± 10V and unipolar formats of 0V to 5V and 0V to 10V are possible using resistor strap options included within the device. Table I and *Figures 5, 6 and 7* summarize the proper pin connections required for these formats.

3.2 Current Mode Operation

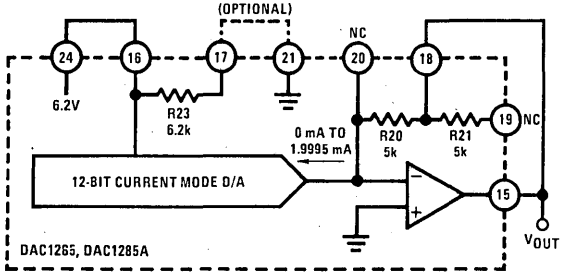
Current mode applications which make use of an external op amp, comparator, or a resistive load are possible with the DAC1285 series using pin 20. When an external op amp is used, the internal scaling resistors should be utilized to minimize full-scale drift. Configurations shown in Table I apply directly. *Figure 8* shows one application using an external fast operational amplifier.

Current mode operation into a resistive load or open circuit must account for the DACs nominal output resistance of 2k at pin 20. With this in mind, the output will swing 0V to −4V open circuit and about −1.5V to +1.5V with the bipolar offset resistor connected. An external load resistor may be used as part of the load, but there will be an error due to temperature coefficients mistracking.

TABLE I. Output Voltage/Current Ranges for DAC1285 Series

Output Range	Digital Input Code	Connect Pin 15 to	Connect Pin 16 to	Connect Pin 17 to	Connect Pin 19 to
± 10V	Complementary Offset Binary	19	24	20	15
± 5V	Complementary Offset Binary	18	24	20	NC
± 2.5V	Complementary Offset Binary	18	24	20	20
10V	Complementary Binary	18	24	21*	NC
5V	Complementary Binary	18	24	21*	20
± 1 mA	Complementary Offset Binary	NC	24	20	NC
− 2 mA	Complementary Binary	NC	24	21*	NC

*Optional, no connection necessary



V_{OUT} = (0 mA to 1.9995 mA) (R20)
= (0 mA to 1.9995 mA) (5k)
= 0V to 9.9976V
1 LSB = 2.44 mV

FIGURE 7. 10V Unipolar Operation

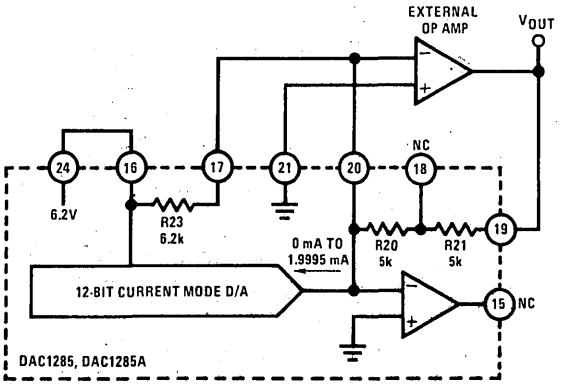


FIGURE 8. ± 10V Bipolar Operation with External Operational Amplifier

3.3 Offset and Full-Scale Adjust

The DAC1285 series may be offset and full-scale adjusted using the circuit shown in *Figure 9*. Offset voltage should be adjusted first. A logic "1" (≥2V) should be applied to all logic inputs. In bipolar mode, the offset is adjusted to equal minus full-scale. In unipolar mode, the offset is adjusted to read 0V at the output. Full-scale is then adjusted by applying a logic "0" (≤0.8V) to all inputs for operation. The range of R1 and R2 shown in *Figure 9* is approximately ± 0.2% of full-scale for the values shown.

A 30 second "warm-up" period should be allowed (after power turn-on) before making the above adjustments.

3.4 Logic Input Coding

The logic inputs to the DAC1285 series are complementary; i.e., a given bit is turned ON by an active low input. Table II summarizes input status for unipolar and bipolar codes.

3.5 Reference Supply

The DAC1285 series is supplied with an internal 6.2V reference regulator (pin 24). In order to obtain the specified unadjusted performance, the reference output (pin 24) should be connected to the reference input (pin 16). An external reference voltage may be used with the DAC1285 series if provision is made to calibrate full-scale as shown in *Figure 9*. Since the reference is buffered, it may be used externally at currents up to 2.5 mA.

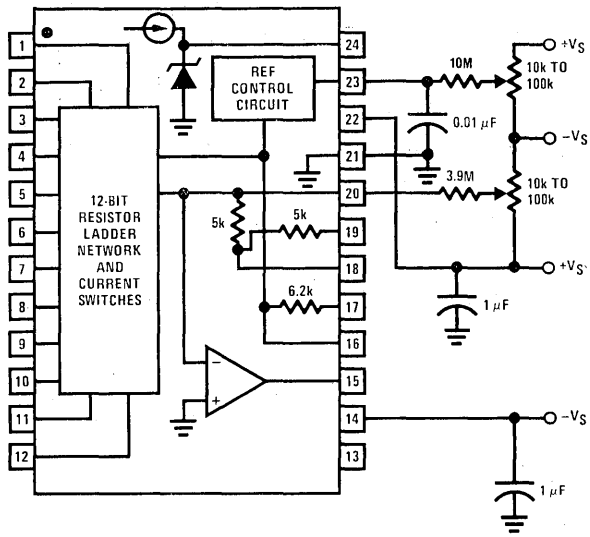


FIGURE 9. External Adjustment and Voltage Supply Connection Diagram

TABLE II

Code Type	Input Code (Note 7) MSB LSB	Output State	Unipolar Output Ranges		
			0V to 10V	0V to 5V	0 mA-2 mA 0 mA-1.25 mA
Unipolar	0 0 0 0 0 0 0 0 0 0 0 0	Full-Scale	9.9976V	4.9988V	−1.9995 mA
Complementary	1 1 1 1 1 1 1 1 1 1 1 0	1 LSB ON	0.0024V	0.0012V	−0.0005 mA
Binary	1 1 1 1 1 1 1 1 1 1 1 1	Zero-Scale	0.0000V	0.0000V	0.0000 mA

Code Type	Input Code (Note 7) MSB LSB	Output State	Bipolar Output Voltage Ranges			
			± 10V	± 5V	± 2.5V	± 1 mA
Bipolar	0 0 0 0 0 0 0 0 0 0 0 0	Full-Scale	9.9951V	4.9976V	2.4988V	−0.9995 mA
Complementary	0 1 1 1 1 1 1 1 1 1 1 1	Half-Scale	0.0000V	0.0000V	0.0000V	0.0000 mA
Binary	1 1 1 1 1 1 1 1 1 1 1 0	1 LSB ON	−9.9951V	−4.9976V	−2.4988V	0.9995 mA
	1 1 1 1 1 1 1 1 1 1 1 1	Zero-Scale	−10.0000V	−5.0000V	−2.5000V	1.0000 mA

Note 7: Logic input sense is such that an active low ($V_{IN} \leq 0.8V$) turns a given bit ON and is represented as a logic "0" in the table.

3.6 Logic Input Compatibility

The design of the current mode switches in the DAC1285 series gives the device true TTL compatibility. It is TTL compatible over the entire operating temperature range and is independent of the reference voltage and V_{CC}. Furthermore, since the input breakdown ratings are in excess of 10V, the DAC1285 series may be driven directly from high (or low) voltage CMOS.

3.7 ±12 Volt Supply Operation

These DACs will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges −10V to +10V and 0V to 10V not be used if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{SUPPLY}| - |V_{OUT}$ maximum$| < 2.0V$.

3.8 Power Supply Connections

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams *(Figure 9)*. These capacitors (1 μF electrolytic recommended) should be located close to the device. Electrolytic capacitors, if used, should be paralleled with 0.01 μF ceramic capacitors for optimum high frequency performance.

Ordering Information

Part Number	Temperature Range	Package
DAC1285ACD DAC85LD-CBI-V	−25°C to +85°C	D24G
DAC1285HCD DAC85-CBI-V		
DAC1285AD DAC87-CBI-V	−55°C to +125°C	

* Devices may be ordered by either part number.

Section 13

13

Fiber-Optic Products

Fiber-Optic Product Selection Guide

Function	Features				−55°C to +125°C	−25°C to +85°C	Page
	Bandwidth*	Drive Current*	Coupled Power*	λ			
Complete Transmitter with LED	DC to 20 Mbits	100mA (max.)	110μW	820nm		FOT180B	13-21

Function	Features			−55°C to +125°C	−25°C to +85°C	Page
	Bandwidth*	Sensitivity*	Power Required for Max. Bit Rate*			
Receiver	DC to 10 Mbits	−55 dBm		LH0082D	LH0082CD	13-4
Complete Receiver with Photodiode	DC to 5 Mbits	−45 dBm	2μW		FOR100B	13-18
Monolithic Receiver with Integral Photodiode	DC to 10 Mbits	−22 dBm	7μW		FOR261F	13-26

*Consult data sheet for descriptions and conditions.

National Semiconductor

LH0082 Optical Communication Receiver

General Description

The LH0082 is a general purpose, low-noise, fiber optic receiver, which may also be used as a fast current to voltage converter, or as a high speed voltage amplifier. The circuit includes a 2GHz gain-bandwidth FET-input amplifier, a 2.4 volt reference, a comparator with hysteresis, and all the necessary resistors and capacitors for feedback and coupling, all integrated in a hermetic dual-in-line package. The large gain-bandwidth of the preamp enables fast response even with high capacitance photodiodes. A separate analog output permits the reception of analog signals to 20MHz via a fiber optic link. The internal comparator converts a low level analog signal to a CMOS/TTL/DTL compatible logic signal at data rates up to 15Mbits/s NRZ. The LH0082 can be used with an external comparator at data rates to 50Mbits/s.

Features

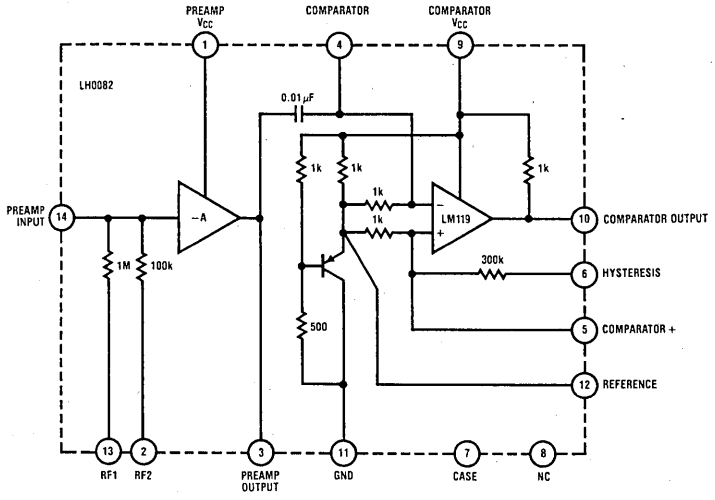
- Single 4.5 to 12 Volt Supply
- DC to 50 Mbits/s NRZ Data Bandwidth
- Low Noise
- $< 10^{-9}$ Bit Error Rate
- Low Input Bias Current
- Pin Selectable Sensitivity: −45dBm/−35dBm*
- CMOS/TTL/DTL Compatibility
- Can be used with photodiodes, PIN photodiodes, phototransistors, avalanche photodiodes, and photomultipliers
- Hermetic Dual In Line Metal Package
- Highly Versatile Building Block
- > 45dB Dynamic Range

*Assumes 0.5A/W PIN diode input

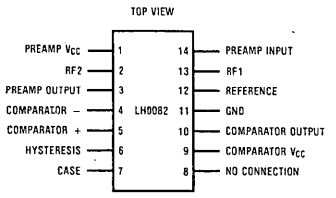
Applications

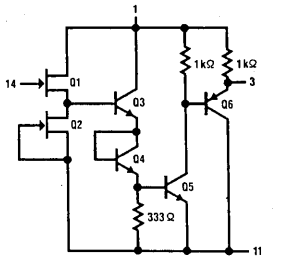
- Data Terminals
- Secure Communication
- Peripheral Control/Communication
- Video Transmission
- Wideband Amplifier
- High Speed Current to Voltage Converter
- Fiber-Optic Repeater
- Video Amplifier
- Industrial Machine Control

LH0082 Schematic Diagram



Connection Diagram





Order Number
LH0082D or LH0082CD
See Package D14F

Absolute Maximum Ratings

Supply Voltage	+15V
Power Dissipation, $T_A = 25°C$	0.5W
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C
Operating Temperature Range	
LH0082D	−55°C to 125°C
LH0082CD	−25°C to 85°C
Lead Temperature (Soldering, 20 Seconds)	300°C
Input Voltage	$V_{CC} - 20 < V_{IN} < V_Q$

Electrical Characteristics Preamplifier: Power supply voltage = $+5V_{DC}$, $T_A = 25°C$, see Figure 1

	Parameter	Min.	Typ.	Max.	Units
I_B	Input Bias Current		100		pA
C_{IN}	Input Capacitance			5	pF
A_V	Voltage Gain		90		V/V
f_{3dB}	−3dB Frequency		18		MHz
V_Q	Output Quiescent Voltage	1.9	2.1	2.6	V
$\Delta V_Q/\Delta T$	Output Quiescent Voltage Drift with Temperature		−6		mV/°C
Z_O	Open Loop Output Impedance at 1 MHz		30		Ω
	Output Noise (10 Hz to 10 MHz)		300		μV RMS
V_O	Output Swing (No Load)	3.5	4.0		V_{P-P}
	Transimpedance:				
	Low Sensitivity	90	100	110	kΩ
	High Sensitivity	0.9	1	1.1	MΩ
I_S	Supply Current		22	30	mA

Electrical Characteristics Comparator/Reference: Power supply voltage = $+5V_{DC}$, $T_A = 25°C$, see Figure 2

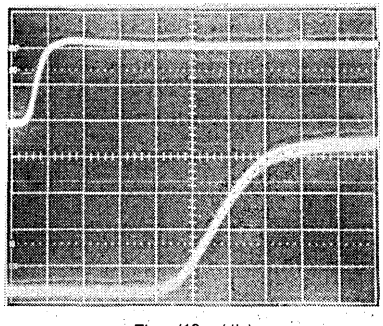
	Parameter	Min.	Typ.	Max.	Units
R_{IN}	Comparator Input Resistance (to reference)	0.95	1	1.05	kΩ
V_{HYST}	Hysteresis Voltage				
	Positive	7	8.7	11.4	mV
	Negative	5	6.9	8.8	mV
R_O	Output Pullup Resistor	0.95	1	1.05	kΩ
V_R	Reference Voltage	2.2	2.4	2.6	V
$\Delta V_R/\Delta T$	Reference Voltage Drift with Temperature		−2		mV/°C
R_O (V_{REF})	Reference Voltage Output Resistance		15		Ω
V_{OL}	($I_{OL} = 3.2mA$)		0.3	0.5	V
V_{OH}	($I_{OH} = -1mA$)	3.8	4		V
T_{PD}	($V_{IN} = 30mV$, $V_{OD} = 15mV$)		160		ns
T_R	($C_L = 3pF$)		80		ns
T_F	($C_L = 3pF$)		60		ns
I_S	Supply Current:				
	Output High	4.5	8	17	mA
	Output Low	9.5	13	22	mA

Electrical Characteristics Fiber Optic Receiver:

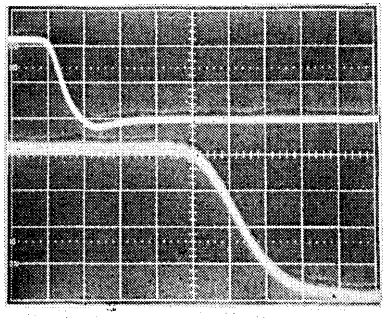
Photodiode responsivity is assumed to be 0.5A/W, capacitance of 10pF at 2.5V reverse bias, $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$

	Parameter	Min.	Typ.	Max.	Units
	High Sensitivity: $R_F = 1M\Omega$, see Figure 3.				
	Input Power for 10^{-9} BER (bit rate = 500Kbit NRZ)		30		nW
t_r, t_f	Analog Output Rise or Fall Time		1.5		μs
	Maximum Data Rate, NRZ, Digital Output		650		Kbit/s
P_N	Noise Equivalent Power		1		nW
i_N	Equivalent Input Noise Current (10Hz to 10MHz)		300		pA RMS
	Low Sensitivity: $R_F = 100K\Omega$, see Figure 4				
	Input Power for 10^{-9} BER (bit rate = 2Mbit NRZ)		300		nW
t_r, t_f	Analog Output Rise or Fall Time		50		ns
	Maximum Data Rate, NRZ, Digital Output		5		Mbit/s
P_N	Noise Equivalent Power		10		nW
i_N	Equivalent Input Noise Current (10Hz to 10MHz)		3		nA RMS
I_S	Total Supply Current (High or Low Sensitivity)		35		mA

Fiber optic receiver preamp response
$R_F = 100\,k\Omega$
Photodiode capacitance = 10pF, $V_{CC} = 5V$

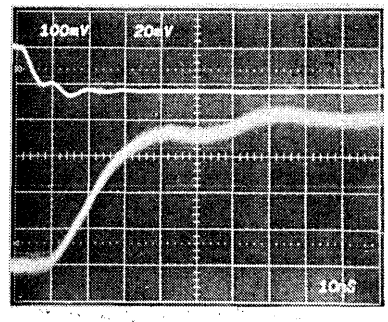


Time (10 ns/div)

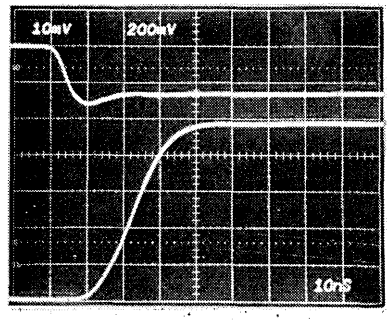


Time (10 ns/div)

Preamp Voltage Mode Pulse Response



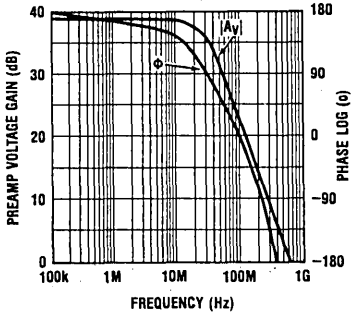
Small Signal



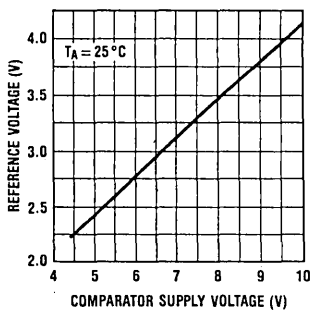
Large Signal

Typical Performance Characteristics

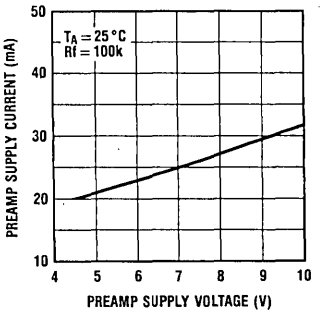
Open Loop Voltage Gain



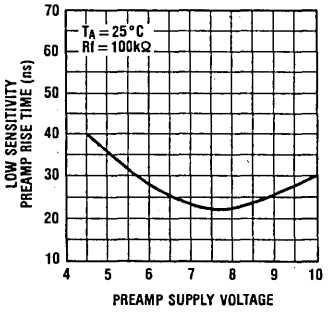
Reference Voltage



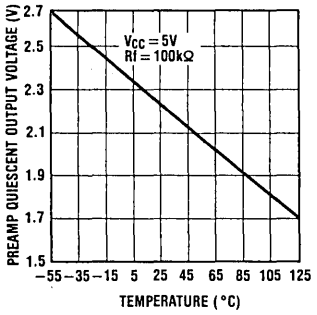
Supply Current



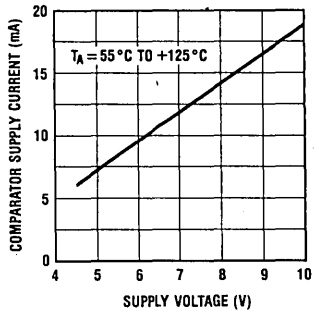
Response Time



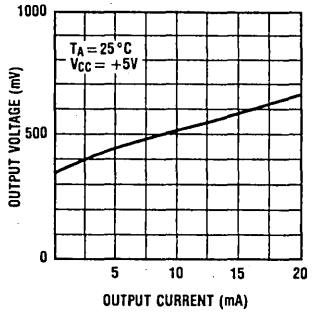
Output Voltage



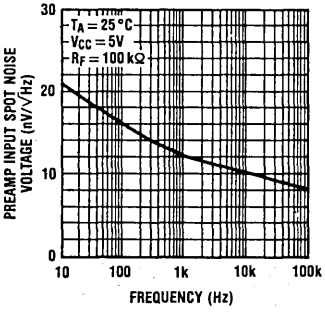
Comparator Supply Current (Output High)



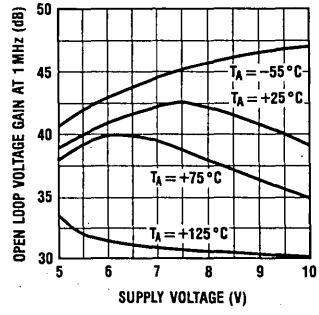
Comparator Output Saturation Voltage



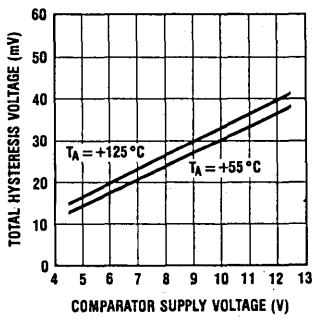
Preamp Input Spot Noise Voltage



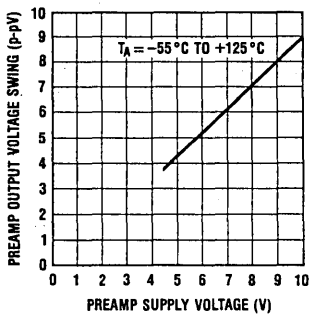
Preamp Open Loop Voltage vs. Supply Voltage



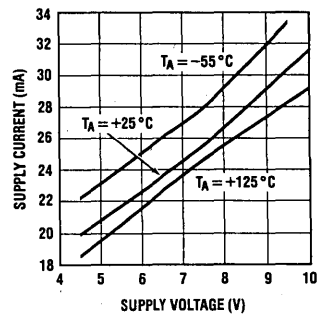
Hysteresis Voltage vs. Comparator Supply Voltage

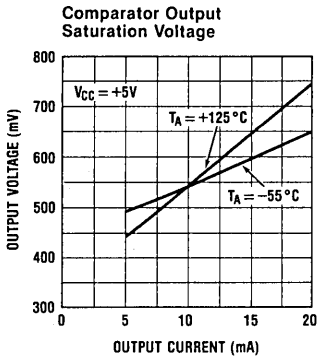


Preamp Output Voltage Swing



Preamp Supply Current





Applications Information

The gain-bandwidth of the LH0082 preamp is nearly 2GHz, thus good bypassing of the supply voltage is necessary; a 3.3μF tantalum capacitor in parallel with a 0.01μF ceramic disc is recommended, placed as close as possible to the device pins.

Careful shielding of pins 2, 13, and 14 is necessary if the LH0082 is used in a high noise environment. Minimize stray capacitance to pin 14 from ground, V_{CC} or pin 3 to avoid slowing overall circuit response. Choose the lowest capacitance photodiode possible for the application. When using phototransistors, only the collector-base junction should be used for fastest response. Additional sensitivity may be gained by using a phototransistor in the transistor mode, although this will result in slower circuit response, and poor DC stability due to beta multiplication of the dark current of the phototransistor. Avoid capacitive loading at the output of the comparator to achieve maximum data rates.

Avalanche photodiodes can be used for improved sensitivity and speed. Overall speed is limited by the internal comparator. Use of an external comparator such as the LM160 will enable the full speed capability to be realized. This requires the use of an additional power supply, see Figure 8.

Increased speed of response may be realized in the high sensitivity mode by the addition of a resistor and a capacitor as shown in Figure 5. The resistor value may need to be adjusted to give a flat frequency response for differing circuit layouts. Figure 6 illustrates how very high sensitivity can be achieved by adding the desired feedback resistor.

The low sensitivity mode's speed of response may also be increased (as shown in Figure 7). A network must be added to the comparator to adjust for frequency dependent thresholds caused by the 0.01 coupling capacitor internal to the LH0082. Figure 8 shows the use of an external comparator to enable 50 Mbit data rates. Figures 9, 10, and 11 demonstrate interfacing techniques to avalanche photodiodes and phototransistors.

With a few additional components, the LH0082 can be used as a repeater as shown in Figure 12. Interfacing to a microcomputer-bus, (Figure 13), is also easy when the LH0082 is teamed with an INS8250 Asynchronous Communications Element. This provides a full duplex link capable of bit rates to 56Kbits/S.

Analog data can be sent along a fiber optic cable via digital means, (Figure 14), or by analog means and recovered as shown in Figure 7. Low temperature drift can be obtained in the analog mode, by using the circuit of Figure 15.

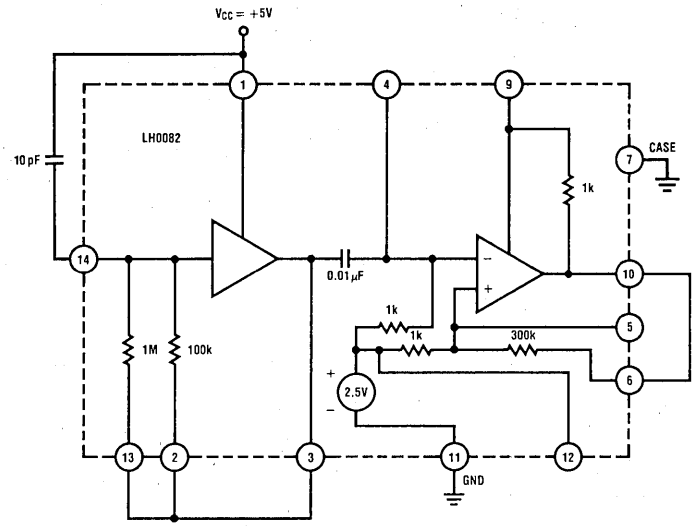


Figure 1. Preamp Test Circuit

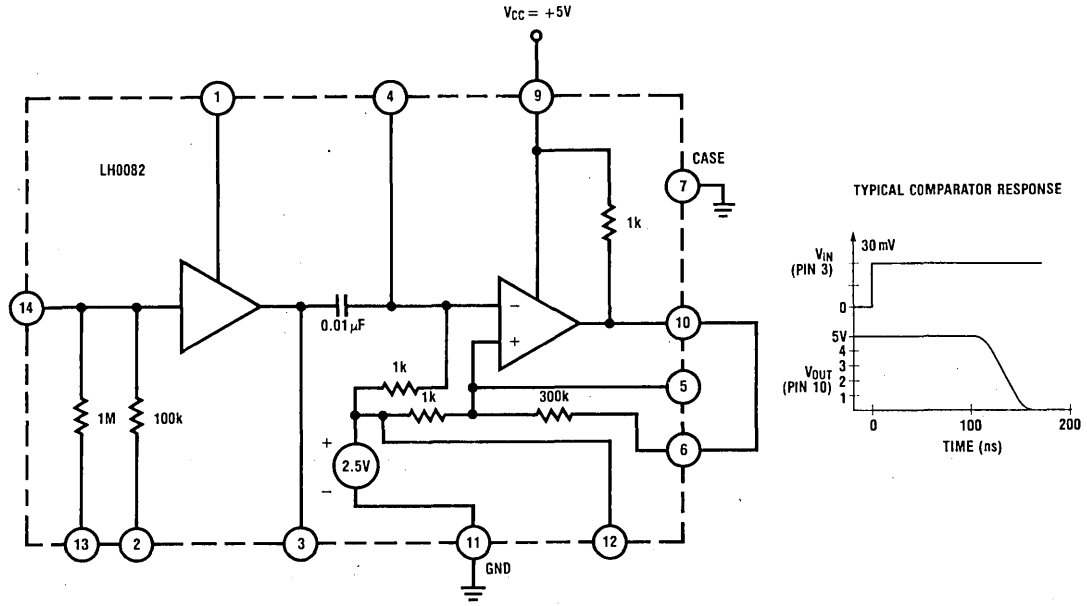


Figure 2. Comparator Test Circuit

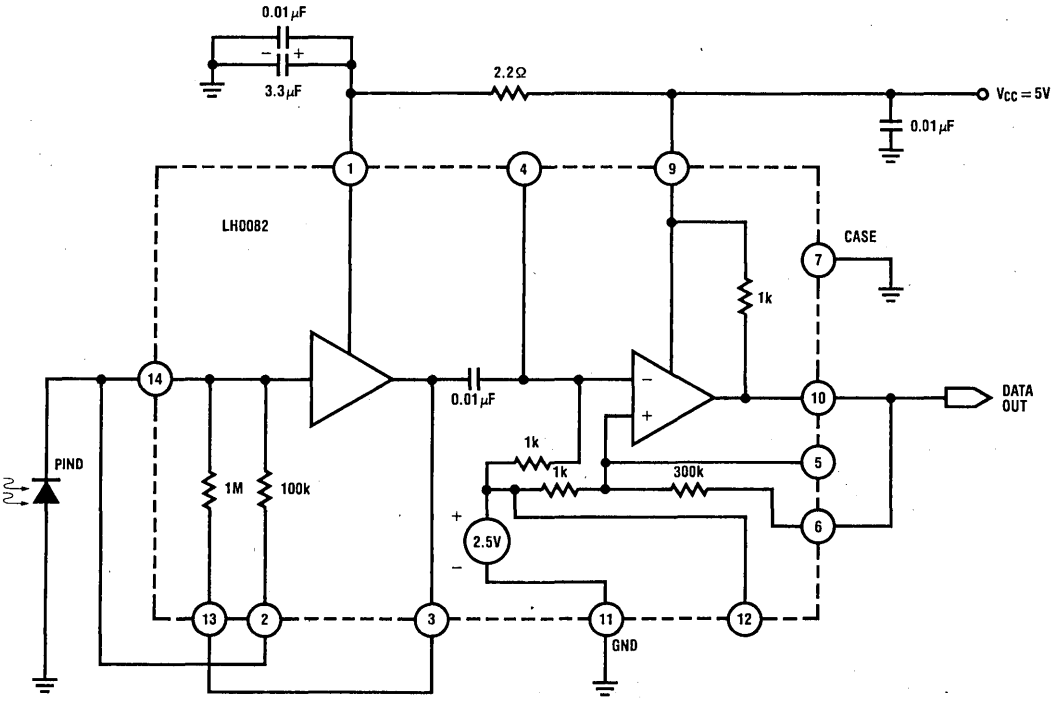


Figure 3. Fiber-Optic Receiver, Basic High Sensitivity: 30nW, 400kbps

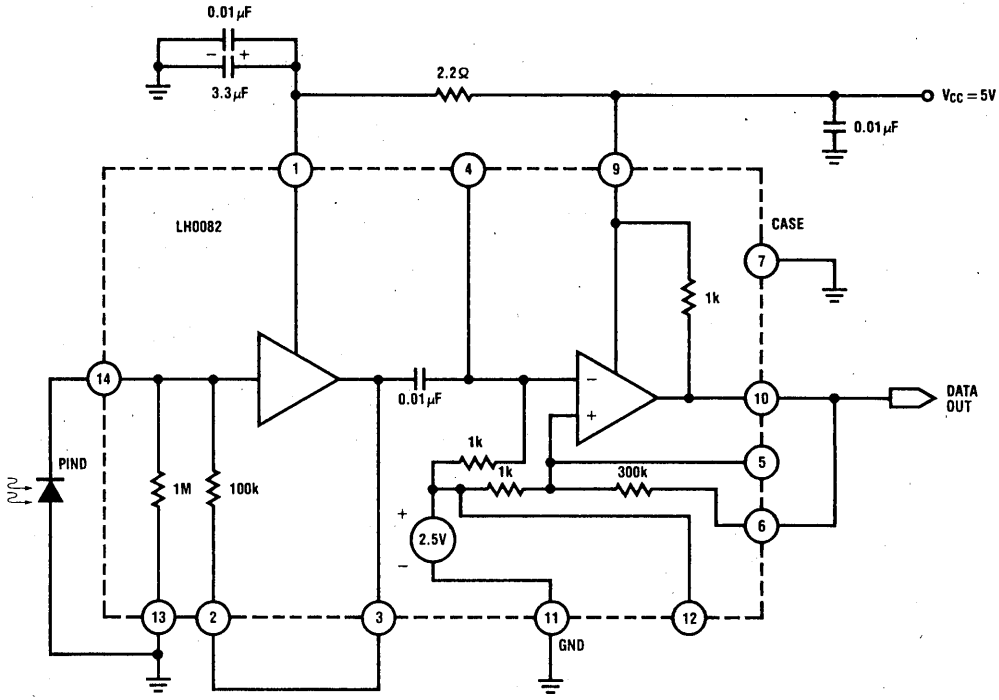


Figure 4. Fiber-Optic Receiver, Basic Low Sensitivity: 2μW, 5Mbit

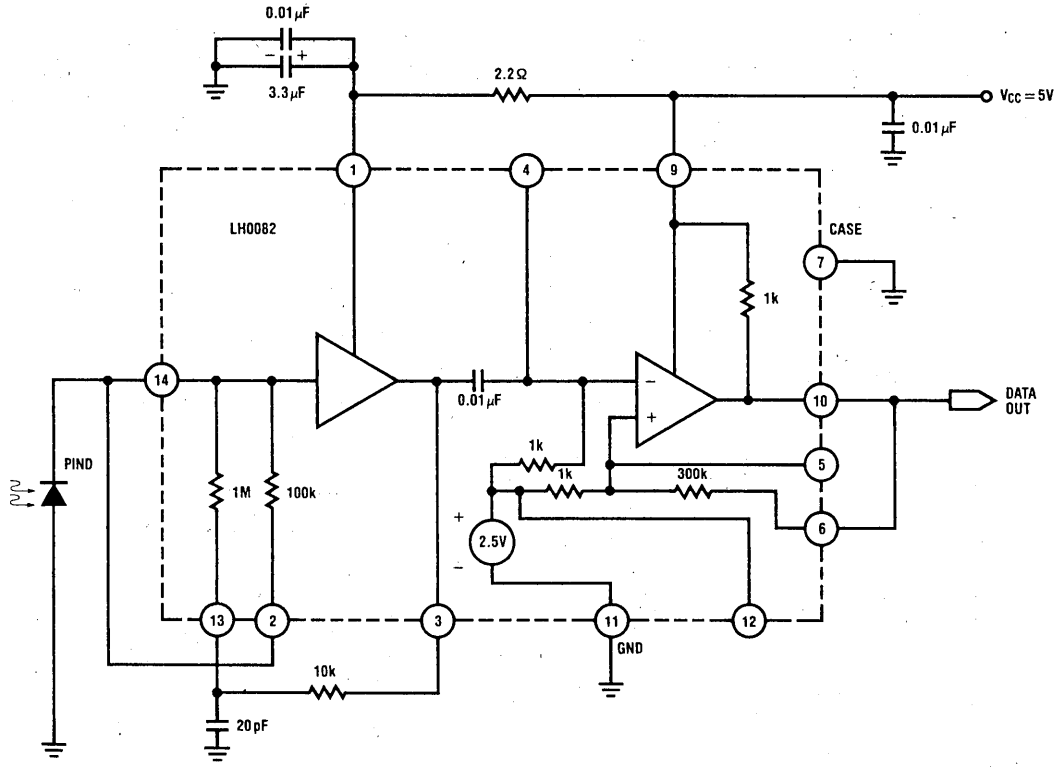


Figure 5. Fiber-Optic Receiver, High Sensitivity—Improved Speed

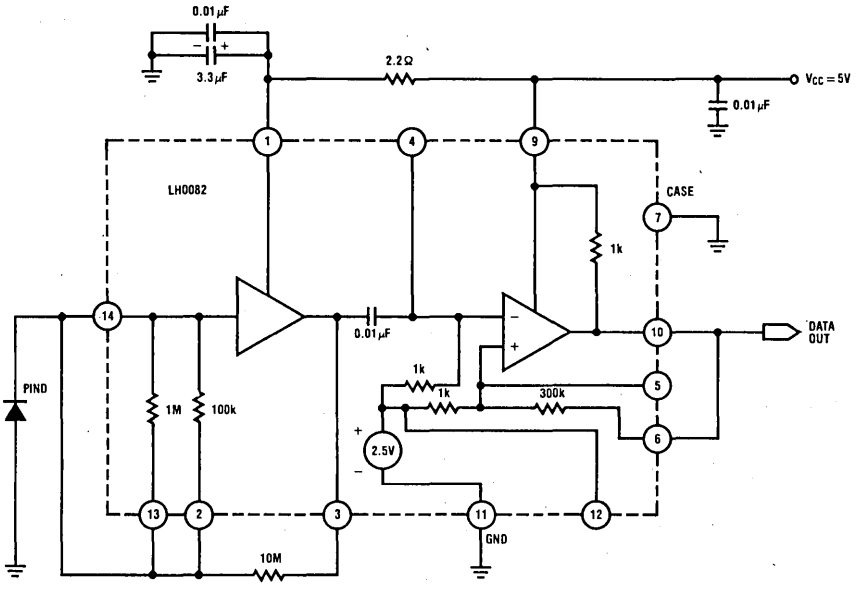
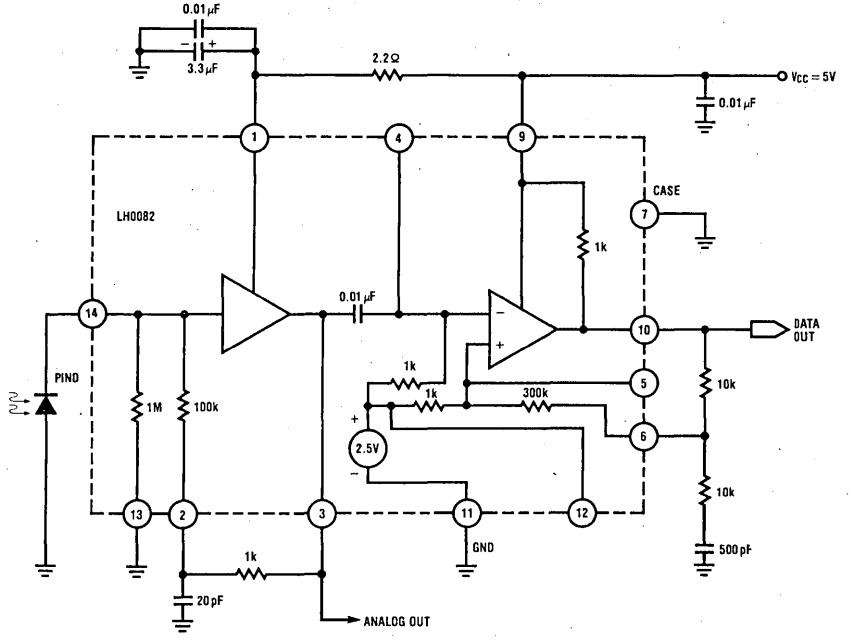
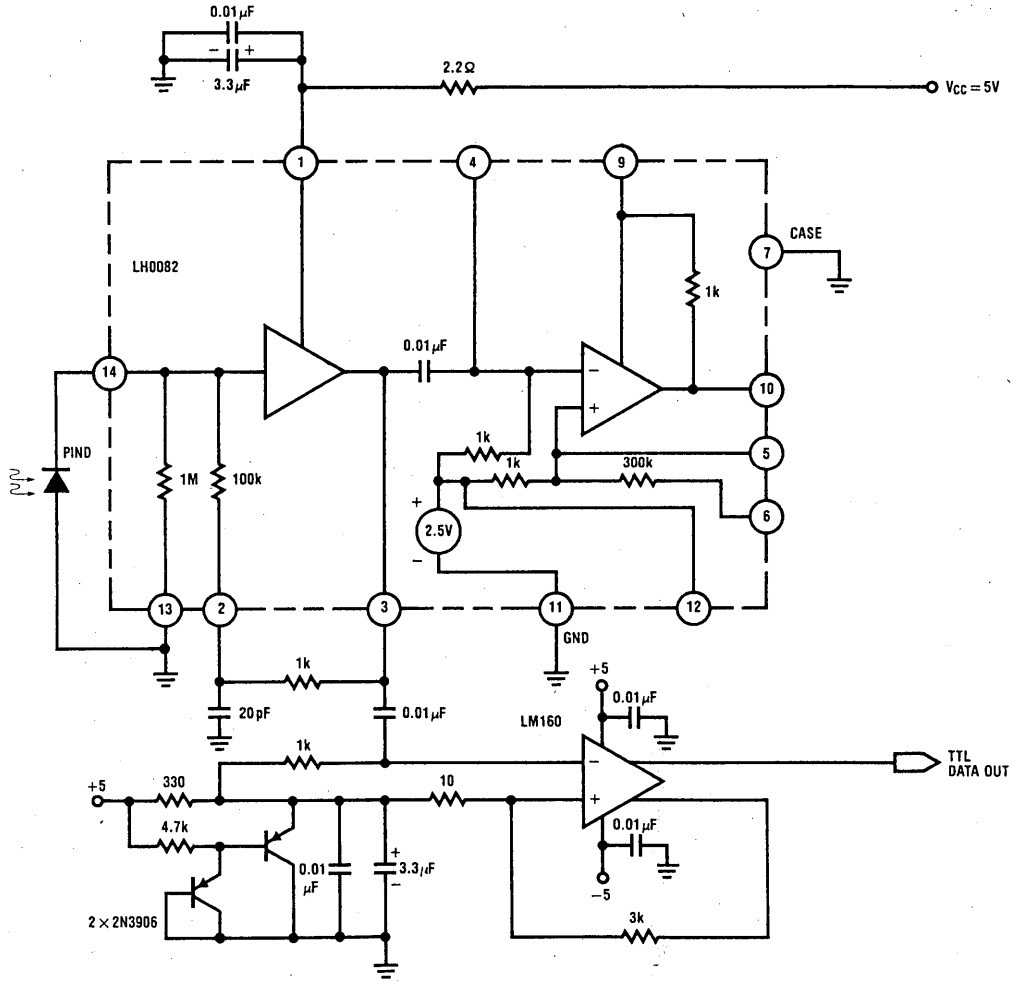


Figure 6. Fiber-Optic Receiver, Very High Sensitivity—Low Speed: 3nW



NOTE: FOR ANALOG OPERATION, USE THE CIRCUIT SHOWN IN FIGURE 7 WITH THE FOLLOWING MODIFICATIONS: DISCONNECT PIN 9 FROM V_{CC}, AND USE PIN 3 AS THE OUTPUT. BANDWIDTH FOR THIS CONFIGURATION IS APPROXIMATELY 20MHz. ANALOG RESPONSIVITY IS 50mV/μW. DYNAMIC RANGE IS 80dB.

Figure 7. 300nW Sensitivity



Speed vs Power Input for Circuit of Figure 8

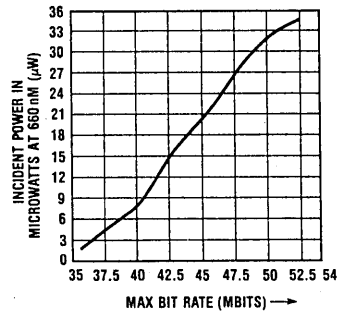


Figure 8. High Speed — Low Sensitivity Receiver

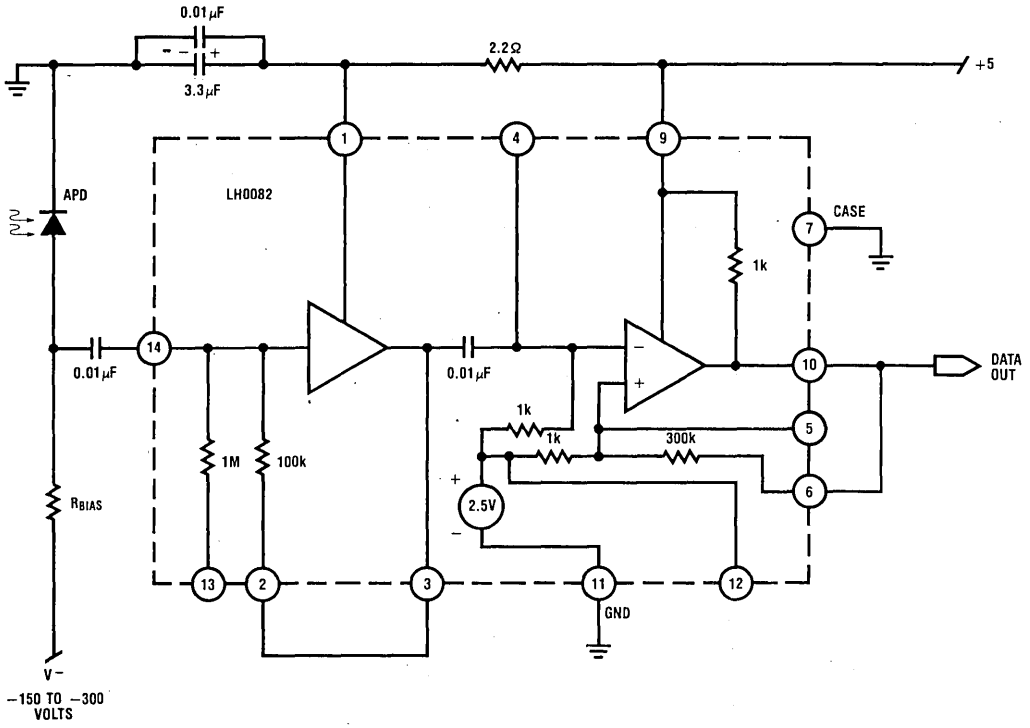


Figure 9. Connection to Avalanche Photodiode

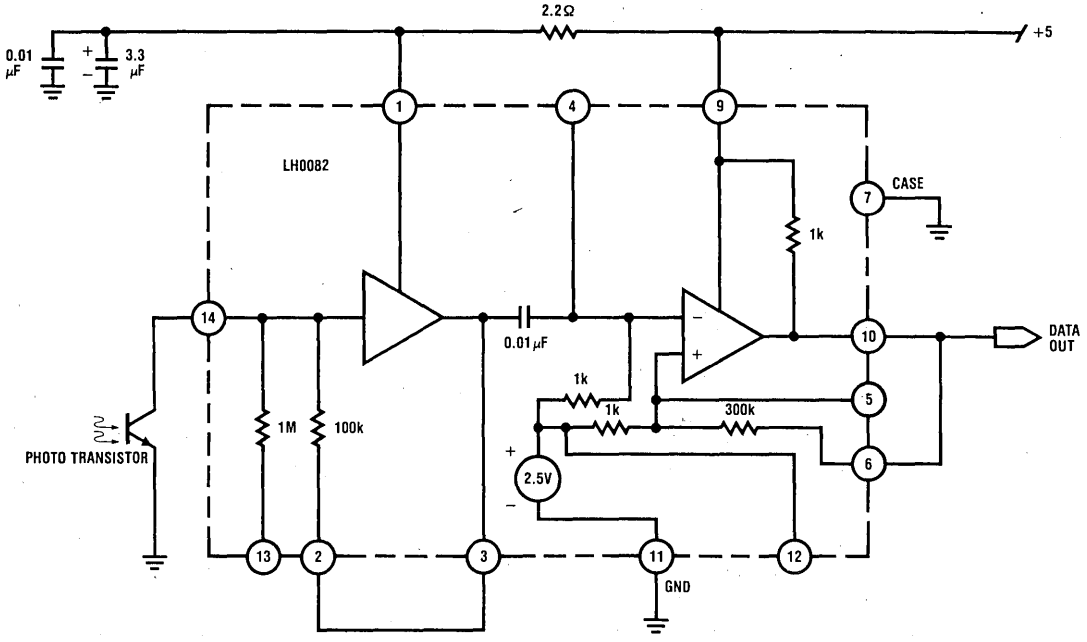


Figure 10. Connection to Phototransistor — High Sensitivity, Low Speed

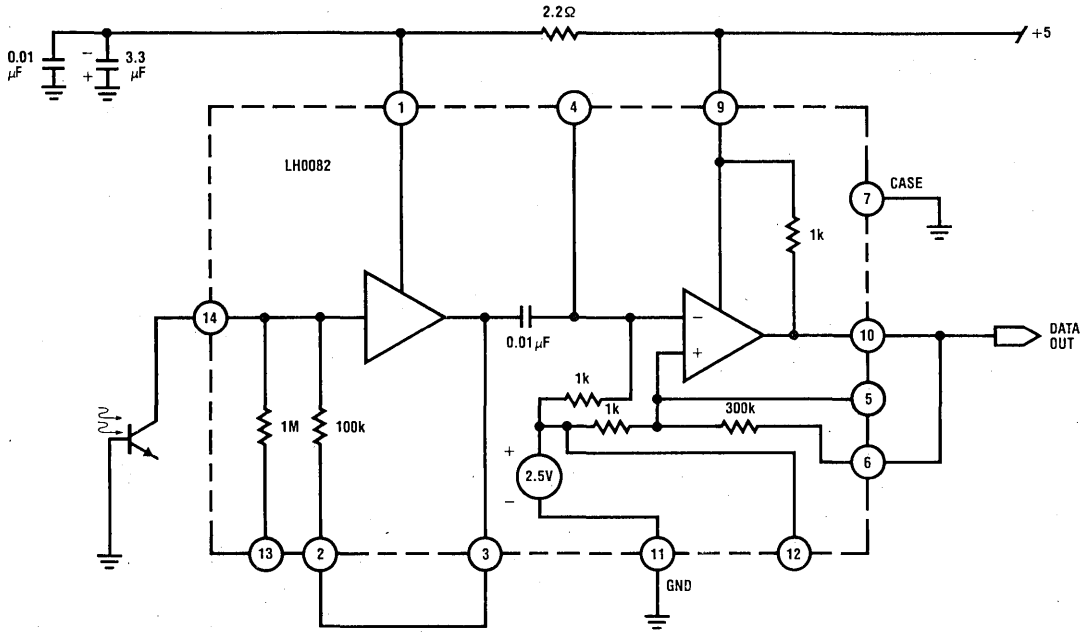


Figure 11. Connection to Phototransistor — Low Sensitivity, High Speed Receiver

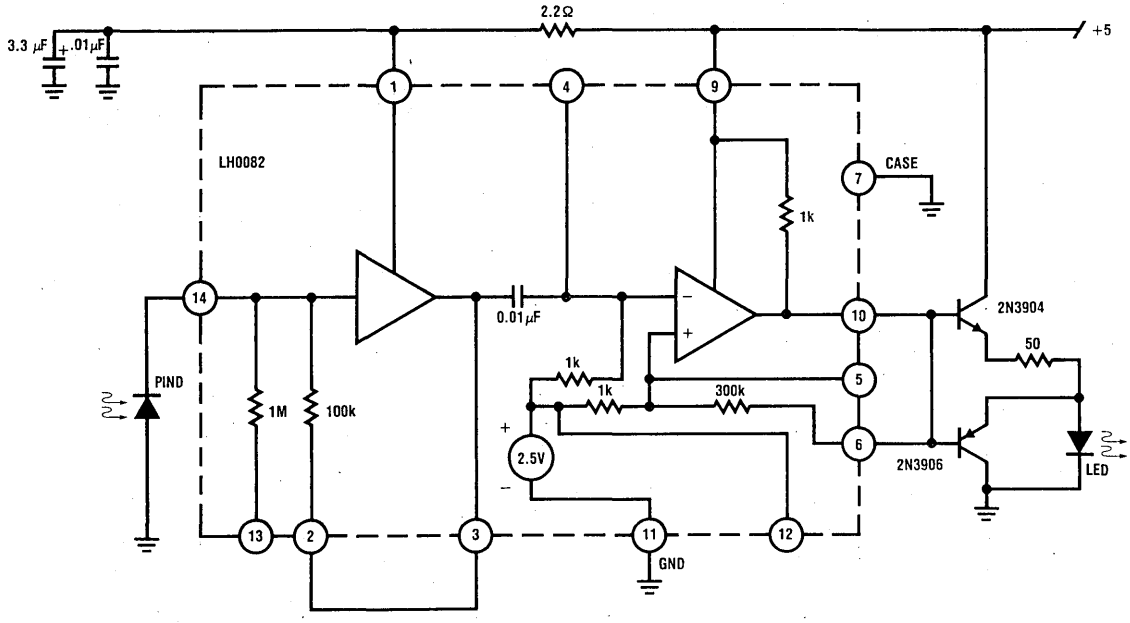


Figure 12. Fiber-Optic Link Repeater

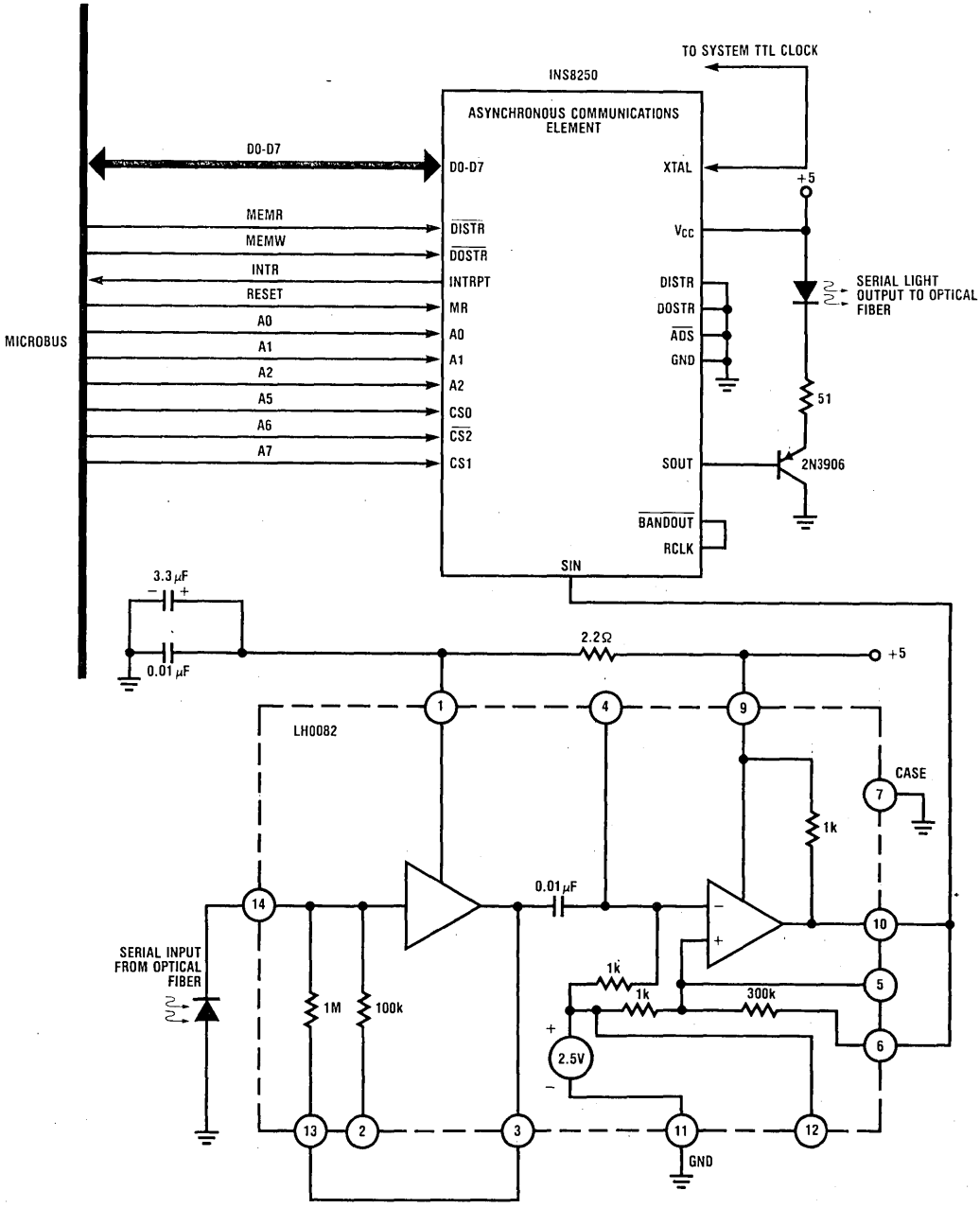


Figure 13. Optical Link to Microbus

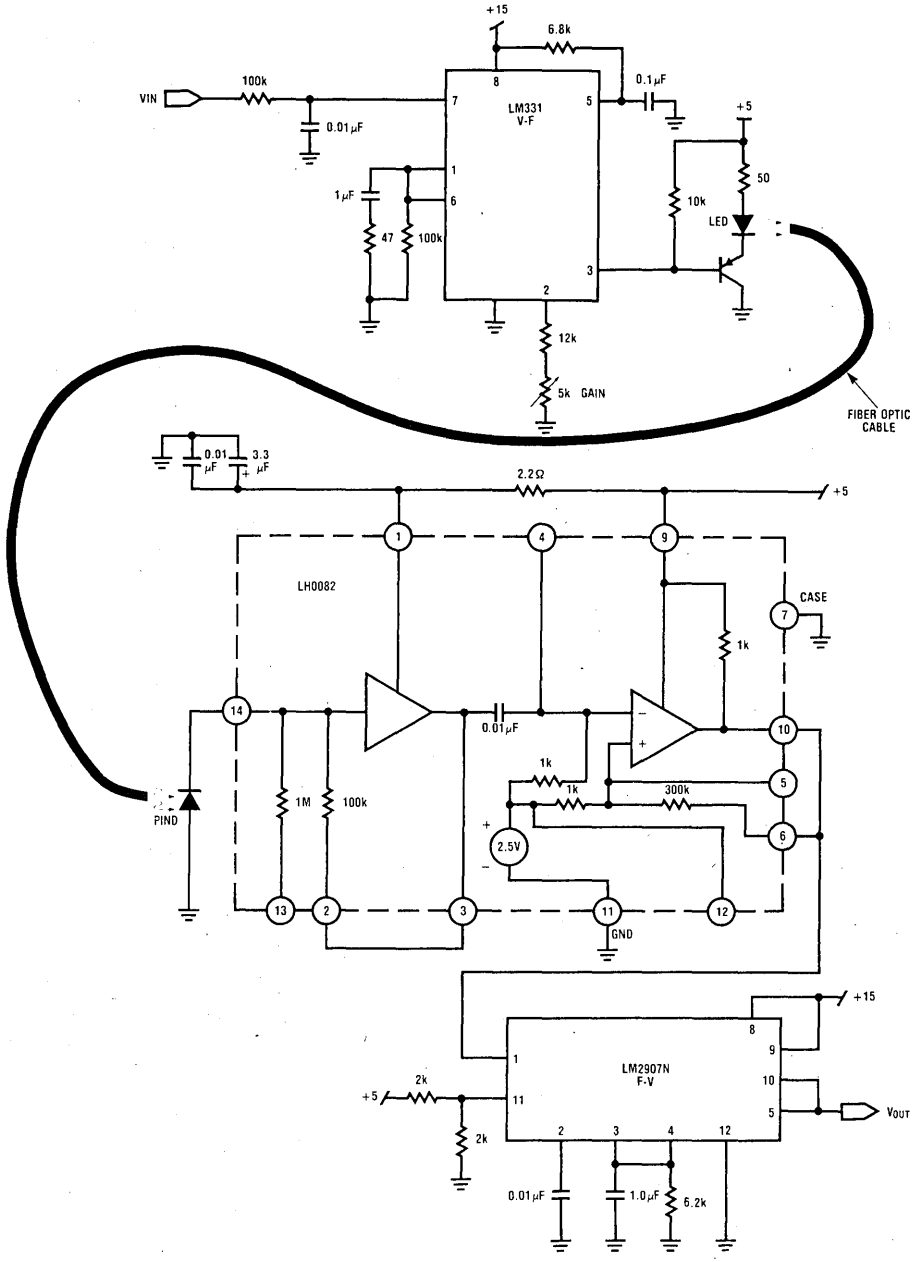


Figure 14. Analog Data Link Using V/F and F/V

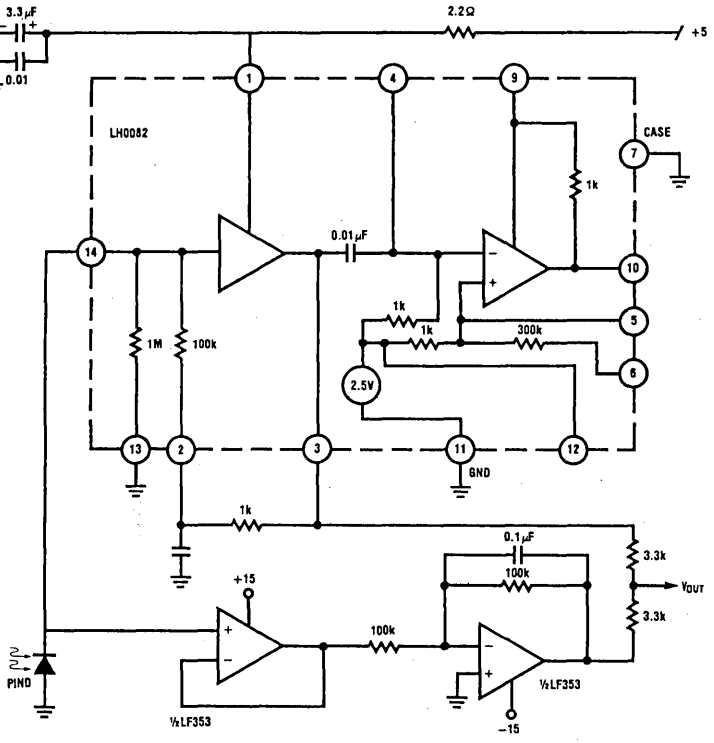


Figure 15. Low Temperature Drift Analog Receiver,

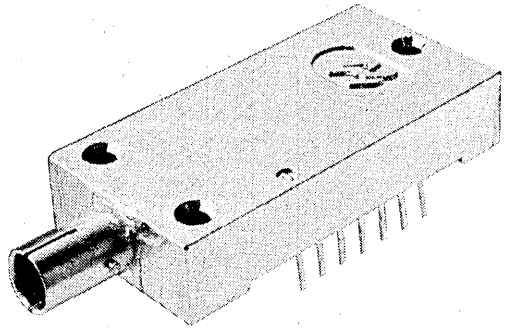
National Semiconductor

ADVANCE INFORMATION

FOR100B Fiber-Optic Receiver

General Description

The FOR100B is a general-purpose fiber-optic receiver. It contains a low-capacitance pin photodiode, FET-input transimpedance preamplifier and a comparator with hysteresis. An integral self-aligning bayonet-style connector simplifies and ensures reliable optical coupling. The low profile metal package is ideal for direct PC board mounting with 0.5" board-to-board spacing. When used with the FOT180B fiber-optic transmitter, the pair will provide a complete fiber-optic data link capable of 5 Mbits/s NRZ data rate with only 2 μW peak optical power input at the receiver. Connectors are available from Amphenol™.



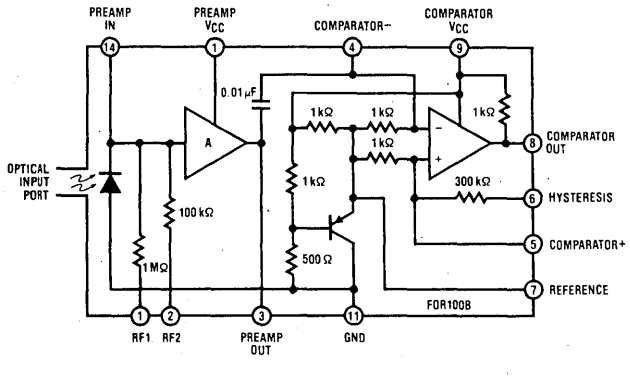
Features

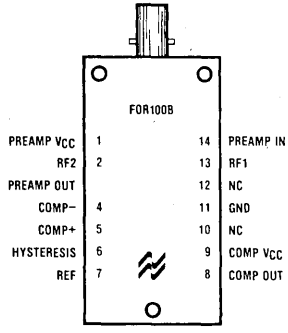
- Single 4.5V to 12V supply
- DC to 5 Mbits/s NRZ data bandwidth
- $<10^{-9}$ bit error rate
- Low capacitance silicon pin photodiode
- Pin selectable sensitivity
- CMOS/TTL compatible logic output
- >21 dB dynamic range (see Note 1, page 2)
- Quickly demountable bayonet-type Amphenol connector
- Separate analog and digital outputs
- 14-pin low-profile (0.3") package for direct PC board mounting

Applications

- Data communication networks
- Secure communications
- Peripheral control/communications
- Video transmission
- Optical modems
- Fiber-optic repeater
- Industrial machine control

Schematic and Connection Diagrams





TOP VIEW
(The 3 mounting holes are tapped for 4—40 screws)

Order Number FOR100B
See NS Package F014A

Amphenol is a trademark of Amphenol Division, Bunker Ramo Corp.

Absolute Maximum Ratings

V_{CC}	Supply Voltage	+15V
T_{STG}	Storage Temperature	−25°C to +85°C
T_A	Operating Temperature Range	−25°C to +85°C
	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical and Optical Characteristics $V_{CC} = +5V$, $T_A = 25°C$

Parameter		Conditions		Typ.	Units
	Preamp Responsivity	$R_F = 1M\Omega$,	$\lambda = 660nm$	430	mV/μW
			$\lambda = 820nm$	600	
		$R_F = 100k\Omega$,	$\lambda = 660nm$	43	
			$\lambda = 820nm$	60	
BW	Data Rate (NRZ)	$R_F = 1M\Omega$, See Fig. 1	$P_{IN} = 350nW$ Peak	1.0	Mbits/s
		$R_F = 100k\Omega$, See Fig. 2	$P_{IN} = 2\mu W$ Peak	5.0	
	Optical Port Diameter			500	μm
NA	Numerical Aperture			0.5	
V_Q	Preamp Quiescent Voltage	No Optical Input		2.1	V
V_{OL}	Comparator Output Low Voltage	$I_{OL} = 3.2mA$		0.3	
V_{OH}	Comparator Output High Voltage	$I_{OH} = -1mA$		4.0	
I_{CC}	Supply Current	Comparator Output High		30	mA
		Comparator Output Low		35	
t_{pd}	Propagation Delay:				ns
	Optical Input to Analog Output	At Pin 3,	$R_F = 100k\Omega$	40	
	Optical Input to TTL Output	At Pin 6		150	

Note 1: With the circuit configuration in Figure 2, the minimum detectable input and maximum allowable inputs are 300nW and 41μW peak respectively, this translates to >21dB dynamic range. This is based on a photodiode responsivity of 0.60A/W @ $\lambda = 820nm$.

Applications Information

The front end of the FOR100B fiber-optic receiver is a wideband transimpedance amplifier, thus good supply bypassing is required. A 3.3μF tantalum capacitor in parallel with a 0.1μF ceramic disc placed as close as possible to device pins is recommended. Also, the metal case should be grounded. The mounting holes are tapped for 4—40 screws.

The FOR100B contains all the components required to function as an optical in/TTL out receiver. No external components are required if the basic receiver configurations are used.

Figure 1 shows the high sensitivity configuration capable of 1Mbit/s NRZ data rate with only 350nW of peak optical power input. Figure 2 shows the low sensitivity circuit capable of 5Mbits/s NRZ operation with only 2μW of optical input.

In applications where external components are required, it is important that the following techniques be considered:

- Make overall layout compact.
- Keep all component lead lengths as short as possible.
- Route the comparator output away from the preamp and comparator inputs.
- Separate preamp input and comparator output lead by a ground or supply trace where possible.

Applications Circuits

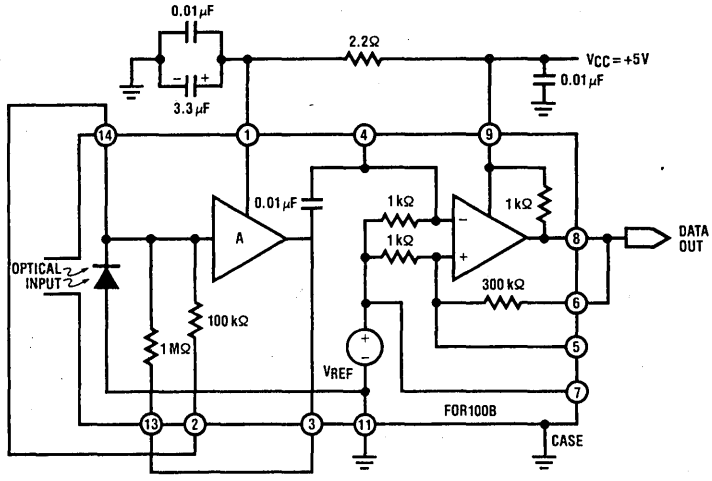


Figure 1. Fiber-Optic Receiver—High Sensitivity: 30nW

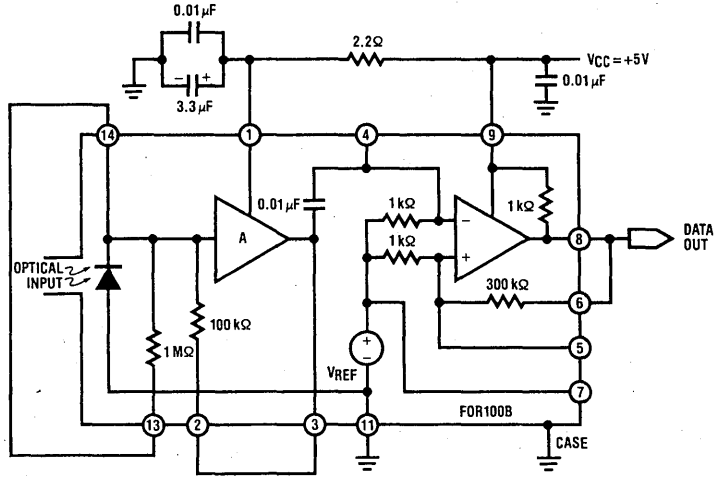


Figure 2. Fiber-Optic Receiver—Low Sensitivity: 300nW

Ordering Information

Bayonet Connector	Part No.	Fiber Diameter
	905-143-5001	125 microns
	905-143-5002	140 microns
	905-143-5003	200 microns
	905-143-5004	230 microns
	905-143-5005	400 microns
	905-143-5006	600 microns
Order from Amphenol Division, Bunker Ramo Corp., Denbury, Connecticut	905-143-5007	1 millimeter

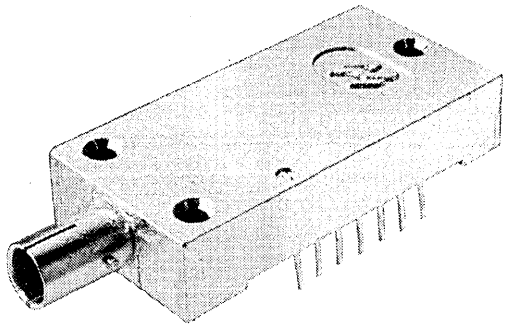
National Semiconductor

ADVANCE INFORMATION

FOT180B Fiber-Optic Transmitter

General Description

The FOT180B is a high-speed general-purpose electro-optical transmitter. It is designed for digital data transmission via optical fibers with data rates up to 20 MBits/s NRZ. The package includes the driver circuitry, optical light source, and connector. The bayonet-type connector on the package simplifies and ensures reliable optical coupling with minimal source to fiber alignment losses. The low-profile metal package is ideal for direct PC board mounting with 0.5″ board-to-board spacing. When used with the FOR100B fiber-optic receiver, the pair provides a complete optical data link with TTL compatible interfacing. Connectors are available from Amphenol™.



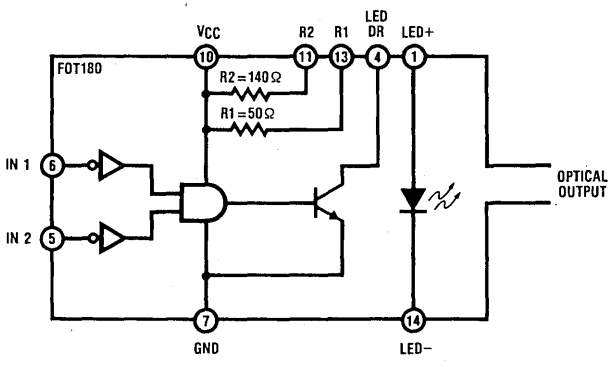
Features

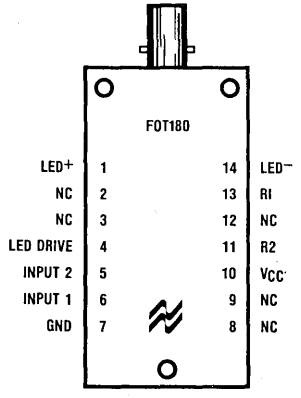
- Single +5 V supply
- DC to 20 Mbits/s NRZ data rate
- Pin selectable optical output power
- LED built-in
- CMOS/TTL compatibility
- Data and enable inputs
- Quickly demountable bayonet-type Amphenol optical connector
- 14-pin low profile package (0.3″) for direct PC board mounting
- Open collector output driver

Applications

- Data communication networks
- Secure communications
- Peripheral control/communication
- Industrial machine control
- T1 and T2 telecom digital links
- Optical modems
- Video transmission

Schematic and Connection Diagram





TOP VIEW
(The 3 mounting holes are tapped for 4—40 screws)

Order Number FOT180B
See NS Package FO14A

Amphenol is a trademark of Amphenol Division, Bunker Ramo Corp. See Page 13.25 for part number.

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Absolute Maximum Ratings

V_{CC}	Supply Voltage	7V
V_{IN}	Input Voltage	5.5V
I_{IN}	Input Current	−30 mA to +5 mA
I_F	LED Forward Current, DC	100 mA
T_A	Operating Temperature	−25°C to +85°C
T_{STG}	Storage Temperature	−25°C to +85°C
	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A = +25°C$.

Driver Specifications

Parameter		Conditions			Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	$V_{CC} = 4.5V$, $V_{IN} = 0.8V$ (see Figure 1)		$I_{OL} = 40$ mA			0.5	V
				$I_{OL} = 70$ mA			0.7	
				$I_{OL} = 100$ mA			0.8	
V_{IH}	Input High Voltage	$V_{CC} = 4.5V$	Guaranteed input logic high for all inputs		2			
V_{IL}	Input Low Voltage		Guaranteed input logic low for all inputs				0.8	
I_{IH}	Input High Current	$V_{CC} = 5.5V$	$V_{IN} = 2.7V$	Input 1			30	μA
				Input 2			20	
I_{IL}	Input Low Current		$V_{IN} = 0.4V$	Input 1			−0.54	mA
				Input 2			−0.36	
I_{CC}	Supply Current			Input 2 = 0V			80	
R_1	Resistance				47.5	50	52.5	Ω
R_2	Resistance				133	140	147	

DC LED Specifications

Parameter		Conditions	Min.	Typ.	Max.	Unit
V_F	Forward Voltage	$I_F = 50$ mA		1.3		V
BV_R	Reverse Breakdown Voltage	$I_R = 100$ μA		5		
λ_{PK}	Peak Emission Wavelength	$I_F = 50$ mA		820		nm

Electrical Characteristics (Continued)

Transmitter Specifications Conditions: $V_{CC} = 5V$, $T_A = 25°C$.

Parameter		Conditions		Fiber Core Diameter	Min.	Typ.	Max.	Unit
P_O	Optical Power Output	(Notes 1 & 2) 100% Duty Cycle	Current limiting resistor = R1	200 μm, 0.4 NA		22		μW
				400 μm, 0.5 NA		110		
			Current limiting resistor = R2	200 μm, 0.4 NA		9		
				400 μm, 0.5 NA		45		
I_F	LED Current	Current limiting resistor = R1 (see Figure 2)				70		mA
		Current limiting resistor = R2 (see Figure 3)				26		
	Data Rate (NRZ)					20		Mb/s
	Optical Port (Fiber Core Diameter)					500		μm
NA	Exit Numerical Aperture					0.5		
t_r	Optical Rise Time	See Figure 2				15		ns
t_f	Optical Fall Time	See Figure 2				15		
t_{pd}	Propagation Delay: Electrical Input to Optical Output	See Figure 2				10		

Note 1: Optical power output (DC) is measured at the end of a one-meter long fiber using an EG & G Model 550 photometer that has been calibrated at 820 nm.

Note 2: The 200 μm fiber used is DuPont S120 Type 30; the 400 μm fiber used is DuPont PIFAX PIR140.

Applications Information

The FOT180B is a hybrid fiber-optic transmitter circuit. It includes the driver circuitry, LED, and two current-limiting resistors. The circuit layout allows the user to have access to the LED drive output pin, the two scaling resistors, and the LED. Access to both the anode and the cathode of the LED allows the user to implement various drive configurations to optimize system performance. Figure 4 shows the FOT180B set up in a series drive scheme using the internal 50 Ω resistor. The drive current can be calculated using the following equation:

$$I_D = \frac{V_{CC} - V_F - V_{OL}}{R}$$

where: I_D = LED drive current
V_{CC} = Supply voltage
V_F = ON-voltage of the LED
V_{OL} = LO-voltage of the open collector output
R = Current-limiting resistor

When input 2 is at logic "0", the LED ON/OFF condition is entirely controlled by input 1 at pin 6. This configuration allows the driver to control the LED and at the same time provide the necessary logic signal levels to interface with other TTL circuits. Also, series drive configurations tend to lower the power consumption in the LED driver. A characteristic of this method is a large current supply step when the LED turns ON and OFF (20 mA to 60 mA depending on the value of the current-limiting resistor). Figures 2 and 3 show the FOT180B set up in a different configuration. The LED is shunted across the drive output transistor instead of in series with it. In this shunt-driven mode the LED drive current is:

$$I_D = \frac{V_{CC} - V_F}{R}$$

where: I_D = LED drive current
V_F = ON-voltage of the LED
R = Current-limiting resistor

The step in supply current due to output switching is much smaller with this method, so the shunt drive configuration has a relatively constant supply current drain and less power supply line modulation.

DC Test Circuit

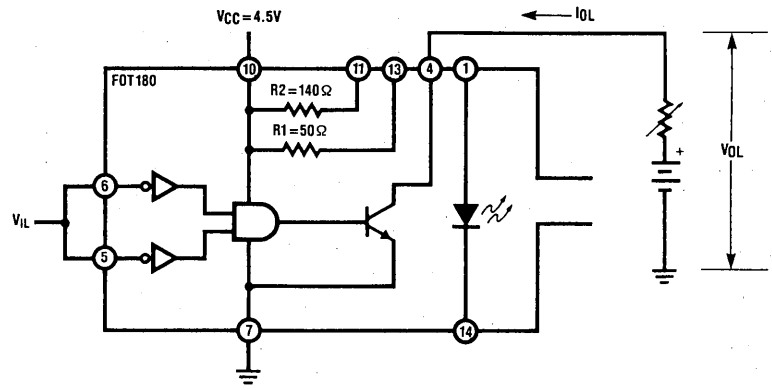
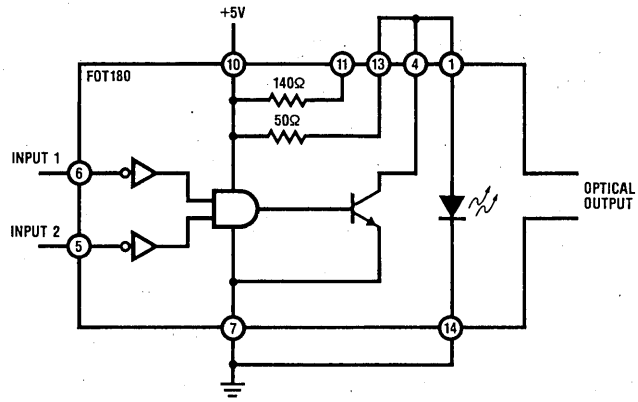


Figure 1. V_{IL}, V_{OL}

Typical Applications



Input 1	Input 2	Optical
0	0	OFF
0	1	ON
1	0	OFF
1	1	OFF

Figure 2. High Current, Shunt Drive

Typical Applications continued

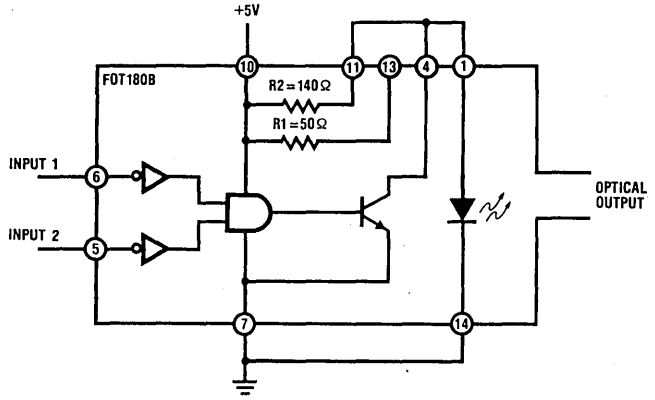
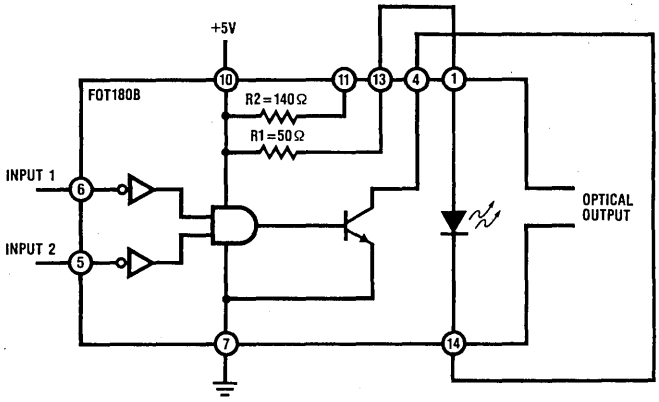


Figure 3. Low Current, Shunt Drive



Input 1	Input 2	Optical
0	0	ON
0	1	OFF
1	0	OFF
1	1	OFF

Figure 4. High Current, Series Drive

Ordering Information

Bayonet Connector	Part No.	Fiber Diameter
	905-143-5001	125 microns
	905-143-5002	140 microns
	905-143-5003	200 microns
	905-143-5004	230 microns
	905-143-5005	400 microns
	905-143-5006	600 microns
Order from Amphenol Division, Bunker Ramo Corp., Denbury, Connecticut	905-143-5007	1 millimeter

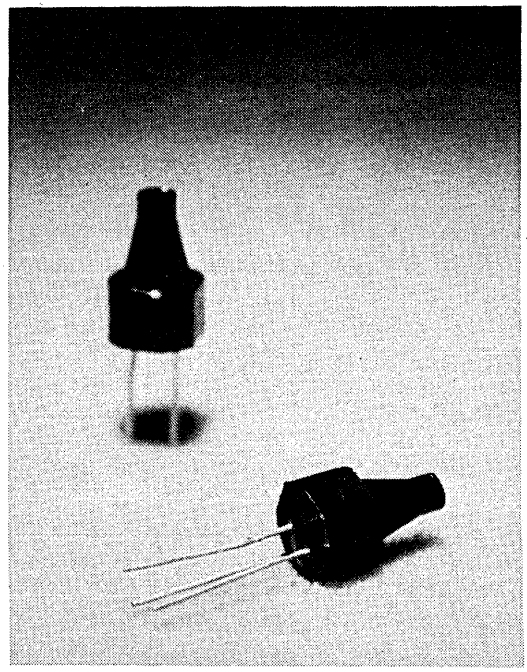
National Semiconductor

ADVANCE INFORMATION

FOR261F Monolithic TTL Fiber-Optic Receiver

General Description

The FOR261F is a high speed monolithic fiber-optic receiver accepting optical input and providing TTL outputs at NRZ data rates to 10 Mbits/s with only 7 μW of optical power. It is available in a short ferrule package which is compatible with Amphenol™ and AMP™ standard receptacles.



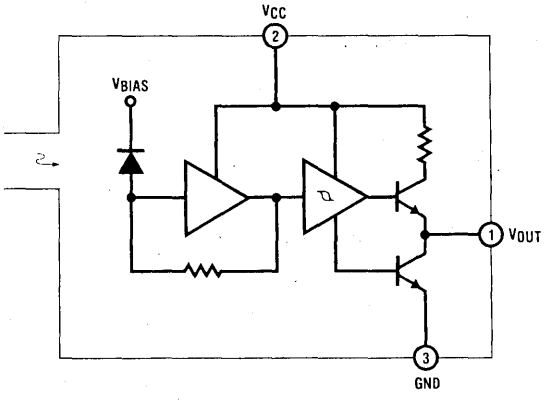
Features

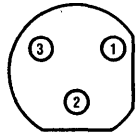
- Single +5V supply
- Optical input, TTL output
- 10 Mbits/s NRZ data rate with only 7 μW of peak optical power
- $<10^{-9}$ bit error rate
- Short ferrule package with 250 μm diameter optical port
- Compatible with AMP #227240-1 and Amphenol #905-135-5000 connectors
- Temperature compensated input

Applications

- Data communications
- Optical modem
- Industrial machine control
- Peripheral control/communications

Equivalent Circuit





Bottom View

Order Number FOR261F
See NS Package FO-03A

AMP is a trademark of AMP Corp.
Amphenol is a trademark of Bunker Ramo Corp.

Absolute Maximum Ratings

V_{CC}	Supply Voltage	+7V
P_{IN}	Optical Power Input	350 μW peak
T_{STG}	Storage Temperature	−25°C to +85°C
T_A	Operating Temperature Range	−25°C to +85°C
	Lead Temperature (Soldering, 10 seconds)	300°C

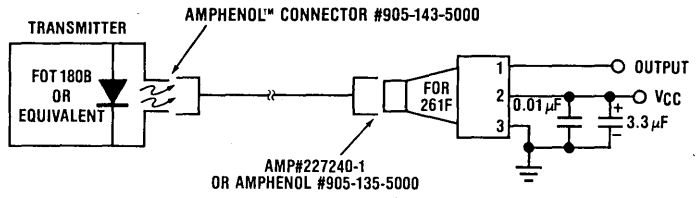
Electrical and Optical Characteristics $V_{CC} = +5V$, $T_A = 25°C$, $\lambda = 820nm$

Parameter		Conditions	Typ.	Units
I_{CC}	Supply Current Output High Output Low	$V_{CC} = 5.5V$	 12 16	mA
V_{OL}	Output Low Voltage	$P_{IN} = 7\mu W$, $I_{OL} = 16mA$	0.5	V
V_{OH}	Output High Voltage	$P_{IN} = 0\mu W$, $I_{OH} = -400\mu A$	2.7	V
BW	Data Rate (NRZ)	$P_{IN} = 7\mu W$, BER$<10^{-10}$	10	Mbits/s
NA	Numerical Aperture		0.5	
	Fiber Core Diameter		400	μm
NEP	Noise Equivalent Power	10 Hz to 10 MHz	14	nW
t_r	Output Rise Time	$P_{IN} = 7\mu W$, pk	40	ns
t_f	Output Fall Time	$P_{IN} = 7\mu W$ pk	40	ns
t_{pd}	Propagation Delay: Optical Input to TTL Output	$P_{IN} = 7\mu W$ pk	80	ns

Applications Information

The FOR261F is a monolithic fiber-optic receiver. It accepts optical input and gives TTL output. Figure 1 shows a typical application using the FOT180B fiber-optic transmitter as the optical source, and the FOR261F as the receiver. With 7 μW of input optical power, this configuration is capable of data rates to 10 Mbits/s NRZ.

Application Circuit



Section 14

Active Filters and Telecommunication Products

Section 14. Active Filters (Building Blocks) Selection Guide

Function	Features	Frequency Accuracy	Q Accuracy	$Q \times F_C$	Part Number −55°C to 125°C	Part Number −25°C to 85°	Page Number
Universal Active Filter	State Variable Building Block	±2.5%	±7.5%	50k	AF100-1	AF100-1C	14-5
		±1.0%	±7.5%	50k	AF100-2	AF100-2C	14-5
Universal Active Filter	State Variable Building Block Wide Bandwidth	±2.5%	±7.5%	200k		AF150-1C	14-53
		±1.0%	±7.5%	200k		AF150-2C	14-53
Dual Universal Active Filter	State Variable Building Block Two AF100 in one package	±2.5%	±7.5%	50k		AF151-1C	14-73
		±1.0%	±7.5%	50k		AF151-2C	14-73
Universal Wideband	FET-Input Amplifier Pin Compatible with AF100J	±2.5%	±7.5%	200k	AF160-1	AF160-1C	14-81
		±1.0%	±7.5%	200k	AF160-2	AF160-2C	14-81
Dual Universal Wideband	FET-Input Amplifier Pin Compatible with AF151J	±2.5%	±7.5%	200k		AF161-1C	14-100
		±1.0%	±7.5%	200k		AF161-2C	14-100
		Resistor Accuracy	**Resistor Match**	**Resistor Tempco (ppm/°C)**			
General Impedance Converter (GIC)	Matched Resistors 7.5k and Controlled TC	1.0%	±0.2%/ 0.1%	±110 ±30	AF120H		14-32
		2.0%	±0.4%/ 0.2%	±110 ±60		AF120CH	14-32

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Section 14. Tuned Active Filters Selection Guide

Function	Features	Cutoff/ Band Edge Freq. (Hz)	Passband Ripple (dB)	Stopband Frequency (Hz)	Stopband Attenuation (dB)	Gain Tolerance (dB)	Part Number	Page Number
Touch Tone* Filters for Dual Tone Multifrequency Receivers (DTMF)	High Band Splitter Filter	1209	±0.5	941	25	±0.5 @ 1336 Hz	AF101CJ	14-82
	Dial Tone Reject Filter	697	±0.5	440	34	±0.5 @ 941 Hz	AF102CJ	14-84
	Low Band Splitter Filter	941	±0.5	1209	25	±0.5 @ 852 Hz	AF103CJ	14-86
Addition Tone Receiver Circuits	Automatic Gain Control (AGC)						AF104 AF105	14-108 14-108
Pulse Code Modulation (PCM) Filters 8 kHz Sampling Rate	Transmit/Receive PCM	3000	±0.5	5300	20	±0.5	AF132CJ	14-108
	Filter for 8 kHz Sampling (sin x)/x Correction	3000	±0.5	4900	20	±0.5		
	5th Order Low Pass Filter	3000	±0.3	4600	30	External	AF133-1CJ	14-98
	Transmit PCM Filter	3000	±0.125	4600	32	Resistor	AF133-2C	14-98
	5th Order Low Pass Filter	3000	±0.3	4600	30	±1.0 @ 1.0 kHz	AF134-1CJ	14-98
	Receive PCM Filter	3000	±0.125	4600	32	±0.5 @ 1.0 kHz	AF134-2CJ	14-98
		Center Freq. (Hz)						
Signalling Tone Filters	2000 Hz Band Reject Filter	2600	±0.2/±0.5	2585/2615	30	@±0.5	AF138**	
	2600 Hz Baud Pass Filter			(2400-2800)	30	−1.25/+1.75	AF139**	
		2600	3	(2100-3100)	50	@2600 Hz		
				>1600	70			
Bandpass Filters for DTMF Detectors	Compatible with Rockwell CRC8030 and Mostek MK5102	697-950	±2dB	500/1200	30	±1.5	AF121-1CJ	14-40
					40	±0.5	AF121-2CJ	
		1209-1633		2200/950	30	±1.5	AF122-1CJ	14-40
					40	±0.5	AF122-2CJ	

*Registered trademark of Western Electric Co.

**The AF138 and AF139 are not available at the time of this printing. Contact sales office for information.

AF100 Universal Active Filter

General Description

The AF100 state variable active filter is a general second order lumped RC network. Only four external resistors program the AF100 for specific second order functions. Lowpass, highpass, and bandpass functions are available simultaneously at separate outputs. Notch and allpass functions are available by summing the outputs in the uncommitted output summing amplifier. Higher order systems are realized by cascading AF100 active filters with appropriate programming resistors.

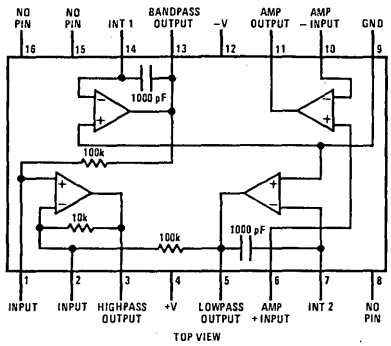
Any of the classical filter configurations, such as Butterworth, Bessel, Cauer, and Chebyshev can be formed.

Features

- Military or commercial specifications
- Independent Q, frequency, gain adjustments
- Low sensitivity to external component variation
- Separate lowpass, highpass, bandpass outputs
- Inputs may be differential, inverting, or non-inverting
- Allpass and notch outputs may be formed using uncommitted amplifier
- Operates to 10 kHz
- Q range to 500
- Power supply range ±5V to ±18V
- Frequency accuracy ±1% unadjusted
- Q frequency product $\leq$ 50,000

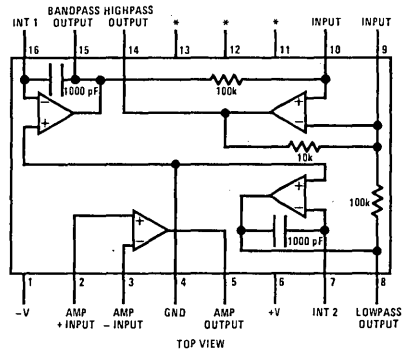
Connection Diagrams

Ceramic Dual-In-Line Package
AF100-1CJ, AF100-2CJ
NS Package Number HY13A



TOP VIEW

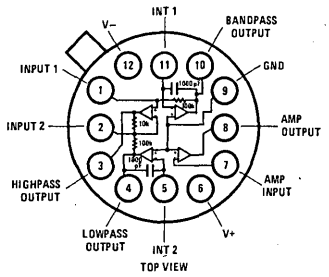
Plastic Dual-In-Line Package
AF100-1CN, AF100-2CN
NS Package Number N16A



TOP VIEW

*Note: Internally connected. Do not use.

Metal Can Package
AF100-1CG, AF100-1G, AF100-2CG, AF100-2G
NS Package Number H12B



TOP VIEW

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation	900 mW/Package (500 mW/Amp)
Differential Input Voltage	±36V
Output Short Circuit Duration (Note 1)	Infinite
Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature	
AF100-1CJ, AF100-2CJ, AF100-1CG, AF100-2CG, AF100-1CN, AF100-2CN	−25°C to +85°C
AF100-1G, AF100-2G	−55°C to +125°C
Storage Temperature	
AF100-1G, AF100-2G	−65°C to +125°C
AF100-1CG, AF100-2CG, AF100-1CJ, AF100-2CJ, AF100-1CN, AF100-2CN	−25°C to +100°C

Electrical Characteristics (Complete Active Filter) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_C \times Q \leq 50{,}000$			10k	Hz
Q Range	$f_C \times Q \leq 50{,}000$			500	Hz/Hz
f_O Accuracy					
AF100-1, AF100-1C	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±2.5	%
AF100-2, AF100-2C	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±1.0	%
f_O Temperature Coefficient			±50	±150	ppm/°C
Q Accuracy	$f_C \times Q \leq 10{,}000$, $T_A = 25°C$			±7.5	%
Q Temperature Coefficient			±300	±750	ppm/°C
Power Supply Current	$V_S = ±15V$		2.5	4.5	mA

Electrical Characteristics (Internal Op Amp) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	6.0	mV
Input Offset Current			4	50	nA
Input Bias Current			30	200	nA
Input Resistance			2.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2k$, $V_{OUT} = ±10V$	25	160		V/mV
Output Voltage Swing	$R_L = 10\ k\Omega$	±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range		±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		dB
Output Short Circuit Current			25		mA
Slew Rate (Unity Gain)			0.6		V/μs
Small Signal Bandwidth			1		MHz
Phase Margin			60		Degrees

Note 1: Any of the amplifiers can be shorted to ground indefinitely, however more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: Specifications apply for $V_S = ±15V$, over −25°C to +85°C for the AF100-1C and AF100-2C and over −55°C to +125°C for the AF100-1 and AF100-2, unless otherwise specified.

Note 3: Specifications apply for $V_S = ±15V$, $T_A = 25°C$.

Applications Information

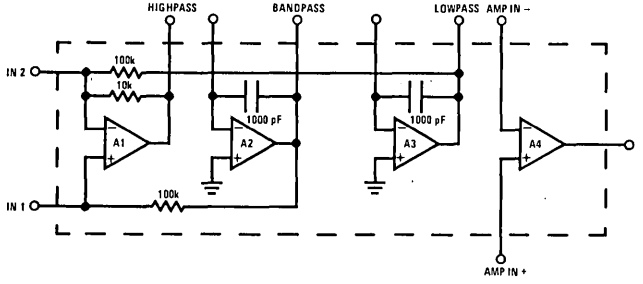


FIGURE 1. AF100 Schematic

CIRCUIT DESCRIPTION AND OPERATION

A schematic of the AF100 is shown in *Figure 1.* Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input. Amplifier A4 is an uncommitted amplifier.

By adding external resistors the circuit can be used to generate the second order system

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_0 = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_0}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(highpass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer function becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(bandpass)}$$

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(lowpass)}$$

Using proper input and output connections the circuit can also be used to generate the transfer functions for a notch and allpass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals 1, and a_3 equals ω_Z^2. The transfer function becomes:

$$T(s) = \frac{s^2 + \omega_Z^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(notch)}$$

In the allpass transfer function $a_1 = 1$, $a_2 = -\omega_0/Q$ and $a_3 = \omega_0^2$. The transfer function becomes:

$$T(s) = \frac{s^2 - \frac{\omega_0}{Q} s + \omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(allpass)}$$

COMMON CONFIGURATIONS

The specific transfer functions for some of the most useful circuit configurations using the AF100 are illustrated in *Figures 2 through 8.* Also included are the gain equations for each transfer function in the frequency band of interest, the Q equation, center frequency equation and the Q determining resistor equation.

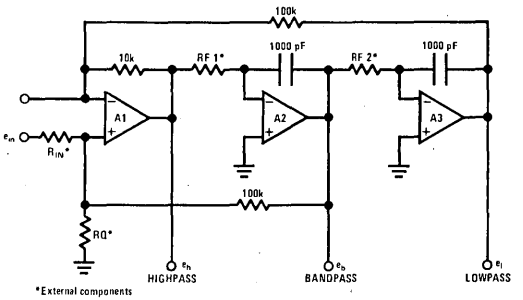


FIGURE 2. Non-inverting Input (Q > Q_{MIN}, See Q Tuning Section)

Applications Information (Continued)

a) Non-inverting input *(Figure 2)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left[\dfrac{1.1}{1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left[\dfrac{1.1}{1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2\left[\dfrac{1.1}{1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\left[\frac{1.1}{1+\dfrac{10^5}{RQ}+\dfrac{10^5}{R_{IN}}}\right]\omega_1 + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{11}{\left(1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}\right)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = \frac{1.1}{\left(1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}\right)}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{\left(1+\dfrac{10^5}{RQ}+\dfrac{10^5}{R_{IN}}\right)}{\left(1+\dfrac{R_{IN}}{10^5}+\dfrac{R_{IN}}{RQ}\right)}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left(\frac{1+\dfrac{10^5}{R_{IN}}+\dfrac{10^5}{RQ}}{1.1}\right)\sqrt{0.1\left(\frac{\omega_2}{\omega_1}\right)}$$

$$RQ = \frac{10^5}{\left(\dfrac{1.1Q}{\sqrt{0.1\dfrac{\omega_2}{\omega_1}}}\right) - 1 - \dfrac{10^5}{R_{IN}}}$$

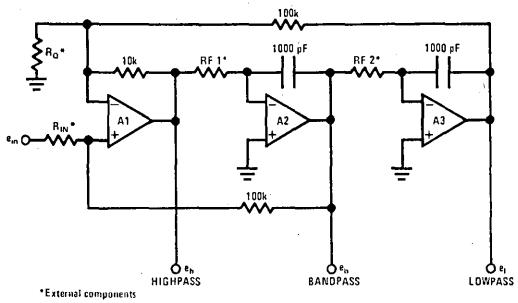


FIGURE 3. Non-Inverting Input ($Q < Q_{MIN}$, See Q Tuning Section)

b) Non-inverting input *(Figure 3)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left[\dfrac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left[\dfrac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2\left[\dfrac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1\left[\frac{1.1+\dfrac{10^4}{RQ}}{\dfrac{10^5}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{1.1+\dfrac{10^4}{RQ}}{0.1\left(1+\dfrac{R_{IN}}{10^5}\right)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = \frac{1.1+\dfrac{10^4}{RQ}}{1+\dfrac{R_{IN}}{10^5}}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{1+\dfrac{10^5}{R_{IN}}}{1+\dfrac{R_{IN}}{10^5}}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1+\dfrac{10^5}{R_{IN}}}{1.1+\dfrac{10^4}{RQ}}\right]\sqrt{0.1\frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^4}{\left(1+\dfrac{10^5}{R_{IN}}\right)\left(\dfrac{\sqrt{0.1\dfrac{\omega_2}{\omega_1}}}{Q}\right) - 1.1}$$

Applications Information (Continued)

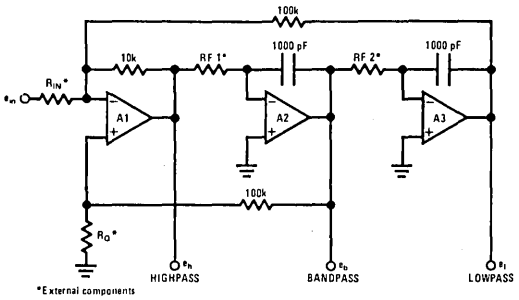


FIGURE 4. Inverting Input

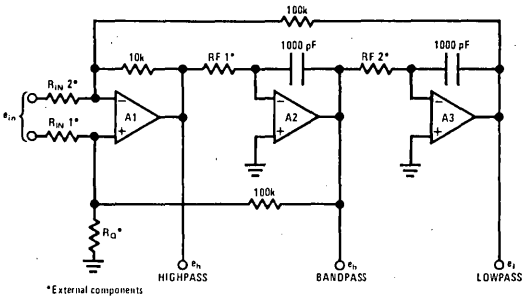


FIGURE 5. Differential Input

c) Inverting input *(Figure 4)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{-s^2 \dfrac{10^4}{R_{IN}}}{\Delta} \qquad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{s\,\omega_1 \dfrac{10^4}{R_{IN}}}{\Delta} \qquad \text{(bandpass)}$$

$$\frac{e_l}{e_{IN}} = \frac{-\omega_1\,\omega_2 \dfrac{10^4}{R_{IN}}}{\Delta} \qquad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \dfrac{10^4}{R_{IN}}}{1 + \dfrac{10^5}{R_Q}} \right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_l}{e_{IN}}\right|_{s \to 0} = -\frac{10^5}{R_{IN}} \qquad \text{(lowpass)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s \to \infty} = -\frac{10^4}{R_{IN}} \qquad \text{(highpass)}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega = \omega_0} = \frac{\dfrac{10^4}{R_{IN}}\left(1 + \dfrac{10^5}{RQ}\right)}{1.1 + \dfrac{10^4}{R_{IN}}} \qquad \text{(bandpass)}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1 + \dfrac{10^5}{RQ}}{1.1 + \dfrac{10^4}{R_{IN}}} \right] \sqrt{0.1 \frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^5}{\dfrac{Q}{\sqrt{0.1 \dfrac{\omega_2}{\omega_1}}} \left(1.1 + \dfrac{10^4}{R_{IN}}\right) - 1}$$

d) Differential input *(Figure 5)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2 \dfrac{10^4}{R_{IN2}}}{\Delta} \qquad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1 \dfrac{10^4}{R_{IN2}}}{\Delta} \qquad \text{(bandpass)}$$

$$\frac{e_l}{e_{IN}} = \frac{\omega_1\omega_2 \dfrac{10^4}{R_{IN2}}}{\Delta} \qquad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \dfrac{10^4}{R_{IN2}}}{1 + \dfrac{10^5}{RQ} + \dfrac{10^5}{R_{IN1}}} \right] + 0.1\,\omega_1\omega_2$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1 + \dfrac{10^5}{RQ} + \dfrac{10^5}{R_{IN1}}}{1.1 + \dfrac{10^4}{R_{IN2}}} \right] \sqrt{0.1 \frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^5}{\dfrac{Q}{\sqrt{0.1 \dfrac{\omega_2}{\omega_1}}} \left(1.1 + \dfrac{10^4}{R_{IN2}}\right) - 1 - \dfrac{10^5}{R_{IN1}}}$$

Applications Information (Continued)

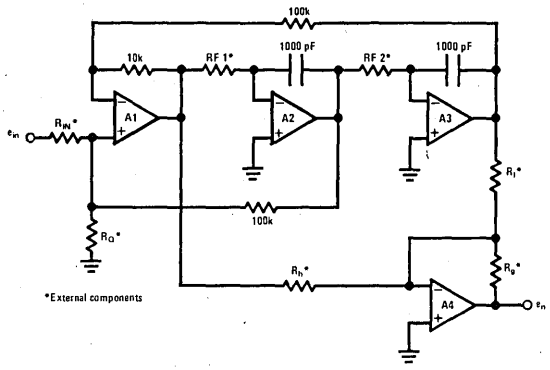


FIGURE 6. Output Notch Using All Four Amplifiers

e) Output notch *(Figure 6)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = \frac{(s^2 + \omega_Z{}^2)\left[\frac{1.1}{1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}}\right]\frac{R_g}{R_h}}{s^2 + s\,\omega_1\left[\frac{1.1}{1 + \frac{10^5}{RQ} + \frac{10^5}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}} \qquad \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\omega_Z = \omega_0\sqrt{\frac{10\,R_h}{R_\ell}}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to 0} = \frac{11}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}\right)}\frac{R_g}{R_\ell}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to \infty} = \frac{1.1}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}\right)}\frac{R_g}{R_h}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega = \omega_Z} = 0$$

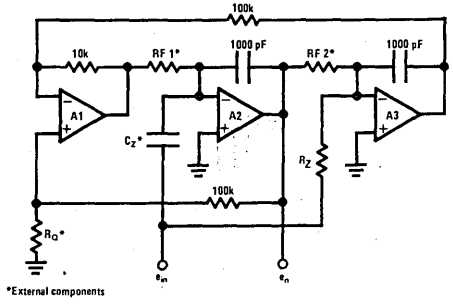


FIGURE 7. Input Notch Using Three Amplifiers

j) Input notch *(Figure 7)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = \frac{\frac{C_Z}{10^{-9}}\left[s^2 + \omega_Z{}^2\right]}{s^2 + s\,\omega_1\left[\frac{1.1\,RQ}{10^5 + RQ}\right] + \omega_0{}^2}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

$$\omega_Z = \omega_0\sqrt{\frac{RF2 \times 10^{-9}}{R_Z\,C_Z}} \qquad \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to 0} = -\frac{R_{F2}}{R_Z}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to \infty} = -\frac{C_Z}{10^{-9}}$$

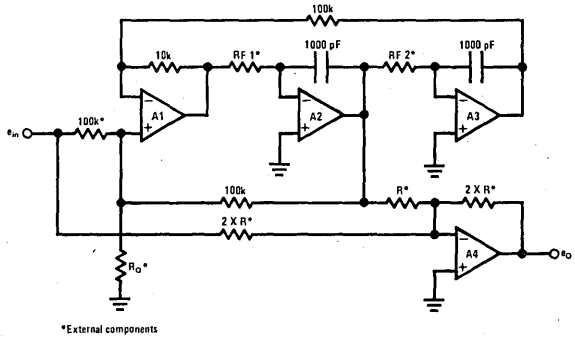


FIGURE 8. Allpass

g) Allpass *(Figure 8)* transfer function equations are:

$$\frac{e_o}{e_{IN}} = -\left[\frac{s^2 - s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{RQ}}\right] + \omega_0{}^2}{s^2 + s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{RQ}}\right] + \omega_0{}^2}\right]$$

$$Q = \frac{2 + \frac{10^5}{RQ}}{1.1}\sqrt{0.1\,\frac{\omega_2}{\omega_1}}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

Time delay at $\omega_0 = \frac{2Q}{\omega_0}$ seconds

FREQUENCY TUNING

To tune the AF100 two resistors are required for frequencies between 200 Hz and 10 kHz. For lower frequencies "T" tuning or addition of external capacitors

Applications Information (Continued)

is required. Using external capacitors allows the user to go as low in frequency as he desires. "T" tuning and external capacitors can be used together.

Two resistor tuning for 200 Hz to 10 kHz

$$R_f = \frac{50.33 \times 10^6}{f_o}\ \Omega$$

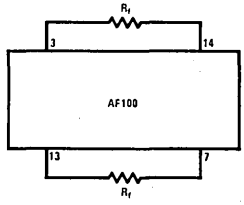
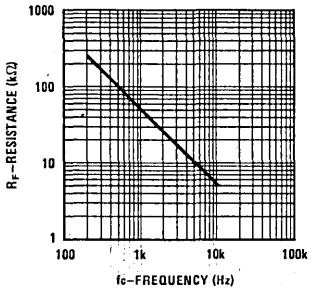


FIGURE 9. Resistive Tuning

GRAPH A. Resistive Tuning



"T" resistive tuning for $f_O < 200$ Hz

$$R_s = \frac{R_t^2}{R_f - 2R_t} \qquad R_t < \frac{R_F}{2}$$

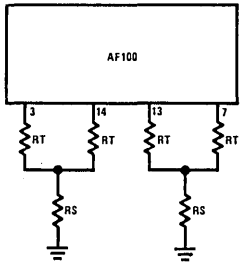
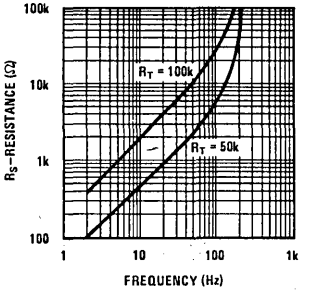


FIGURE 10. T Tuning

GRAPH B. "T" Tuning



RC tuning for $f_O < 200$ Hz

$$R_f = \frac{0.05033}{f_o\ (C + 1 \times 10^{-9})}$$

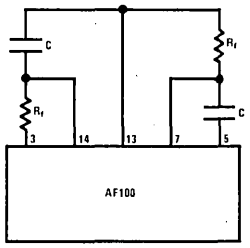
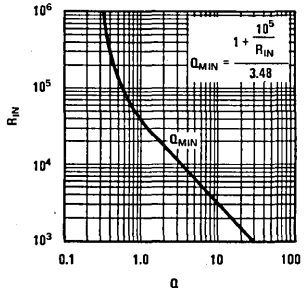


FIGURE 11. Low Frequency RC Tuning

Q TUNING

To tune the Q of an AF100 requires one resistor from pins 1 or 2 to ground. The value of the Q tuning resistor depends on the input connection and input resistance as well as the value of the Q. The Q of the unit is inversely proportional to resistance to ground at pin 1 and directly proportional to resistance to ground from pin 2.

GRAPH C. Q_{MIN}, Non-Inverting Input



For $Q > Q_{MIN}$ in non-inverting mode:

$$RQ = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}}$$

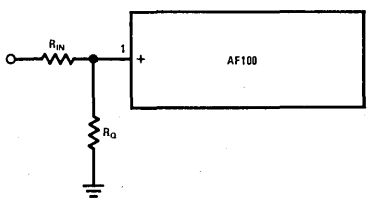
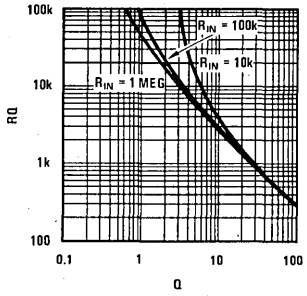


FIGURE 12. Q Tuning for $Q > Q_{MIN}$, Non-Inverting Input

Applications Information (Continued)

GRAPH D. Q > Q_{MIN}, Non-Inverting Input



For $Q < Q_{MIN}$ in non-inverting mode:

$$RQ = \frac{10^4}{0.3162 \frac{\left(1 + \frac{10^5}{R_{IN}}\right)}{Q} - 1.1}$$

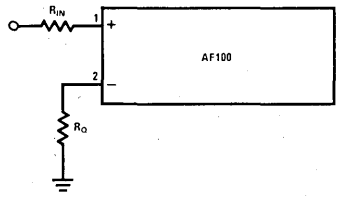
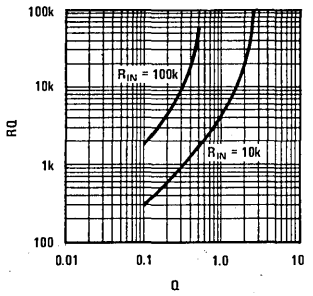


FIGURE 13. Q Tuning for $Q < Q_{MIN}$, Non-Inverting Input

GRAPH E. $Q < Q_{MIN}$, Non-Inverting Input



For any Q in inverting mode:

$$RQ = \frac{10^5}{3.16Q \left(1.1 + \frac{10^4}{R_{IN}}\right) - 1}$$

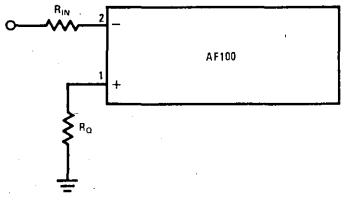
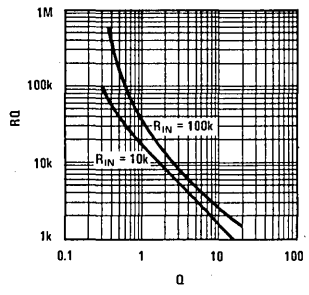


FIGURE 14. Q Tuning Inverting Input

GRAPH F. Q Tuning, Inverting Input



NOTCH TUNING

Two methods to generate notches are the RC input and lowpass/highpass summing. The RC input method requires adding a capacitor and resistor connected to the two integrator inputs. The capacitor connects to "Int 1" and the resistor connects to "Int 2." The output summing requires two resistors connected to the lowpass and highpass output.

For input RC notch tuning:

$$R_Z = \frac{R_F \times 10^{-9}}{C_Z} \left(\frac{f_O}{f_Z}\right)^2$$

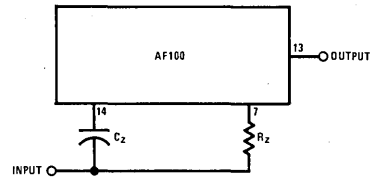
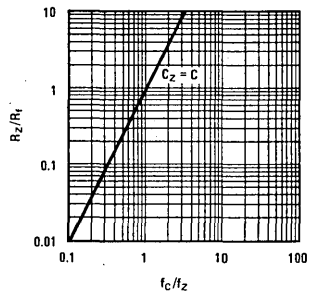


FIGURE 15. Input RC Notch

GRAPH G. Input RC Notch



For output notch tuning:

$$R_{HP} = \left(\frac{f_Z}{f_O}\right)^2 \frac{R_{LP}}{10}$$

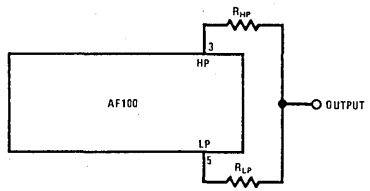
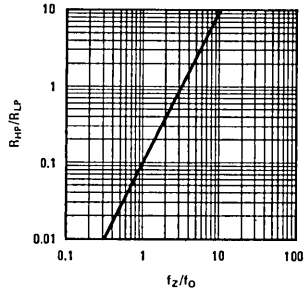


FIGURE 16. Output Notch

Applications Information (Continued)

GRAPH H. Output Notch



TUNING TIPS

In applications where 2 to 3% accuracy is not sufficient to provide the required filter response, the AF100 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the bandpass (pin 13) output.

Before any tuning is attempted the lowpass (pin 7) output should be checked to see that the output is not clipping. At the center frequency of the section the lowpass output is 10 dB higher than the bandpass output and 20 dB higher than the highpass. This should be kept in mind because if clipping occurs the results obtained when tuning will be incorrect.

Frequency Tuning

By adjusting the resistance between pins 7 and 13 the center frequency of a section can be adjusted. If the input is through pin 1 the phase shift at center frequency will be 180° and if the input is through pin 2 the phase shift at center frequency will be 0°. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

"Q" Tuning

The "Q" is tuned by adjusting the resistance between pin 1 or 2 and ground. Low Q tuning resistors will be from pin 2 to ground ($Q < 0.6$). High Q tuning resistors will be from pin 1 to ground. To tune the Q correctly the signal source must have an output impedance very much lower than the input resistance of the filter since the input resistance affects the Q. The input must be driven through the same resistance the circuit will see to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right) \times (f_O)$$

where f_O = center frequency

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q}\right) \times (f_O)$$

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair the notch can be tuned by adjusting the ratio of the summing resistors (lowpass/highpass summing) or the input resistance (input RC).

In either case the signal is connected to the input and the proper resistor is adjusted for a null at the output.

Special Cases

When using the input RC notch the unit cannot be tuned through the normal input so an additional 100k resistor can be added at pin 1 and the unit can be tuned normally. Then the 100k input resistor should be grounded and the notch tuned through the normal RC input.

An alternative way of tuning is to tune using the Q resistor as the input. This requires the Q resistor be lifted from ground and connecting the signal source to the normally grounded end of the Q resistor. This has the problem that when the Q resistor is grounded after tuning, its value is decreased by the output impedance of the source. This technique has the advantage of not requiring an additional resistor.

TUNING PROCEDURE (See *Figure 17*)

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the lowpass output pin 5 (AF100J).

Adjust the resistance between pins 13 and 7 until the phase shift between input and bandpass output is 180°.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

Zero Tuning

Set the oscillator output to the zero frequency and tune the zero resistor for a null at the output of the summing amplifier.

Gain Adjust

Set the oscillator to any desired frequency and the gain can be adjusted by measuring the output of the summing amplifier and adjusting the feedback resistance.

Applications Information (Continued)

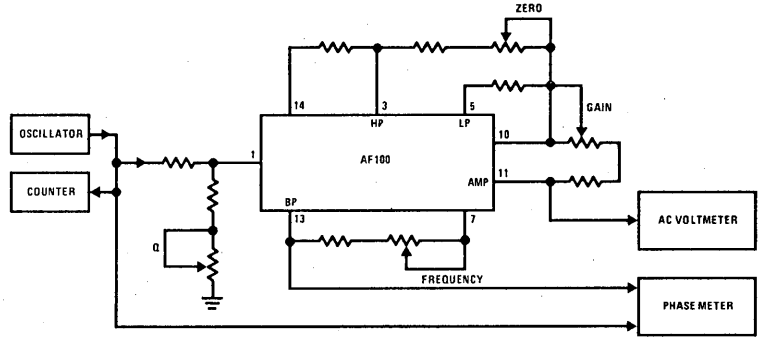


FIGURE 17. Filter Tuning Setup

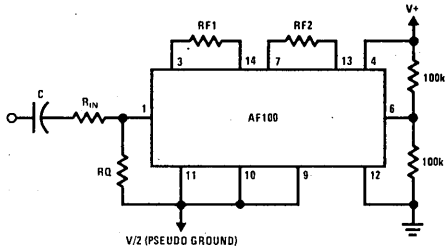


FIGURE 18. Single Power Supply Connection Using Uncommitted Amplifier to Split Supply

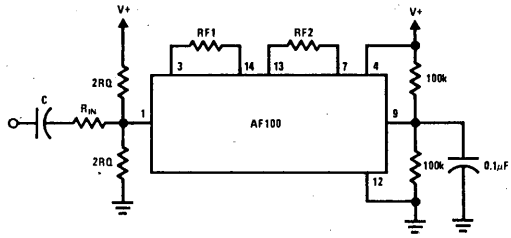
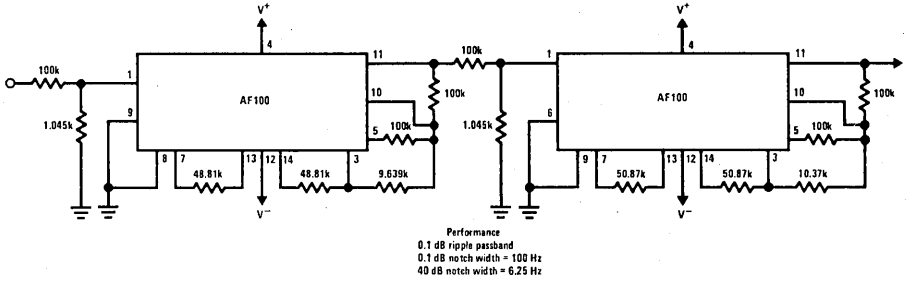
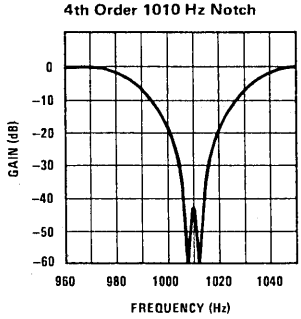


FIGURE 19. Single Power Supply Connection Using Resistive Dividers





STAGE 1

F_c = 1031.1 Hz
Q = 28.34
F_z = 1012.2 Hz

STAGE 2

F_c = 989.3 Hz
Q = 28.34
F_z = 1007.8 Hz

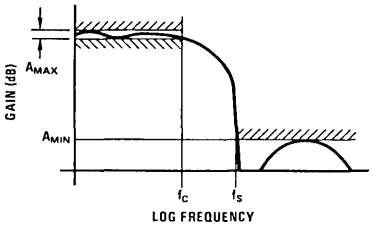
FIGURE 20. 1010 Hz Notch–Telephone Holding Tone Reject Filter

FILTER DESIGN

Since most filter tables are in terms of a normalized lowpass prototype, the filter to be designed is usually reduced to a lowpass prototype. After the lowpass transfer function is found, it is transformed to obtain the transfer function for the actual filter desired. *Graph I* shows the lowpass amplitude response which can be defined by four quantities.

Applications Information (Continued)

GRAPH I. Lowpass Prototype Response



A_{MAX} = the maximum peak to peak ripple in the passband.

A_{MIN} = the minimum attenuation in the stopband.

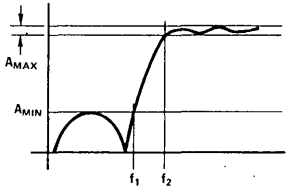
f_C = the passband cutoff frequency.

f_S = the stopband start frequency.

By defining these four quantities for the lowpass prototype the normalized pole and zero locations and the Q (quality) of the poles can be determined from tables or by computer programs.

To obtain the lowpass prototype for the highpass filter (*Graph J*) A_{MAX} and A_{MIN} are the same as for the lowpass case but $f_C = 1/f_2$ and $f_S = 1/f_1$.

GRAPH J. Highpass Response



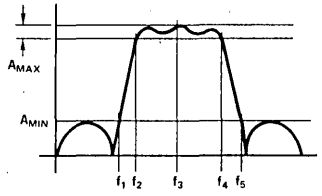
To obtain the lowpass prototype for a bandpass filter (*Graph K*) A_{MAX} and A_{MIN} are the same as for the lowpass case but

$$f_C = 1 \quad f_S = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 f_5} = \sqrt{f_2 f_4}$ i.e. geometric symmetry

$f_5 - f_1$ = A_{MIN} bandwidth
$f_4 - f_2$ = Ripple bandwidth

GRAPH K. Bandpass Response

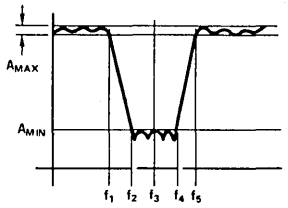


To obtain the lowpass prototype for the notch filter (*Graph L*) A_{MAX} and A_{MIN} are the same as for the lowpass case and

$$f_C = 1 \qquad f_S = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 f_5} = \sqrt{f_2 f_4}$

GRAPH L. Notch Response



Normalized Lowpass Transformed To Un-Normalized Lowpass

The normalized lowpass filter has the passband edge normalized to unity. The un-normalized lowpass filter instead has the passband edge at f_C. The normalized and un-normalized lowpass filters are related by the transformation $s = s\omega_c$. This transforms the normalized passband edge $s = j$ to the un-normalized passband edge $s = j\omega_C$.

Normalized Lowpass Transformed To Un-Normalized Highpass

The transformation that can be used for lowpass to highpass is $S = \omega_C/s$. Since S is inversely proportional to s, the low frequency and high frequency responses are interchanged. The normalized lowpass $1/(S^2 + S/Q+1)$ transforms to the un-normalized highpass

$$\frac{s^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c{}^2}$$

Normalized Lowpass Transformed To Un-Normalized Bandpass

The transformation that can be used for lowpass to bandpass is $S = (s^2 + \omega_0{}^2)/BWs$ where $\omega_0{}^2$ is the center frequency of the desired bandpass filter and BW is the ripple bandwidth.

Normalized Lowpass Transformed To Un-Normalized Bandstop (Or Notch)

The bandstop filter has a reciprocal response to a bandpass filter. Therefore a bandstop filter can be obtained by first transforming the lowpass prototype to a highpass and then performing the bandpass transformation.

SELECTION OF TRANSFER FUNCTION

The selection of a function which approximates the shape of the response desired is a complicated process. Except in the simplest cases it requires the use of tables or computer programs. The form of the transfer function desired is in terms of the pole and zero locations. The most common approximations found in tables are Butterworth, Tschebycheff, Elliptic, and Bessel. The decision as to which approximation to use is usually a function of the requirements and system objectives. Butterworth filters are the simplest but have the disadvantage of requiring high order transfer functions to obtain sharp roll-offs.

Applications Information (Continued)

The Tschebycheff function is a min/max approximation in the passband. This approximation has the property that it is equiripple which means that the error oscillates between maximums and minimums of equal amplitude in the passband. The Tschebycheff approximation, because of its equiripple nature, has a much steeper transition region than the Butterworth approximation.

The elliptic filter, also known as Cauer or Zolotarev filters, are equiripple in the passband and stopband and have a steeper transition region than the Butterworth or the Tschebycheff.

For a specific lowpass filter three quantities can be used to determine the degree of the transfer function: the maximum passband ripple, the minimum stopband attenuation, and the transition ratio ($tr = \omega_S/\omega_C$). Decreasing A_{MAX}, increasing A_{MIN}, or decreasing tr will increase the degree of the transfer function. But for the same requirements the elliptic filter will require the lowest order transfer function. Tables and graphs are available in reference books such as "Reference Data for Radio Engineers," Howard W. Sams & Co., Inc., 5th Edition, 1970 and Erich Christian and Egon Eisenmann, "Filter Design Tables and Graphs," John Wiley and Sons, 1966.

For specific transfer functions and their pole locations such text as Louis Weinberg, "Network Analysis and Synthesis," McGraw Hill Book Company, 1962 and Richard W. Daniels, "Approximation Methods for Electronic Filter Design," McGraw-Hill Book Company, 1974, are available.

DESIGN OF CASCADED MULTISECTION FILTERS

The first step in designing is to define the response required and define the performance specifications:

1. Type of filter:
   Lowpass, highpass, bandpass, notch, allpass
2. Attenuation and frequency response
3. Performance
   Center frequency/corner frequency plus tolerance and stability
   Insertion loss/gain plus tolerance and stability
   Source impedance
   Load impedance
   Maximum output noise
   Power consumption
   Power supply voltage
   Dynamic range
   Maximum output level

Second step is to find the pole and zero location for the transfer function which meet the above requirements. This can be done by using tables and graphs or network synthesis. The form of the transfer function which is easiest to convert to a cascaded filter is a product of first and second order terms in these forms:

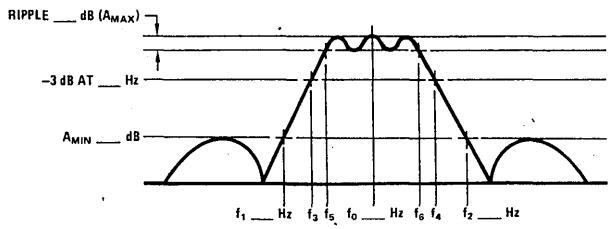
First Order	Second Order	
$\frac{K}{s+\omega_R}$	$\frac{K}{s^2+\frac{\omega_0}{Q}s+\omega_0{}^2}$	(low pass)
$\frac{Ks}{s+\omega_R}$	$\frac{Ks^2}{s^2+\frac{\omega_0}{Q}s+\omega_0{}^2}$	(highpass)
	$\frac{Ks}{s^2+\frac{\omega_0}{Q}s+\omega_0{}^2}$	(bandpass)
	$\frac{K(s^2+\omega_Z{}^2)}{s^2+\frac{\omega_0}{Q}s+\omega_0{}^2}$	(notch)
	$\frac{s^2-\frac{\omega_0}{Q}s+\omega_0{}^2}{s^2+\frac{\omega_0}{Q}s+\omega_0{}^2}$	(allpass)

Each of the second order functions is realizable by tuning an AF100 stage. By cascading these stages the desired transfer function is realized.

CASCADING SECOND ORDER STAGES

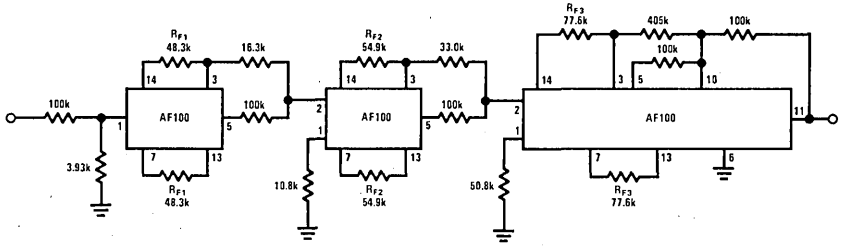
The primary concern in cascading second order stages is to minimize the maximum difference in amplitude from input to output over the frequencies of interest. A computer program is probably required in very complicated cases but some general rules that can be used that will usually give satisfactory results are:

GRAPH M. Generalized Model Response



Applications Information (Continued)

1. The highest "Q" pole pair should be paired with the zero pair closest in frequency.
2. If highpass and lowpass stages are cascaded the lowpass sections should be the higher frequency and highpass sections the lower frequency.
3. In cascaded filters of more than two sections the first section should be the section with "Q" closest to 0.707 and then additional stages should be added in order of least difference between first stage Q and their Q.



Lowpass Elliptic Filter

$F_C = 1$
$F_S = 1.3$
$A_{MAX} = 0.1$ dB
$A_{MIN} = 40$ dB
$N = 6$

$f_{O1} = 1.0415 \quad Q_1 = 7.88 \quad f_{Z1} = 1.329 \quad f_Z/f_O = 1.28 \quad \left(\frac{f_Z}{f_O}\right)^2 = 1.63$

$f_{O2} = 0.9165 \quad Q_2 = 1.79 \quad f_{Z2} = 1.664 \quad f_Z/f_O = 1.82 \quad \left(\frac{f_Z}{f_O}\right)^2 = 3.30$

$f_{O3} = 0.649 \quad Q_3 = 0.625 \quad f_{Z3} = 4.1285 \quad f_Z/f_O = 6.36 \quad \left(\frac{f_Z}{f_O}\right)^2 = 40.5$

$$R_{F1} = \frac{(503.3)}{f_{O1} \times f_C} \times 10^5 \qquad R_{F2} = \frac{(503.3)}{f_{O2} \times f_C} \times 10^5 \qquad R_{F3} = \frac{(503.3)}{f_{O3} \times f_C}$$

at 1000 Hz = f_C

$R_{F1} = 48.3k \qquad R_{F2} = 54.9k \qquad R_{F3} = 77.6k$

6th Order Elliptic Filter

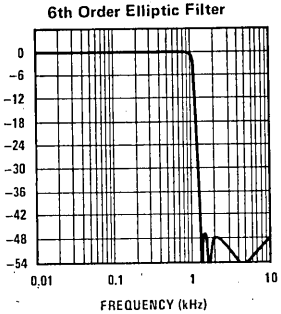
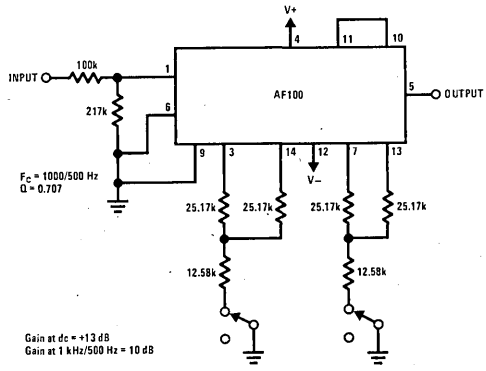


FIGURE 21. Lowpass Elliptic Filter Example

Applications Information (Continued)



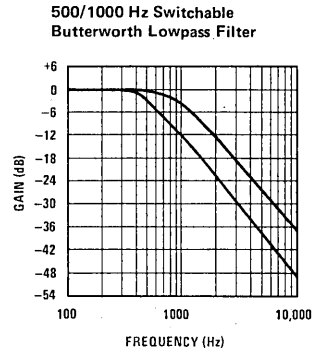
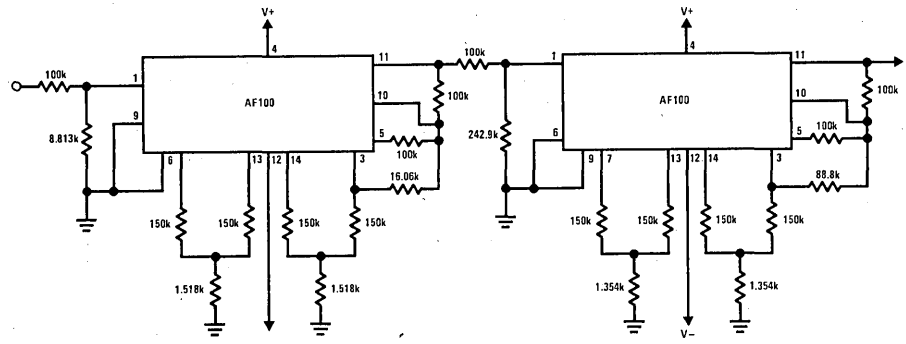
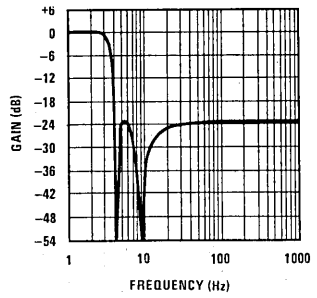


FIGURE 22. Switchable Filter Example: 500 Hz/1000 Hz Butterworth Lowpass



STAGE 1

F_C = 3.328 Hz
Q = 3.84
F_Z = 4.218 Hz



STAGE 2

F_C = 2.975 Hz
Q = 0.693
F_Z = 8.865 Hz

FIGURE 23. EEG Delta Filter—3 Hz Lowpass

Applications Information (Continued)

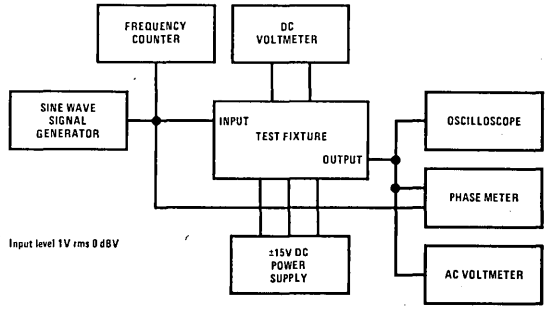


FIGURE 25. Test Circuit Block Diagram

COMPUTER AIDED DESIGN EXAMPLE*

This design is an example of a 60 Hz notch filter. The response is to have the following specifications:

Maximum passband ripple 0.1 dB

Minimum rejection 35 dB

0.1 dB bandwidth 15 Hz max

−35 dB bandwidth 1.5 Hz min

The steps in the design of this filter are:

1. Design a lowpass "prototype" for the filter.
2. Transformation of the lowpass prototype into a notch filter design.
3. Using the pole and zero locations found in step two calculate the value of the resistors required to build the filter.
4. Draw a schematic of filter using values obtained in step three.

*Computer programs shown are user interactive. Underlined copy is user input, non-underlined copy is computer response, and line indications in parenthesis are included for easy identification of data common to several programs.

PROGRAM NO. 1

```
RUN

THIS PROGRAM DESIGNS BUTTERWORTH CHEBYCHEFF OR ELLIPTIC NORMALIZED
LOWPASS FILTERS
WHAT TYPE OF FILTER ? B-C-E

ELLIPTIC
 DO YOU KNOW THE ORDER OF THE FILTER ? Y/N
? NO
INPUT FC,FS,AMAX,AMIN
? 1, 10, .1, 35
     FC                    1.000
     FS                   10.000
     AMAX                   .100
     AMIN                 35.000
     N                     2.000
     ATT AT FS          −35.671     (ATTENUATION IN dB)
IS THIS SATISFACTORY ? Y/N
? YES

   F                 Q
    1.823 (Line 1.1)      .775 (Line 1.2)
   Z
   14.124 (Line 1.3)
```

Applications Information (Continued)

PROGRAM NO. 2
(DETERMINES UN-NORMALIZED POLE + ZERO LOCATIONS OF FIRST SECTION)
(DATA ENTERED FROM PROGRAM NO. 1)

```
RUN
WHAT TYPE FILTER BANDPASS OR NOTCH
? NOTCH
ENTER # OF POLE PAIRS? 1

ENTER # OF JW AXIS ZEROS? 1

  ENTER # OF REAL POLES? 0

  ENTER # OF ZEROS AT ZERO? 0

  ENTER # OF COMPLEX ZEROS? 0

ENTER # OF REAL ZEROS? 0

   ENTER F & Q OF EACH POLE PAIR
? 1.823, .775  (FROM LINE 1.1 AND LINE 1.2)

ENTER VALUES OF JW AXIS ZEROS
? 14.124  (FROM LINE 1.3)

ENTER FREQUENCY SCALING FACTOR
? 1
  ENTER THE # OF FILTERS TO BE DESIGNED
? 1
  ENTER THE C.F. AND BW OF EACH FILTER
? 60, 15
```

OUTPUT OF PROGRAM NO. 2
TRANSFORMED POLE/ZERO LOCATIONS
FIRST SECTION

```
                POLE LOCATIONS
   CENTER FREQ.                    Q

56.93601   (From Line 2.3)     11.31813  (From Line 2.4)
63.228877  (From Line 2.5)     11.31813  (From Line 2.6)
                JW AXIS ZEROS
59.471339  (From Line 2.1)
60.533361  (From Line 22
```

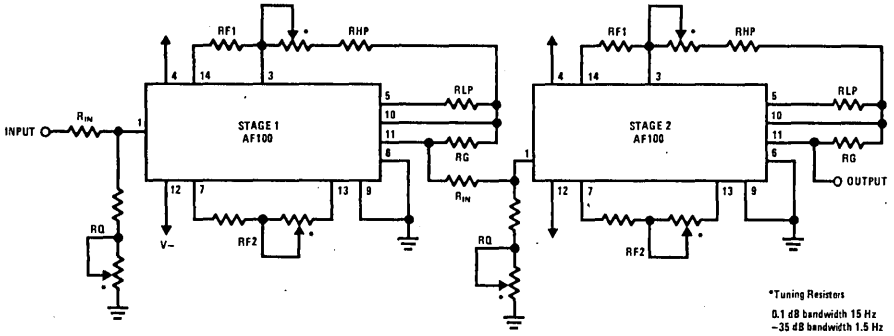
PROGRAM NO. 3
(CHECK OF FILTER RESPONSE USING PROGRAM NO. 2 DATA BASE)

```
RUN

NUMERATOR (ZEROS)
A(I)S^2+R(I)S+Z(I)^2
 1     0     59.471339     (From Line 2.1)
 1     0     60.533361     (From Line 2.2)

REAL POLE

COMPLEX POLE PAIRS

        F          Q
1     56.93601   11.31813   (From Lines 2.3 and 2.4)
2     63.228877  11.31813   (From Lines 2.5 and 2.6)
```

RUN

FREQUENCY	NOR. GAIN (DB)	PHASE	DELAY	NOR. DELAY	FREQUENCY	NOR. GAIN (DB)	PHASE	DELAY	NOR. DELAY
40.000	.032	347.69	.002275	5.847169	60.600	−47.102	169.17	.050801	108.232021
45.000	.060	342.20	.004107	8.749738	60.800	−33.650	165.48	.051677	110.096278
50.000	.100	330.70	.009983	21.268142	61.000	−27.577	161.72	.052809	112.508334
55.000	−.795	290.54	.046620	99.324027	61.200	−23.418	157.87	.054167	115.403169
56.000	−2.298	270.61	.063945	136.234562	61.400	−20.198	153.92	.055712	118.694436
57.000	−5.813	245.51	.072894	155.299278	61.600	−17.554	149.85	.057391	122.270086
58.000	−12.748	220.19	.065758	140.096912	61.800	−15.308	145.65	.059136	125.989157
58.200	−14.740	215.54	.063369	135.006390	62.000	−13.362	141.33	.060869	129.681062
58.400	−17.032	211.06	.060979	129.914831	63.000	−6.557	118.23	.065975	140.559984
58.600	−19.722	206.76	.058692	125.043324	64.000	−2.936	95.30	.059402	126.556312
58.800	−22.983	202.61	.056588	120.561087	65.000	−1.215	76.38	.045424	96.774832
59.000	−27.172	198.60	.054724	116.589928	66.000	−.463	62.43	.032614	69.484716
59.200	−33.235	194.72	.053139	113.212012	67.000	−.138	52.44	.023498	50.062947
59.400	−46.300	190.94	.051856	110.478482	70.000	.091	35.43	.010452	22.267368
59.600	−42.909	7.24	.050888	108.417405	75.000	.085	23.44	.004250	9.054574
59.800	−36.897	3.60	.050242	107.040235	80.000	.060	17.80	.002310	4.921727
60.00	−35.567	360.00	.049916	106.346516	85.000	.043	14.50	.001460	3.110493
60.200	−36.887	356.41	.049907	106.326777	90.000	.032	12.31	.001011	2.154297
60.400	−42.757	352.81	.050206	106.963750					

Applications Information (Continued)



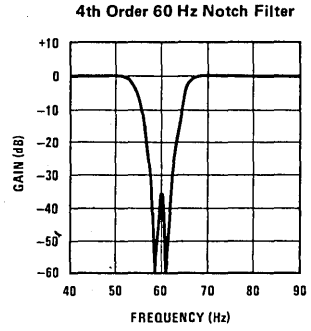


FIGURE 26. Implementation of a 60 Hz Notch From Computer Calculations

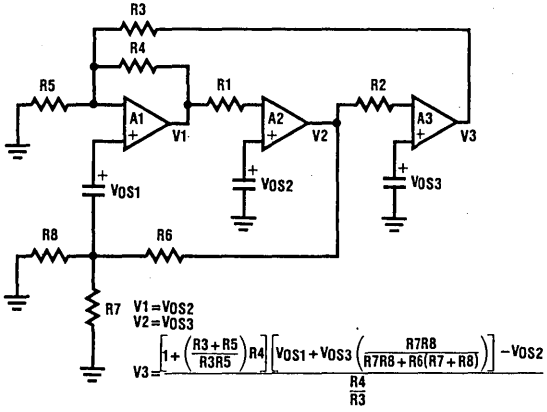


FIGURE 27. DC Output Voltage Due to Amplifier V_{OS}

DEFINITION OF TERMS

A_{MAX}	Maximum passband peak-to-peak ripple
A_{MIN}	Minimum stopband loss
f_Z	Frequency of jw axis pair
f_O	Frequency of complex pole pair
Q	Quality of pole
f_C	Passband edge
f_S	Stopband edge
A_{HP}	Gain from input to highpass output
A_{BP}	Gain from input to bandpass output
A_{LP}	Gain from input to lowpass output
A_{AMP}	Gain from input to output of amplifier
R_f	Pole frequency determining resistance
R_Z	Zero Frequency determining resistance
R_Q	Pole Quality determining resistance
f_H	Frequency above center frequency at which the gain decreases by 3 dB for a bandpass filter
f_L	Frequency below center frequency at which the gain decreases by 3 dB for a bandpass filter
BW	The bandwidth of a bandpass filter
N	Order of the denominator of a transfer function

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E. Christian and E. Eisenmann, *"Filter Design Tables and Graphs,"* John Wiley & Sons, New York, 1966

A. I. Zverev, *"Handbook of Filter Synthesis,"* John Wiley & Sons, New York, 1967

Burr-Brown Research Corp., *"Handbook of Operational Amplifier Design and Applications,"* McGraw-Hill Book Co., New York, 1971

National Semiconductor

AF101 High Band Splitter Filter

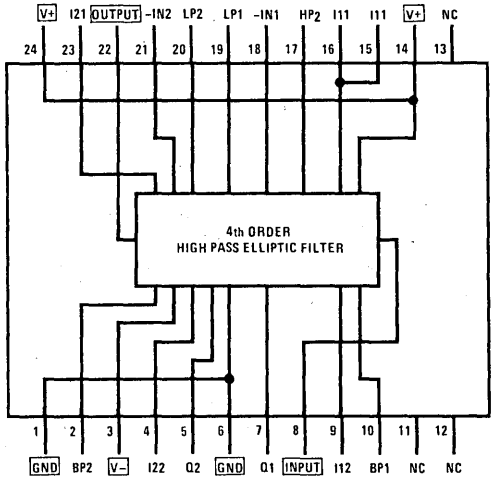
General Description

The AF101 is a fourth order high pass elliptic filter designed to pass frequencies above 1200 Hz. This filter is used to separate the high band of frequencies from the low band in a Dual Tone Multi Frequency (DTMF) Touch Tone® receiver. The unit is fully tuned and requires no external components – only power supply, input, and output connections.

Features

- Fully tuned
- High input impedance
- Low output impedance
- Wide power supply range ±5V to ±18V

Connection Diagram



Ceramic Dual-In-Line Package HY24A
AF101CJ

Note: Only those pin functions marked with a □ need be connected for normal operation. All other pins are internal connections or test points; DO NOT USE.

® Registered service mark of AT&T Company.

Absolute Maximum Ratings

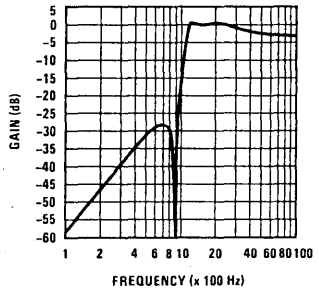
Supply Voltage	±18V
Power Dissipation	1W
Input Voltage	±36V
Output Short Circuit Duration	Infinite
Lead Temperature (soldering, 10 sec.)	300°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−25°C to +100°C

Electrical Characteristics $V_S \pm 12V$ to $\pm 15V$, $T_A = 0°C$ to 70°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cutoff Frequency	f_c			1190	1209	Hz
Passband Ripple	A_{MAX}	1190 to 1660Hz	−0.5	0	0.5	dB
Stopband Edge	f_s		941	955		Hz
Stopband Attenuation	A_{MIN}		25	28		dB
Gain	A_O	at 1336Hz	−0.5	0	+0.5	dB
Group Delay	gd				2	ms
Input Impedance	Z_{IN}		30k	32k		Ω
Output Impedance	Z_O			< 1	5	Ω
Operating Supply Voltage	V_S		±5		±18	V
Power Supply Current	I_S	$V_S = \pm 15V$		5	9	mA

Typical Performance Characteristics

Typical Amplitude Response



National Semiconductor

AF102 Dial Tone Reject Filter

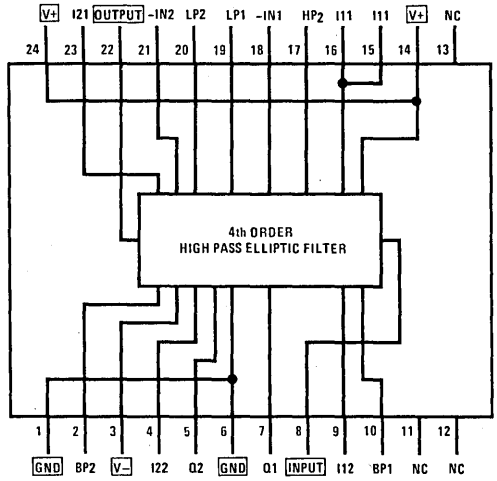
General Description

The AF102 is a fourth order elliptic highpass filter designed to reject frequencies below 650Hz. This filter rejects the 350Hz and 440Hz dial tone frequencies present on a telephone line. The unit is fully tuned and requires no external components – only input, output and power supply connections.

Features

- Fully tuned
- High input impedance
- Low output impedance
- Wide power supply range ±5V to ±18V

Connection Diagram



Ceramic Dual-In-Line Package HY24A
AF102CJ

Note: Only those pin functions marked with a □ need be connected for normal operation. All other pins are internal connections or test points; DO NOT USE.

Absolute Maximum Ratings

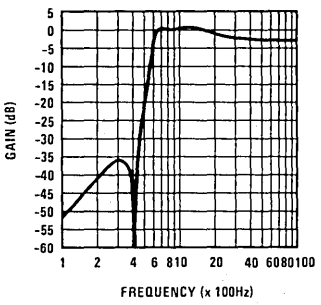
Supply Voltage	±18V
Power Dissipation	1W
Input Voltage	±36V
Output Short Circuit Duration	Infinite
Lead Temperature (soldering, 10 sec.)	300°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-25°C to +100°C

Electrical Characteristics $V_S \pm 12V$ to $\pm 15V$, $T_A = 0°C$ to 70°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cutoff Frequency	f_c			685	697	Hz
Passband Ripple	A_{MAX}	f = 685Hz to 1660Hz	-0.5	0	0.5	dB
Stopband Frequency	f_s		440	450		Hz
Stopband Attenuation	A_{MIN}	f < 440Hz	34	35		dB
Gain	A_O	at 941Hz	-0.5	0	0.5	dB
Group Delay	gd				2	ms
Input Impedance	Z_{IN}		29k	30k		Ω
Output Impedance	Z_O			< 1	5	Ω
Power Supply Voltage	V_S		±5		±18	V
Power Supply Current	I_S	$V_S = \pm 15V$		5	9	mA

Typical Performance Characteristics

Typical Amplitude Response



National Semiconductor

AF103 Low Band Splitter

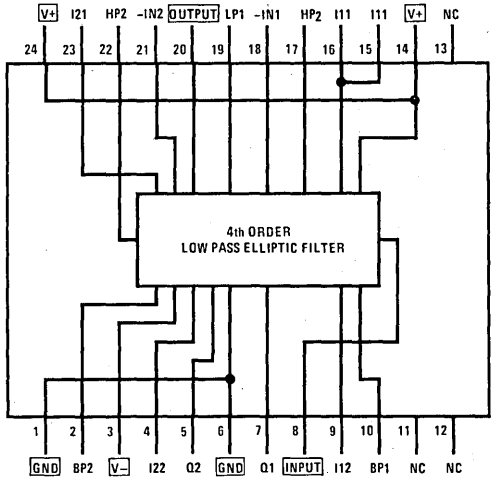
General Description

The AF103 is a fourth order elliptic low pass filter designed to reject frequencies above 1200 Hz and pass signals below 950 Hz. This filter is used to separate the low band of frequencies from the high band in a Dual Tone Multi Frequency (DTMF) Touch Tone® receiver. The unit is fully tuned and requires no external components – only power supply, input and output connections.

Features

- Fully tuned
- High input impedance
- Low output impedance
- Wide power supply range ±5V to ±18V

Connection Diagram



Ceramic Dual-In-Line Package HY24A
AF103CJ

Note: Only those pin functions marked with a □ need be connected for normal operation. All other pins are internal connections or test points; DO NOT USE.

® Registered service mark of AT&T Company.

Absolute Maximum Ratings

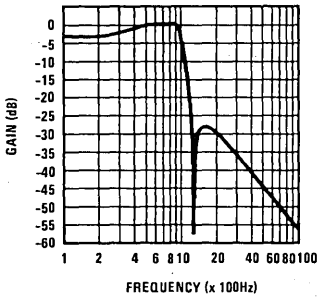
Supply Voltage	±18V
Power Dissipation	1W
Input Voltage	±36V
Output Short Circuit Duration	Infinite
Lead Temperature (soldering, 10 sec.)	300°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-25°C to +100°C

Electrical Characteristics $V_S \pm 12V$ to $\pm 15V$, $T_A = 0°C$ to 70°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cutoff Frequency	f_c		941	955		Hz
Passband Ripple	A_{MAX}	f = 686 Hz to 955 Hz	-0.5	0	0.5	dB
Stopband Frequency	f_s			1190	1209	Hz
Stopband Attenuation	A_{MIN}	f > 1200 Hz	25	28		dB
Gain	A_O	at 852 Hz	-0.5	0	0.5	dB
Group Delay	gd				2	ms
Input Impedance	Z_{IN}		30k	33k		Ω
Output Impedance	Z_O			< 1	5	Ω
Operating Supply Voltage	V_S		±5		±18	V
Power Supply Current	I_S	$V_S = \pm 15V$		5	9	mA

Typical Performance Characteristics

Typical Amplitude Response



National Semiconductor

AF104/AF105 DTMF AGC Amplifier

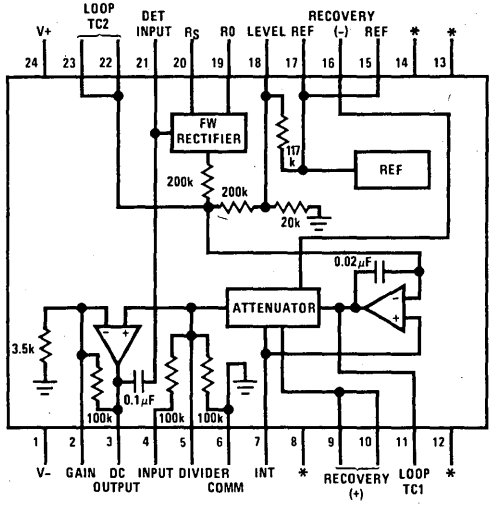
General Description

The AF104 AGC Amplifier is a direct coupled amplifier whose voltage gain is internally controlled by the output signal. The gain control feedback system is AC coupled so that DC signals do not affect the gain.

Features

- Optional gain adjustment
- High input impedance 100k
- 0dBm output level
- Internal reference
- Wide supply voltage range ±9.0V to ±18V
- Input level range +30dBm (2.45 V_{rms})
- Frequency range 500Hz to 10kHz

Connection Diagram



Ceramic Dual-In-Line Package HY24A
AF104CJ
AF105CJ

*Internally connected. DO NOT USE.

Absolute Maximum Ratings

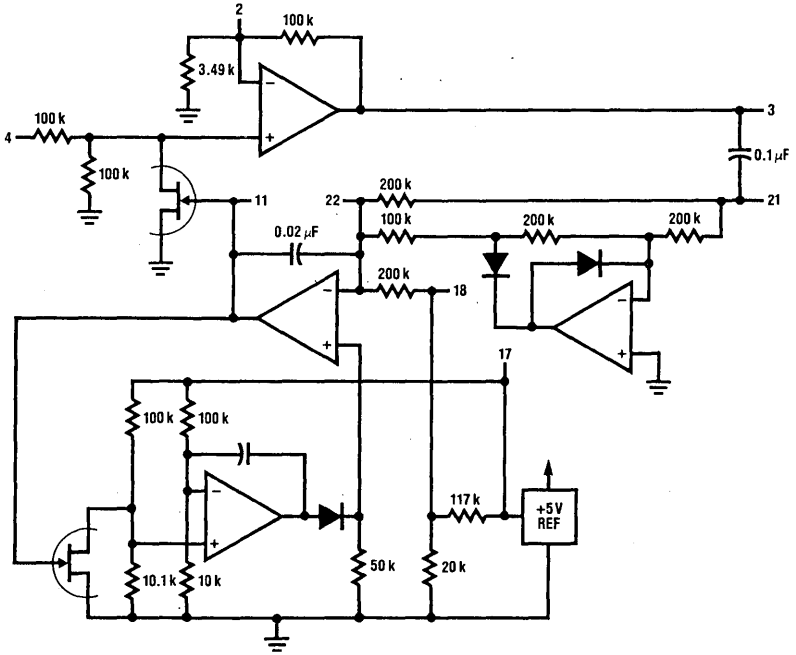
Supply Voltage	±18V
Power Dissipation	1W
Input Voltage	±36V
Output Short Circuit Duration	Infinite
Lead Temperature (soldering, 10 sec.)	300°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−25°C to +100°C

Electrical Characteristics

$V_S = \pm 12V$ to $\pm 15V$, $T_A = 0°C$ to 70°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Level	V_O	Single 1kHz tone of $-22 \leq A \leq +10$dBm	−0.35	0	0.35	dBm
Input Level	V_{IN}		−20		+10	dBm
Input Impedance	Z_{IN}			100		kΩ
Open Loop Gain	A_O	AF104 AF105	21.4 22.4	22 23	22.6 23.6	dB dB
Output Impedance	Z_O			< 1		Ω
Recovery Time		Input step from no signal, 0dBm, 1kHz tone		5		ms
Power Supply Voltage	V_S		±9		±18	V
Power Supply Current V^+ V^-	I_S^+ I_S^-			5.5 2.5	11 5	mA mA
Operating Frequency Range			0.5	0.3 To 12	10	kHz

Schematic Diagram



OPEN LOOP GAIN ADJUSTMENT

The open loop gain is internally set to 21dB but can be externally adjusted by adding one external resistor. The practical limits are 0dB to 40dB. When the gain is increased the bandwidth is decreased.

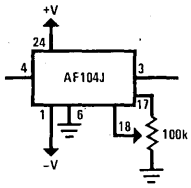
OUTPUT LEVEL ADJUSTMENT

The output level can be adjusted by connecting a 100k pot between pin 17 and ground with the wiper arm connected to pin 18. Output level can be adjusted ±10dB without affecting other parameters such as loop time constant and recovery time.

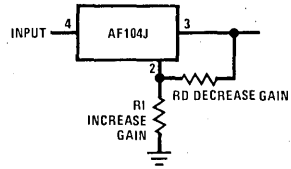
EXTENDING LOW FREQUENCY RESPONSE

An external capacitor in parallel with the internal loop time constant capacitor will extend the low frequency response and lower the distortion through the AGC. It has the effect of slowing the response time due to the longer loop time constant. To maintain amplitude stability at low frequencies an external capacitor should be added in parallel with the loop coupling capacitor.

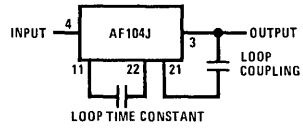
Test Circuits



Output Level Adjust



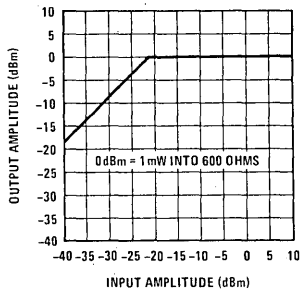
Open Loop Gain Adjust



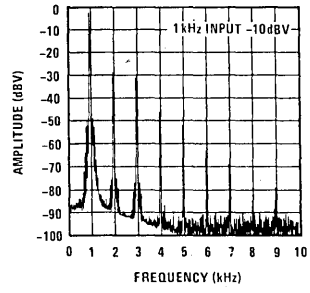
AGC Loop Response

Typical Performance Characteristics

Transfer Characteristic



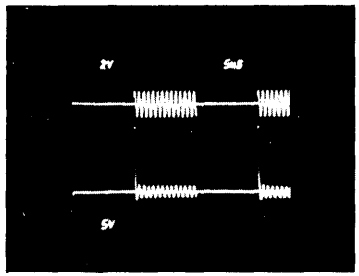
Frequency Response



Transient Response

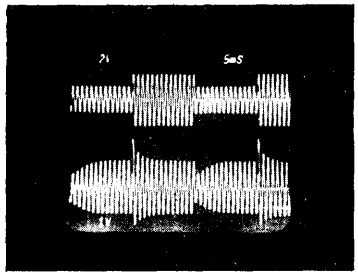
Input
0, 0.77V Step (1 kHz)

Output



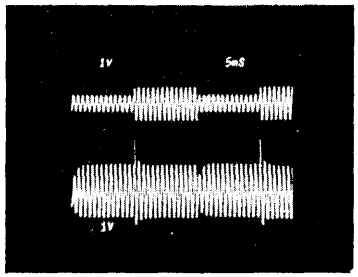
Input
0dBm, +6.0 dBm (1 kHz)

Output



Input
−10dBm, −4.0 dBm (1 kHz)

Output



National Semiconductor

Active Filters

AF120 Generalized Impedance Converter, GIC

General Description

The AF120 contains a pair of operational amplifiers and four precision thin film resistors connected as shown below. A gyrator may be formed by adding one external capacitor; or a frequency dependent negative resistance FDNR may be formed by adding two external capacitors. In the gyrator mode, $Z_{IN} \propto j\omega C$, which is equivalent to a grounded inductor. In the FDNR mode, $Z_{IN} \propto -1/\omega^2 C1C2$. The AF120 may also be used in pairs to form ungrounded inductors or inductor networks. Thus, with appropriate transformations, the GIC makes possible an active realization of any low-frequency ladder filter network. The advantage of ladder filters being, of course, that they exhibit lower sensitivity to component variations than any other type of filter realization. Temperature coefficient of the internal resistors is equal and opposite in sign to that of polystyrene capacitors, thus RC products exhibit approximately zero TC.

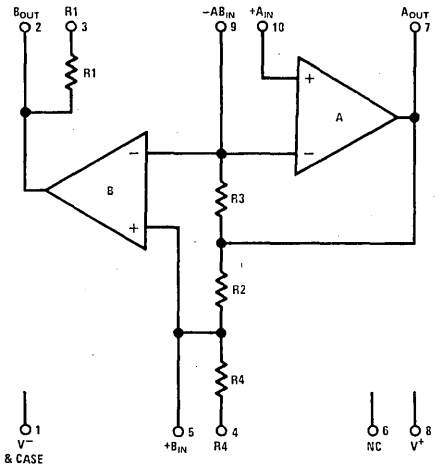
Features

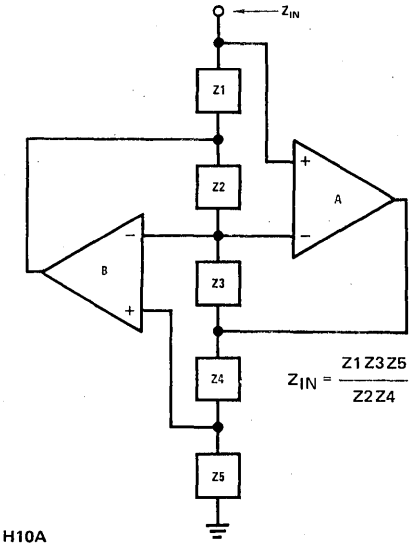
- Matched internal resistors 7500Ω ±0.1%
- Resistor TC = +110 ±30 ppm/°C
- Supply voltage ±5 to ±18V
- Input impedance 7500Ω

Applications

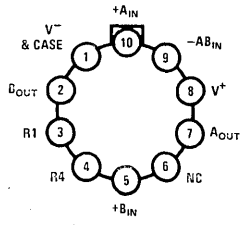
- Gyrator, $Z \propto s$
- Frequency dependent negative resistance, $Z \propto 1/s^2$
- Use in low-frequency active ladder filter networks

Schematic and Connection Diagrams





Metal Can Package H10A
AF120CH
AF120H



TOP VIEW

Absolute Maximum Ratings

Supply Voltage, V_S	±18V
Power Dissipation, T_A = 25°C	500 mW
Derate 18 mW/°C above 60°C	
Operating Temperature, T_A	
AF120	−55°C to +125°C
AF120C	−25°C to +85°C
Storage Temperature, T_{STG}	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

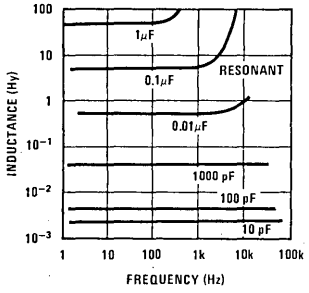
Electrical Characteristics $T_A = 25°C$, $V_S = \pm 5.0V$ to $\pm 15V$, except as noted

PARAMETER		CONDITIONS	AF120			AF120C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$\|Z_{IN}\|$	Input Impedance	*(Figure 1)*	7425	7500	7575	7350	7500	7650	Ω
θ	Phase (Note 1)		89.5	90	90.5	89	90	91	DEG.
V_{OS}	DC Voltage measured at Input Terminal			1	8		1	10	mV
	R1, R2, R3, R4		7485	7500	7515	7470	7500	7530	Ω
	R2/R3		0.999	1.000	1.001	0.998	1.000	1.002	
TC	Resistor Temp. Coeff.		80	110	140	50	110	170	ppm/°C
V_O	Op Amp Output Voltage	$V_S = \pm 15V$, $R_L = 2k$	±10	±13		±10	±13		V
I_{SC}	Op Amp Short-Circuit Output Current	$V_S = \pm 15V$		20			20		mA
I_S	Supply Current	$V_S = \pm 15V$		3	5.6		3	5.6	mA

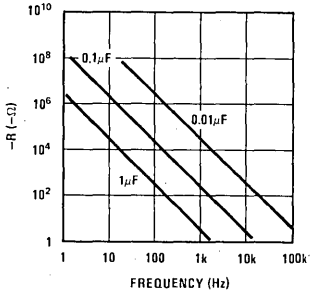
Note 1: 90° indicates that connection actually simulates a pure inductor.

Typical Performance Characteristics

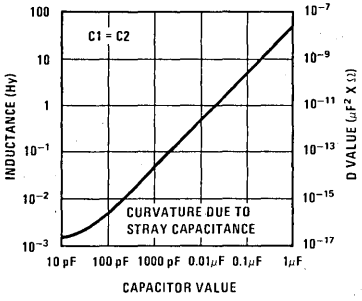
Equivalent Inductance vs Frequency



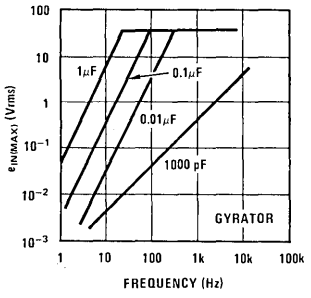
FDNR Value vs Frequency



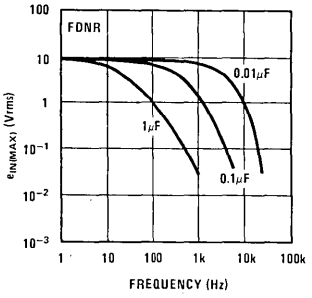
Equivalent L and D vs Capacitor Values



Maximum Terminal Voltage vs Frequency



Maximum Terminal Voltage vs Frequency



Applications Information

The generalized impedance converter GIC is a versatile tool for realization of inductive components in low-sensitivity filters. The driving point impedance is $Z_i(s) = k(s)\ Z_L(s)$. The input impedance of the AF120 is

$$Z_i = \frac{Z1\,Z3\,Z5}{Z2\,Z4} \quad \text{(Refer to } \textit{Figure 2}\text{)}$$

which reduces to

$$Z_i = \frac{Z1\,Z5}{Z2}$$

since Z3 = R3, Z4 = R2 and R2 = R3. No more than one or two of Z1, Z2 and Z5 may be external capacitors. Internal resistor R4 is available for use as Z5, and internal resistor R1 may be used as either Z1 or Z2. External resistors of other values may be substituted for R1 or R4 if proper attention is paid to temperature coefficients. The TC of internal resistors is +110 ±30 ppm/°C to compensate for the TC of polystyrene capacitors.

The AF120 may be used for the following impedance conversions:

Positive impedance converter (PIC) — k(s) is positive and real

$$Z2 = R1,\ Z5 = R4,\ k = R4/R1 = +1,$$

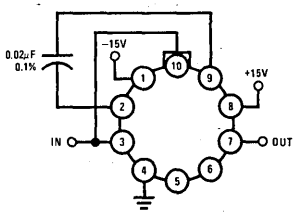
$$Z_i(\omega) = Z1(\omega) \quad \text{(trivial case)}$$

Positive impedance inverter (PII) — k(s) is positive and real

$$Z1 = R1,\ Z5 = R4,\ k = R1\,R4 = (7500)^2$$

$$Z_i(\omega) = R1\,R4/Z2(\omega)$$

If Z2 is an external capacitor, then $Z_i(\omega) = R1\,R2j\omega C$, and $Z_i(s) \propto (s)$



$V_{IN} \leq 1Vrms$ @ 1053 Hz

FIGURE 1. Test Circuit

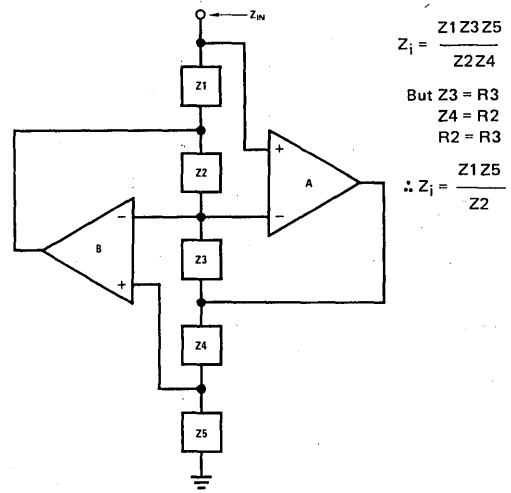


FIGURE 2. GIC Circuit

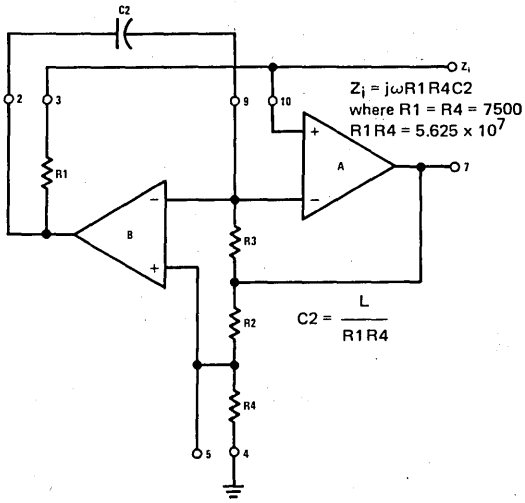


FIGURE 3. Gyrator (Inductive Element)

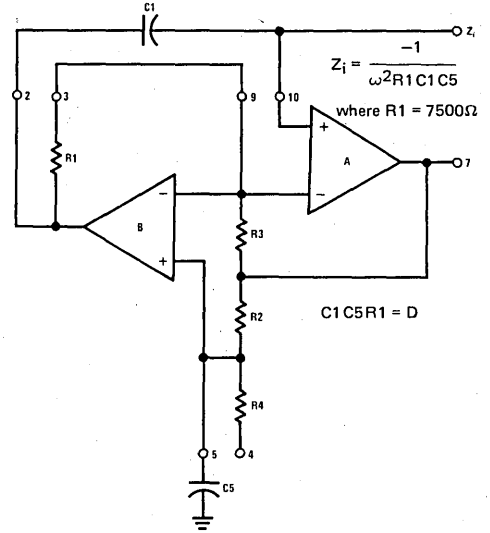
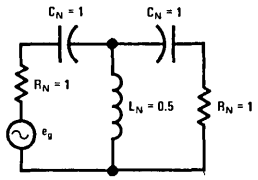
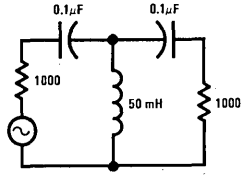


FIGURE 4. FDNR (D Element)

Applications Information (Cont'd.)

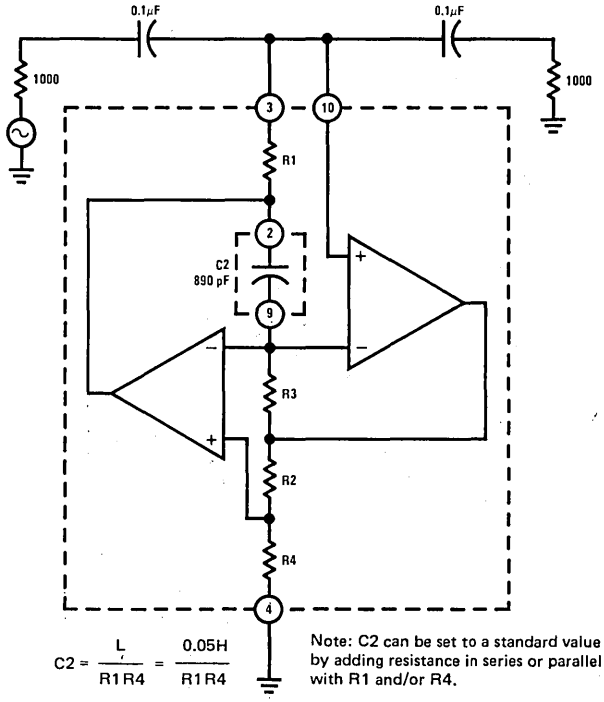


(a) Prototype



$R_O = 1\ k\Omega$
$f_c = 1590\ Hz$
$\omega_c = 10^4$

(b) Filter after Frequency and Impedance Transformation



(c) GIC Active Realization

FIGURE 5. Third-Order Butterworth Highpass Filter

Frequency dependent negative resistance (FDNR)

$$Z2 = R1,\ k = 1/R1$$
$$Z_I = Z1(\omega)Z5(\omega)/R1$$

If Z1 and Z5 are both external capacitors, then $Z_I = -1/R1\omega^2C1C5$, and $Z_I(s) \propto -1/s^2$

GIC elements are especially useful for active simulation of low-sensitivity passive ladder filters. Symmetrically terminated ladder filters exhibit an exceptionally low sensitivity to changes in network element value; in fact, they exhibit the lowest sensitivity of any filter type. This means that practical realization of multistage filter functions may be achieved with moderate tolerance components, and that component shifts due to temperature variations will have minimal effect on the filter transfer function. Additionally, a great deal of ladder filter design information exists in handbook form; hence the value of the GIC as a network element. Several examples are given on the following pages for the realization of filters with grounded inductors, with ungrounded inductors, and with both grounded and ungrounded inductors.

Highpass Filter (with Grounded Inductors)

Figure 5 shows the development of the GIC active realization of the prototype ladder filter of *Figure 5(a).* The network is first designed with normalized values for all components. Next, the component values are transformed according to the desired characteristic impedance and cutoff frequency of the filter. To transform from prototype normalized values where $R_O = 1$ and $\omega_c = 1$,

$$\left.\begin{array}{l}\text{Multiply all R and L by } R_O \\ \text{Divide all C by } R_O \\ \text{Divide all L and C by } \omega_c\end{array}\right\} \text{ to obtain } \left\{\begin{array}{l}R = R_O R_N \\ L = R_O L_N/\omega_c \\ C = C_N/R_O\omega_c\end{array}\right.$$

where N subscripts indicate original normalized values.

Lowpass Filter (with Ungrounded Inductors)

Since the simple GIC realization of an inductor results only in a grounded inductor, a network transformation is necessary in order to use the GIC in a lowpass filter. *Figure 6* shows the frequency and impedance transformation of the prototype lowpass filter, followed by a 1/s impedance transformation. When this 1/s transformation is made, the performance of the filter is unchanged, therefore the transformation is valid. The

Applications Information (Cont'd.)

resultant circuit shown in *Figure 6(c)* allows the realization of the prototype ungrounded inductor circuit with a grounded D element (FDNR). To make the 1/s transformation, each impedance is multiplied by 1/s so that

each R is replaced by a $C = 1/\omega_c R$,

each L is replaced by an $R = \omega_c L$, and

each C is replaced by a $D = C/\omega_c$.

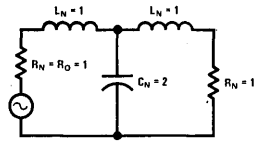
Examination of the GIC realization of an FDNR in *Figure 4* will reveal that a resistive path from FDNR terminal 10 must exist to ground in order to supply bias current to the internal amplifiers. The circuit of *Figure 6(c)* is, therefore, incomplete as no resistive path exists from D element to ground. If a large R were shunted across D, that R would appear in *Figure 6(b)* as an inductor across the C. The solution is to place large R's across the C's in *Figure 6(c)* which appear as large inductors across R_O of *Figure 6(b)*, and thus do not significantly affect the transfer function except near $\omega = 0$. The resultant network appears in *Figure 6(d)*. The transfer function at $\omega = 0$ is $T(0) = 0.5$, therefore resistors R_A and R_B must be chosen to affect this value. Then $T(0) = 0.5 = R_B/(R_A + R_B + 2R_O)$.

The GIC realization of the lowpass filter, complete with low-frequency compensation appears in *Figure 6(e)*. Note again, that C1 and C5 can be varied or can be unequal just so long as C1C5R1 = D. Also note that in the final transformation of *Figure 6(c)*

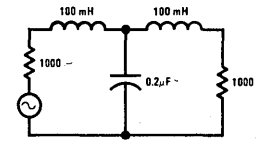
$D = C_N/\omega_c^2 R_O$

$R = R_O L_N$

$C = 1/\omega_c R_O R_N$

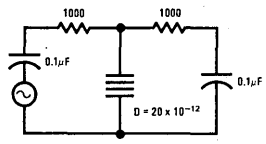


(a) Prototype

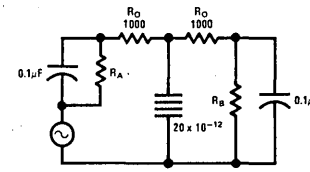


$R_O = 1\ k\Omega$
$f_c = 1590\ Hz$
$\omega_c = 10^4$

(b) Filter after Frequency and Impedance Transformation

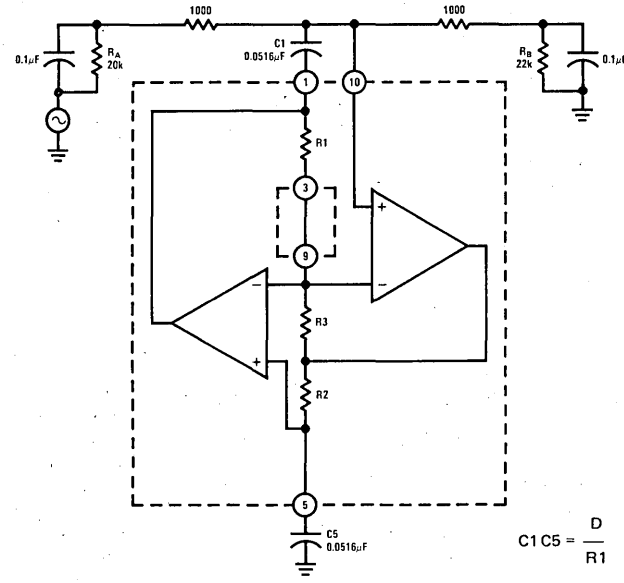


(c) Filter after 1/s Transformation



$R_A, R_B >> R_O$
$R_B = R_A + 2R_O$

(d) Final Circuit with Low-Frequency Compensation



$C1\,C5 = \frac{D}{R1}$

(e). Active Realization

FIGURE 6. Third-Order Butterworth Lowpass Filter

Applications Information (Cont'd.)

GIC Embedding

Ungrounded inductors may be simulated by embedding an ungrounded resistor between two GIC's as shown in *Figure 7(a)*. Actually, the embedded element may be any 2 or 3-terminal network and the GIC may be given any of its realizable impedance transformations Z(s), $Z(s^{-2})$, $Z(s^{-1})$ or $Z(s^2)$*.

Bandpass Filter (with Grounded and Ungrounded Inductors)

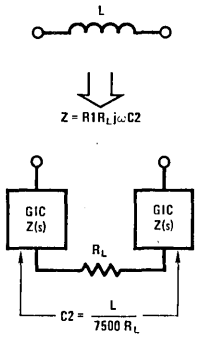
Direct RC active simulation of this filter requires the use of GIC embedding techniques (as described above) because there is no transformation which will eliminate all ungrounded L or D elements. *Figure 8* shows the step-by-step realization of a 6-pole Butterworth bandpass filter.

The filter circuit of *Figure 8(c)* constructed with AF120 and with R and C values shown performed as indicated in the plot of *Figure 9*. Note that the band center and cutoff frequencies occur at the design points as indicated by the phase measurements at 0°C and ±135°C.

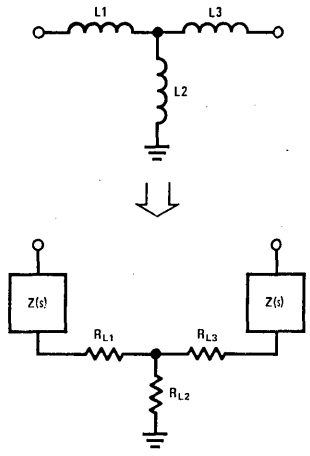
The circuit of *Figure 8(c)* is simplified with a shorthand notation for the GIC's. This shorthand circuit is equivalent to the GIC as shown in *Figure 10*.

The final circuit for the bandpass filter of *Figure 8* contains six capacitors, one for each pole of the 6-pole network. This circuit then contains a minimum number of reactive elements to satisfy the prototype design. A dc path to ground exists for all GIC elements in this design so no additional resistors are needed for dc compensation. Note also that even though one and two percent components have been used throughout the circuit and the $C_D C_C$ product is in error by 3%, performance is as designed. It should be clear from this exercise that ladder networks of virtually any complexity may be realized using the AF120 GIC circuit.

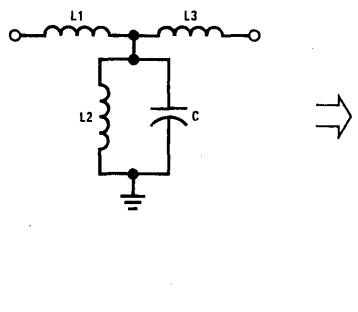
*$Z(s^2)$ is not realizable with the AF120.



(a) Ungrounded Inductor



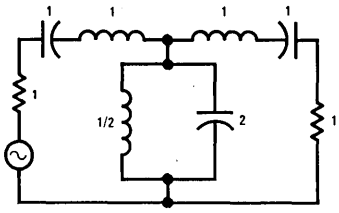
(b) Grounded T Network



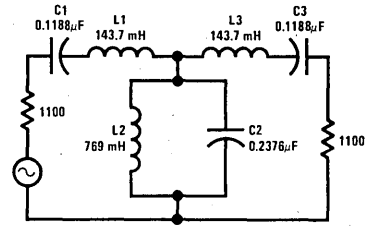
(c). GIC Realization of Complex T Network

FIGURE 7. GIC Realization of Ungrounded Inductors and T Networks

Applications Information (Cont'd.)

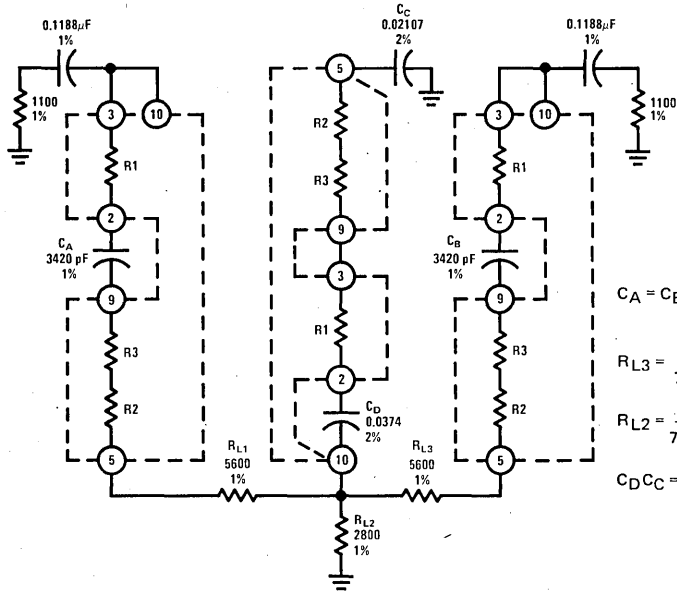


(a) Prototype



$R_O = 1100\Omega$
$f_O = 1218$ Hz
$f_L = 752.8$ Hz
$f_H = 1970.8$ Hz

(b) Filter after R_O and ω_O Transformations



$$C_A = C_B = \frac{L1}{7500\ R_{L1}} = 3420\ pF$$

$$R_{L3} = \frac{L3}{7500\ C_A} = 5600\Omega$$

$$R_{L2} = \frac{L2}{7500\ C_A} = 2800\Omega$$

$$C_D C_C = C_A C2 = 812 \times 10^{-6}\ \mu F^2$$

(c) GIC Realization

FIGURE 8. 6-Pole Butterworth Bandpass Filter

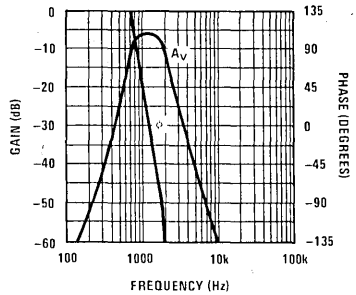
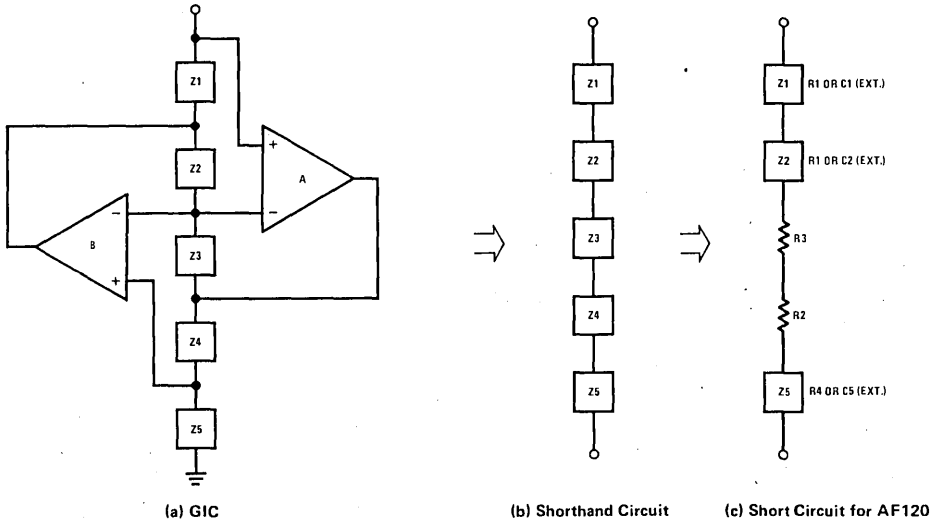


FIGURE 9. Gain and Phase Transfer Functions of the Filter of Figure 8(c).

Applications Information (Cont'd)



(a) GIC (b) Shorthand Circuit (c) Short Circuit for AF120

FIGURE 10. Development of GIC Shorthand Circuit

National Semiconductor

AF121, AF122 DTMF Bandpass Filters

General Description

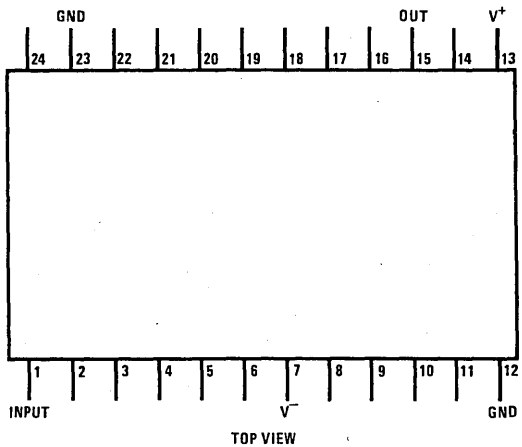
The AF121 and AF122 are 6th order elliptic bandpass filters designed for use with digital DTMF detectors. These filters are compatible with tone detector circuits such as the Rockwell CRC8030 and the Mostek MK5102 DTMF digital receivers. The filters provide 40 dB separation between the high and low frequency signaling groups and the dial tone frequencies. The bandpass feature eliminates the need for a separate dial tone reject filter.

Features

- Compatible with Rockwell CRC8030 and Mostek MK5102
- Gain 0 ±0.5 dB
- Ripple 2 dB peak to peak
- Input Impedance 175 kΩ min
- Power Supply ±5V to ±18V

Connection Diagram

Dual-In-Line Package



TOP VIEW

Unspecified pins are for internal use only and should not be used for external connection.

Order Number
AF121-1CJ, AF121-2CJ
AF122-1CJ, AF122-2CJ

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation	1W
Input Voltage	±100V
Output Short Circuit Duration	Infinite
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−25°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_S = \pm12V$ to $\pm15V$, $T_A = 0°C$ to $70°C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	AF121-2CJ			AF121-1CJ			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
A_O	Gain	f = 800 Hz	−0.5	0	0.5	−1.5	0	1.5	dB
A_{MAX}	Ripple (Pk to Pk)	697 Hz ≤ f ≤ 950 Hz		1.5	2			5	dB
A_{MIN}	Rejection	f ≤ 500 Hz, f ≥ 1200 Hz	−40			−38			dB
Z_{IN}	Input Impedance		175			175			kΩ
Z_{OUT}	Output Impedance			1			1		Ω
V_{OS}	DC Offset			30	80		30	130	mV
P_D	Power Dissipation	$T_A = 25°C$, $V_S = \pm15V$		165			165		mW
					270			270	mW
V_{CC}	Power Supply	$V_{CC} = (V^+) - (V^-)$	10		36	10		36	V_{DC}

SYMBOL	PARAMETER	CONDITIONS	AF122-2CJ			AF122-1CJ			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
A_O	Gain	f = 1405 Hz	−0.5	0	0.5	−1.5	0	1.5	dB
A_{MAX}	Ripple (Pk to Pk)	1209 Hz ≤ f ≤ 1633 Hz		1.2	2			4	dB
A_{MIN}	Rejection	f ≥ 2200 Hz, f ≤ 950 Hz	−40			−38			dB
Z_{IN}	Input Impedance		175			175			kΩ
Z_{OUT}	Output Impedance			1			1		Ω
V_{OS}	DC Offset			20	70		20	120	mV
P_D	Power Dissipation	$T_A = 25°C$, $V_S = \pm15V$		165			165		mW
					270			270	mW
V_{CC}	Power Supply	$V_{CC} = (V^+) - (V^-)$	10		36	10		36	V_{DC}

Typical Performance Characteristics

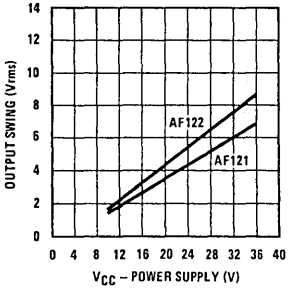


FIGURE 1. Output Swing vs Power Supply Voltage

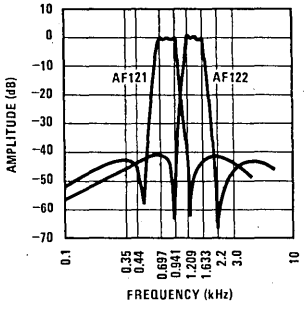


FIGURE 2. Typical Amplitude Response

Applications Information

The DTMF receivers used to detect signals from push-button telephones require at least 2 filters. In recent years single chip integrated circuits have been designed to detect the signaling tones and perform the logic functions required in DTMF receivers. These receivers still require input band splitting filters to separate the 2 input tones. Two such detectors are the Rockwell CRC8030 and the Mostek MK5102. The National Semiconductor AF121-2CJ and AF122-2CJ are bandpass filters which provide 40 dB separation between the bands. The AF121 and AF122 filters are 6th order elliptic bandpass filters. The AF121-2CJ and AF122-2CJ have 0 dB ± 0.5 dB gain at the center of the pass band with a maximum ripple of 2 dB peak to peak. The stop band rejection is greater than 40 dB. *Figure 2* shows the typical amplitude response of the 2 filters.

Figure 3 is the block diagram of a tone receiver system using the AF121 and AF122 to split the input signal into low group and high group signals. The signals are next passed through AGC circuits which provide amplitude correction to equalize the signal level in the 2 channels and to provide a known level to the limiters. The limiters have a threshold setting circuit such that signals which exceed the threshold will appear at the inputs of the digital tone detector.

The input bandpass filters reject the dial tone signals, when present, and provide enough rejection to noise and extraneous signals to assure a low error rate system. The AGC amplifiers equalize the tone levels in each band. This allows the detection of signals with large twists. The AGC amplifiers also provide up to 24 dB gain to the tone signal, allowing operation over a wide range of input levels.

The National Semiconductor AF104 AGC amplifier is a linear fixed gain device with an input attenuator controlled by the average output amplitude. Additional circuitry provides fast recovery when a burst of signal is applied to the input. The typical recovery time of the circuit is one half cycle of the input frequency.

The limiters can be built of discrete components using a comparator such as the National Semiconductor LM339. The limiter threshold can be set by using the internal reference of the AF104, which is a +5V regulator. This provides a stable threshold independent of the system power supply. Since none of the analog circuits are dependent on the power supply for a reference and all the circuits have good common-mode rejection, a simple power supply is all that is required as long as the supply voltages remain greater than ±9V.

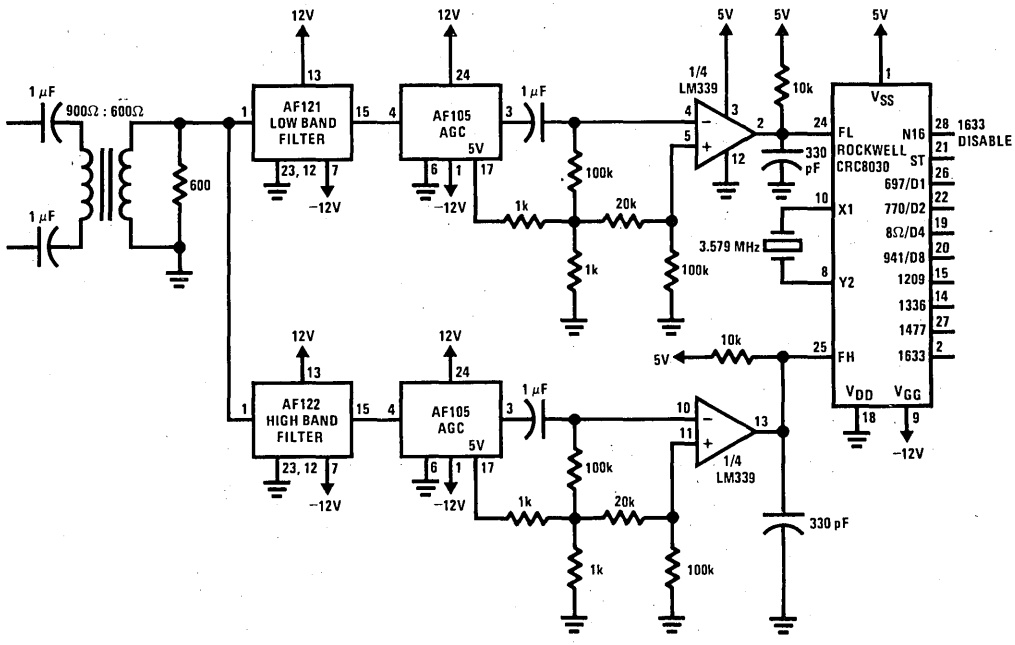


FIGURE 3. Tone Receiver Block Diagram Using Rockwell CRC8030

Applications Information (Continued)

Figure 4 shows a complete circuit for interfacing to Mostek's MK5102. The limiters are formed using a single LM2901 and provide hysteresis to prevent oscillations at the input of the decoder.

The AF121-1CJ and AF122-1CJ are DTMF band splitter filters for applications with less stringent electrical requirements.

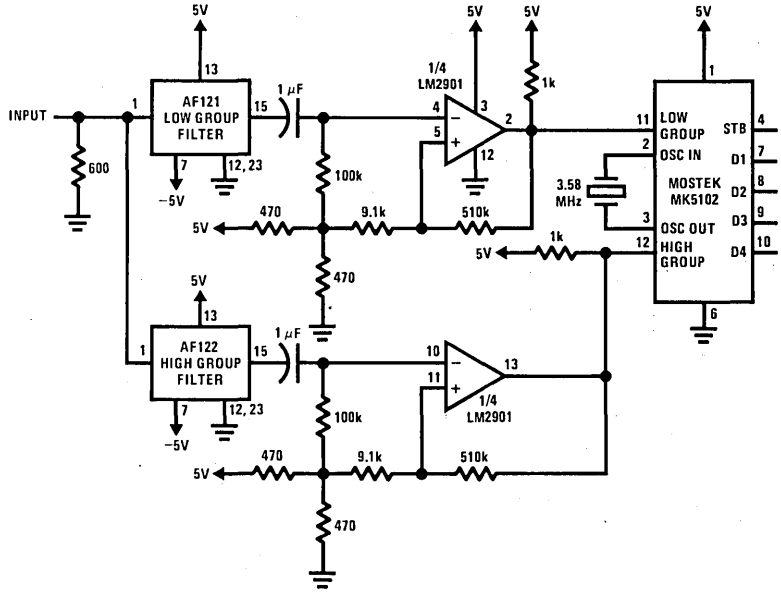


FIGURE 4. Tone Receiver Circuit Using Mostek MK5102

National Semiconductor

AF132 Dual PCM Transmit/Receive Filter

General Description

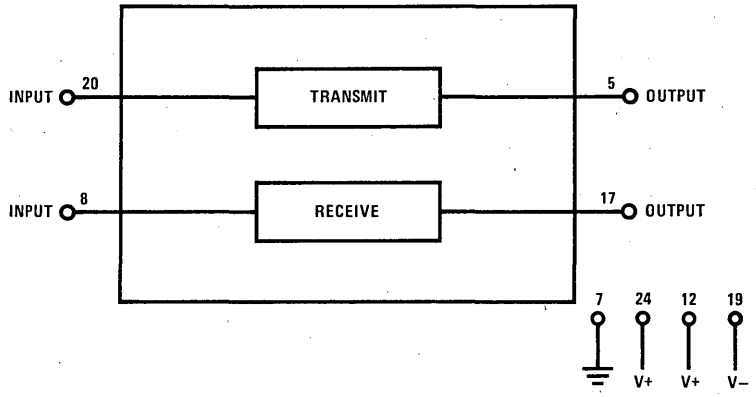
The AF132 filter circuits are specifically designed to meet the less stringent requirements of the PBX and PABX telephone industry. Special attention has been given not only to the electrical filtering requirements, but also to the physical size, environmental, life, and cost requirements.

The filters are manufactured using a well understood and dependable thick film technology using laser trimmed resistors and the highest quality components.

Features

- No external components required
- Consistent uniform product
- Insensitive to time and temperature
- Wide power supply range ±9.0V to ±15V

Connection Diagram



Ceramic Dual-In-Line
Package HY24A
AF132CJ

Absolute Maximum Ratings

Supply Voltage	±18 V
Power Dissipation	1 W/Package
Input Voltage	±18 V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	0° to +70°C
Storage Temperature Range	−25°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°

Electrical Characteristics

Unless otherwise noted, these specifications apply over the temperature range from 0°C to +70°C and are tested using ±12° V power supplies, but are guaranteed for any symmetrical power supply operating between ±9.0 V to ±15 V.

Parameter		Conditions	Transmit			Receive			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
A_O	Voltage Gain	f = 800 Hz	−0.5	0	0.5	−0.36	0.14	0.64	dB
ΔA	Ripple	300 Hz ≤ f ≤ 3000 Hz, (Note 1)		±0.35	±0.5		±0.35	±0.5	dB
A	Gain (Stop Band)	f > 5.3 kHz	−20						dB
A	Gain (Stop Band)	f > 4.6 kHz				−20			dB
e_O	Output Voltage Swing	V_{CC} ± 12 V, R_L = 2k		20		20			V_{P-P}
V_{OS}	Output DC Offset		−100		100	−100		100	mV
Z_{IN}	Input Impendance	DC to 10 kHz, T_A = 25°C	90	100		90	100		kΩ
Z_O	Output Impedance	DC to 10 kHz, T_A = 25°C		0.5	1.0		0.5	1.0	Ω
PSRR	Power Supply Rejection	120 Hz to 3.4 kHz		97			97		dB
		3.4 kHz to 25 kHz		90			90		dB
P_D	Power Dissipation	V_{CC} = ±12 V		135	220				mW
		V_{CC} = ±15 V		190	270				mW

Note 1: For the receive section, ripple is specified as the deviation from the ideal pass band response that would result if the $\frac{\text{SIN}\frac{\pi f}{8000}}{\frac{\pi f}{8000}}$ roll-off characteristics were compensated perfectly, and assumes the inclusion of a sample and hold.

Applications Information

GENERAL

The transmit and receive filters are both third order elliptic low pass filters that have been specifically designed for 8 kHz sampled data systems found in telephone PCM communication systems and some military systems, *(Figure 1)*.

The transmit filter is designed to provide a flat band pass response from DC to 3.0 kHz and attenuate signals above 4.5 kHz to prevent these signals from occuring in the sampled data.

The receive filter is designed to receive the sampled data in order to reconstruct the original analog signal. Because the information has been processed through a sample and hold technique, the amplitude information in the band pass has a characteristic SIN X/X response. The purpose of the receive filter is to provide the necessary response to compensate for the input signal frequency response and restore the amplitude information to a flat band pass characteristic.

The block diagram in *Figure 2*, indicates the basic construction of the AF132.

All other pins not shown connected should be left open.

PROVIDING LOW FREQUENCY ROLL-OFF

In most systems, it is necessary to have a low frequency high pass filter in front of the transmit filter to attenuate 60 Hz and 120 Hz. Some attenuation can be achieved by capacitively coupling the input signal, with the proper value of capacitor, C, selected to trade off 60 Hz attenuation with the amount of band pass

Applications Information (Continued)

flatness near 300 Hz. The capacitor is easily selected since the input impedance (resistive only) is specified. A second, and more desirable solution, is shown in *Figure 4*. This filter makes use of the AF100 as a second order high pass filter. It provides 22 dB of attenuation of 60 Hz, and has less than 0.03 dB effect on the band pass characteristics at 300 Hz.

TESTING

The circuit in *Figure 5* is typical of that used by National Semiconductor to test the active filters. In testing and in actual application, the filter must be driven from a low impedance source ($R_S \leq 50\Omega$).

CODEC

National Semiconductor presently manufactures two monolithic circuits designed to perform the entire companding coder/decoder function. Before proceeding with your design, please contact National for information about these devices, the MM58100 and the LF2700.

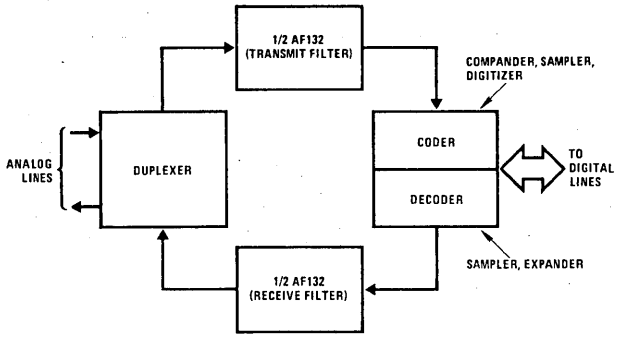


FIGURE 1. PCM Block Diagram

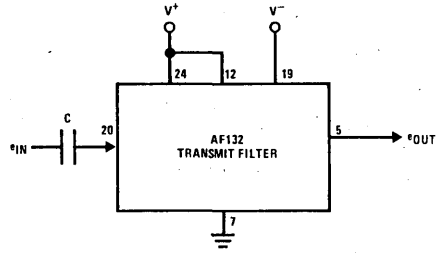
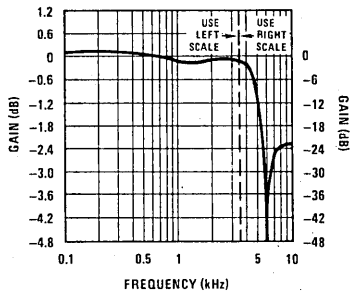


FIGURE 2. Capacitive Coupling to Provide Low Frequency Roll-Off

AF132 TRANSMIT FILTER SECTION

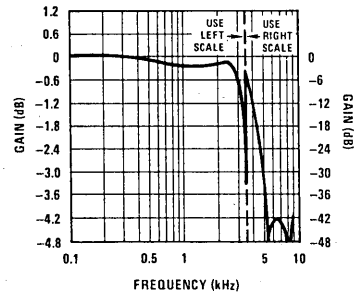
The transmit section is a third order elliptic low pass filter designed to provide a flat amplitude response from 300 Hz to 3.0 kHz, and 20 dB or more attenuation of signals above 4.5 kHz.



Transmit Filter

AF132 RECEIVE FILTER SECTION

The receive section is a third order elliptic low pass filter designed to receive PCM information. Because this information has been transmitted in a sampled data PCM system, the amplitude information has been degraded by the inherent SIN X/X sampling function. The receive filter approximates the required function that is necessary to compensate the frequency response and restore a flat band pass response.



Receive Filter

Applications Information (Continued)

FREQUENCY	ATTENUATION
60 Hz	−22 dB
120 Hz	- 6 dB
180 Hz	−1.5 dB
300 Hz	−0.03 dB

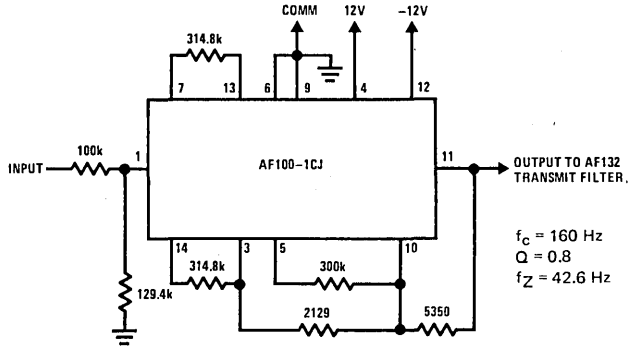


FIGURE 3. Providing 60 Hz Attenuation

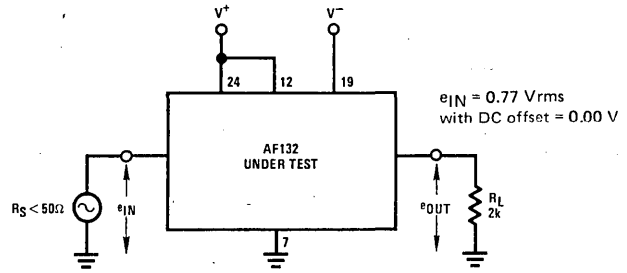


FIGURE 4. Test Circuit

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National Semiconductor

AF133/AF134 PCM Transmit/Receive Filters

General Description

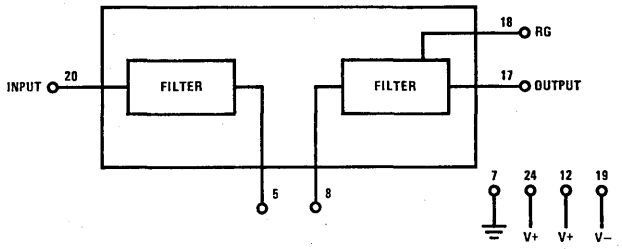
The AF133 and AF134 filter circuits are specifically designed to meet the stringent requirements of the telephone industry. Special attention has been given not only to the electrical filtering requirements of the D3 channel bank, but also to the physical size, environmental, life and cost requirements.

The filters are manufactured using a well understood and dependable thick film technology using laser trimmed resistors and the highest quality components.

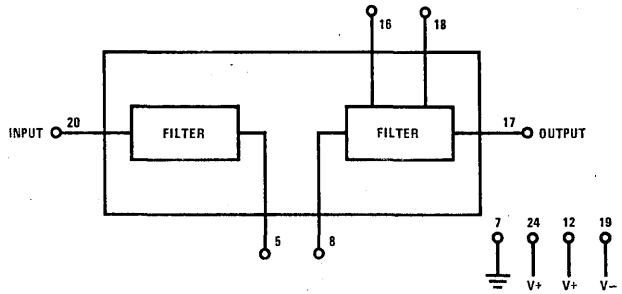
Features

- No external components required
- Active laser trimmed
- Consistent uniform product
- Insensitive to time and temperature
- Designed for D3 system requirements
- Wide power supply range ±12V to ±15V

Connection Diagram



Ceramic Dual-In-Line Package HY24A
AF133-1CJ
AF133-2CJ



Ceramic Dual-In-Line Package HY24A
AF134-1CJ
AF134-2CJ

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation	1W/Package
Input Voltage	±18V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−25°C to +100°C

Electrical Characteristics

Unless otherwise noted, these specifications apply over the temperature range from 0°C to +70°C and are tested using ±12V supplies, but are guaranteed for any symmetrical supply operation between ±12V to ±15V.

AF133 Transmit Filter

SYMBOL	PARAMETER	CONDITIONS	AF133-1			AF133-2			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE									
	Voltage Gain	(Note 2)							
A		f = 3.4 kHz	−1.5	−0.6	0	−0.9	−0.6	0	dB
A		f = 4 kHz		−16	−14		−16	−15	dB
A		f ≥ 4.5 kHz		−33	−30		−33	−32	dB
ΔA	Pass Band Ripple	300 Hz ≤ f ≤ 3 kHz		±0.08	±0.3		±0.08	±0.125	dB
Δt	Differential Delay	1 kHz ≤ f ≤ 2.6 kHz		60	90		60	80	μs
$\Delta A_O/\Delta T$	Gain Stability with Temperature	f = kHz, e_{IN} = 0.1 Vrms		0.0015			0.0015		dB/°C
$\Delta A_O/\Delta t$	Gain Stability with Time	f = 1 kHz, e_{IN} = 0.1 Vrms		0.0005			0.0005		dB/Yr
THD	Distortion	f = 1 kHz, e_{IN} = 0.1 Vrms		0.1	0.5		0.1	0.5	%
e_n	Output Noise Voltage	10 Hz to 50 kHz, e_{IN} = 0V, T_A = 25°C		150	250		150	250	μVp-p
e_o	Output Voltage Swing	V_{CC} = ±12V, R_L = 2k, A = A_O, (Note 2)	10	15		10	15		Vp-p
V_{OS}	Output DC Offset		−150		150	−75		75	mV
Z_{IN}	Input Impedance	DC to 10 kHz, T_A = 25°C	100k			100k			Ω
Z_o	Output Impedance	DC to 10 kHz, T_A = 25°C		0.5	1		0.5	1	Ω
PSRR	Power Supply Rejection	120 Hz to 3.4 kHz		97		97			dB
		3.4 kHz to 25 kHz		90		90			dB
P_D	Power Dissipation	V_{CC} = ±12V		135	220		135	220	mW
		V_{CC} = ±15V		190	270		190	270	mW

Note 1: The voltage gain may be adjusted. Refer to application discussion.
Note 2: The AF133 requires an external gain resistor, (R = 133k typ). All gain measurements assume gain at DC set for 0 dB at 1 kHz.

Electrical Characteristics

AF134 Receive Filter

SYMBOL	PARAMETER	CONDITIONS	AF134-1			AF134-2			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE									
	Voltage Gain	(Notes 1 and 2)							
		f = 1 kHz	−0.08	0.22	0.52	0.095	0.22	0.345	dB
A_o		f = 3.4 kHz	−1.2	−0.6	0	−0.9	−0.6	0	dB
A		f = 4 kHz		−12	−10		−12	−11	dB
A		f > 4.5 kHz		−25	−24		−26	−25	dB
A		f = 8 kHz		−31	−30		−31	−30	dB
ΔA	Pass Band Ripple	300 Hz ≤ f ≤ 3 kHz, (Note 2)	−0.3		0.3	−0.125	0	0.125	dB
Δt	Differential Delay	1 kHz ≤ f ≤ 2.6 kHz		80	90		80	90	μs
$\Delta A_o/\Delta T$	Gain Stability with Temperature	f = 1 kHz, e_{IN} = 0.1 Vrms		0.0015			0.0015		dB/°C
$\Delta A_o/\Delta t$	Gain Stability with Time	f = 1 kHz, e_{IN} = 0.1 Vrms		0.0005			0.0005		dB/Yr
THD	Distortion	f = 1 kHz, e_{IN} = 0.1 Vrms		0.1	0.5		0.1	0.5	%
e_n	Output Noise Voltage	10 Hz to 50 kHz, e_{IN} = 0V, T_A = 25°C		150	250		150	250	μVp p
e_o	Output Voltage Swing	V_{CC} = ±12V, R_L = 2k	10	15		10	15		Vp-p
V_{OS}	Output DC Offset	V_{IN} = 0V, T_A = 25°C	−150		150	−75		75	mV
Z_{IN}	Input Impedance	DC to 10 kHz, T_A = 25°C	100k			100k			Ω
Z_o	Output Impedance	DC to 10 kHz, T_A = 25°C		0.5	1		0.5	1	Ω
PSRR	Power Supply Rejection	120 Hz to 3.4 kHz		97		97			dB
		3.4 kHz to 25 kHz		90		90			dB
P_D	Power Dissipation	V_{CC} = ±12V		135	220		135	220	mW
		V_{CC} = ±15V		190	270		190	270	mW

Note 1: The voltage gain may be adjusted. Refer to application discussion.

Note 2: For the AF134, the pass band ripple specifications do not refer to the AF134 itself. This specification is the deviation from the ideal band pass response that would result if the $\left[\frac{\sin\frac{\pi f}{8000}}{\frac{\pi f}{8000}}\right]$ roll-off characteristic were compensated perfectly, and assumes the inclusion of an ideal sample and hold.

Applications Information

GENERAL

The AF133 and AF134 are both fifth order elliptic low pass filters that have been specifically designed for 8 kHz sampled data systems found in telephone PCM communication systems and some military systems, *(Figure 1)*.

The AF133 transmit filter is designed to (a) provide a very flat band pass response from DC to 3.2 kHz, (b) attenuate signals at 4 kHz (1/2 the sampling rate) by at least 16 dB to prevent "aliasing" or "frequency folding" in the sampled data, and (c) attenuate signals above

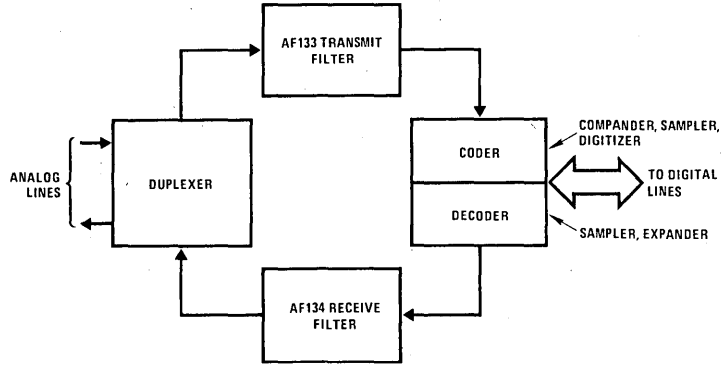


FIGURE 1. PCM Block Diagram

Applications Information (Continued)

4.5 kHz to prevent these signals from occuring in the sampled data.

The AF134 receive filter is designed to receive the sampled data in order to reconstruct the original analog signal. Because the information has been processed through a sample and hold technique, the amplitude information in the band pass has a characteristic (SIN X)/X response. The purpose of the AF134 filter is to provide the necessary response to compensate for the input signal frequency response and restore the amplitude information to a flat pass band characteristic.

GAIN ADJUST

The block diagram in *Figure 2* indicates the basic connection of the AF133.

It consists of 2 separate sections which are connected together externally by the user by jumpering pin 5 to pin 8.

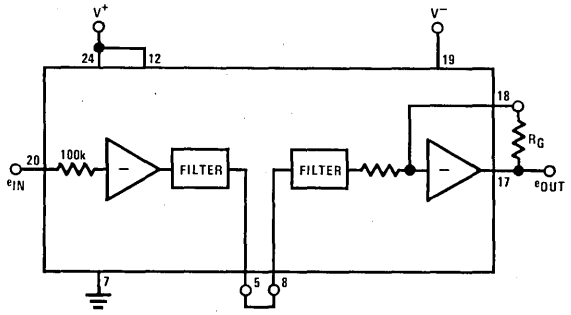
Because it is desirable to have the ability to adjust the voltage gain of the filter, provision has been made to do so *by omitting the gain setting resistor in the feedback path of the output operational amplifier*. For this reason, an external resistor *must* be added between pins 17 and 18 to render the filter operative. The nominal value of the resistor required is 133 kΩ for a 0 dB voltage gain.

All other pins not shown connected should be left open.

Likewise, provision has been made for the user to adjust the gain of the AF134 receive filter as shown in *Figure 3*.

Although R1 and/or R2 are not required for normal operation, it can be easily seen that the addition of R1 (across the internal 100k resistor) will increase the gain, whereas the addition of R2 (across the internal feedback resistor) will decrease the gain.

Obviously, R1 and R2 can be replaced by a single pot with the wiper arm tied to pin 18.



R_G = 133 kΩ for 0 dB gain (nominal)

FIGURE 2. Functional Diagram of AF133

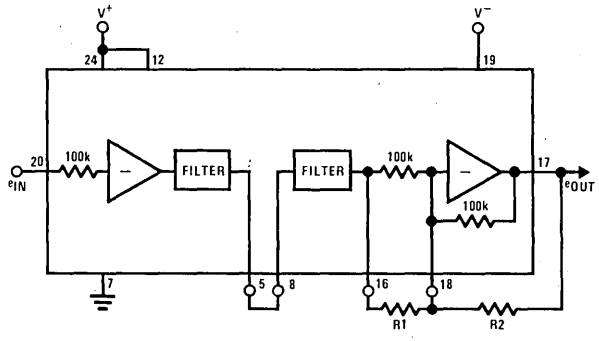


FIGURE 3. AF134 Gain Adjust

PROVIDING LOW FREQUENCY ROLL-OFF

In some systems, it is necessary to have a low frequency high pass filter in front of the transmit filter to attenuate 60 Hz and 120 Hz. Some attenuation can be achieved by capacitively coupling the input signal, with the proper value of capacitor, C, selected to trade off 60 Hz attenuation with the amount of band pass flatness near 300 Hz. The capacitor is easily selected since the input impedance (resistive only) is specified. A second, and more desirable solution, is shown in *Figure 4*. This filter makes use of the AF100 as a second order high pass filter. It provides 22 dB of attenuation of 60 Hz, and has less than 0.03 dB effect on the band pass characteristics at 300 Hz.

Applications Information (Continued)

FREQUENCY	ATTENUATION
60 Hz	−22 dB
120 Hz	−6 dB
180 Hz	−1.5 dB
300 Hz	−0.03 dB

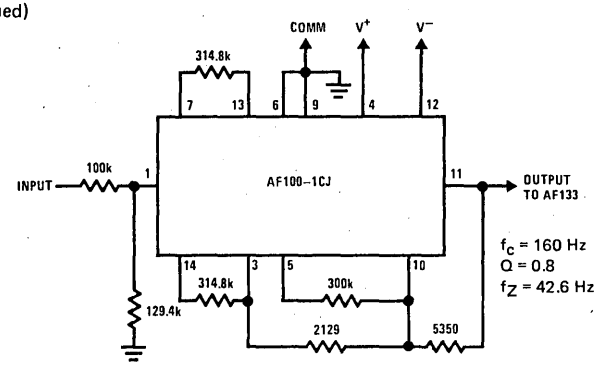


FIGURE 4. Providing 60 Hz Attenuation

TESTING

The circuit shown below is typical of that used by National Semiconductor to test the active filters. In testing and in actual application, the filter must be driven from a low impedance source ($R_S \leq 50\Omega$).

CODEC

National Semiconductor presently manufactures 2 monolithic circuits designed to perform the entire companding coder/decoder function. Before proceeding with your design, please contact National for information about these devices, the MM58100 and the LF2700.

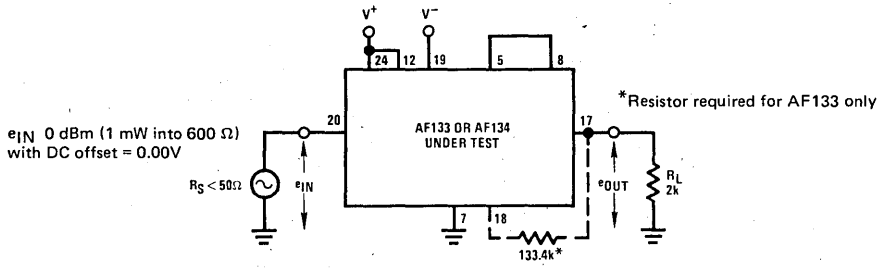


FIGURE 5. Test Circuit

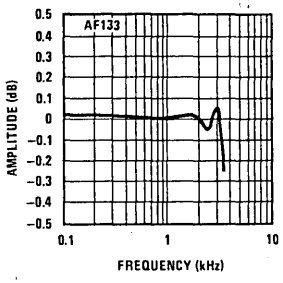


FIGURE 6. AF133 Pass Band Frequency Response

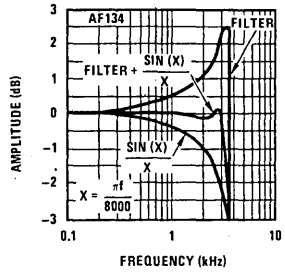


FIGURE 7. AF134 Pass Band Frequency Response

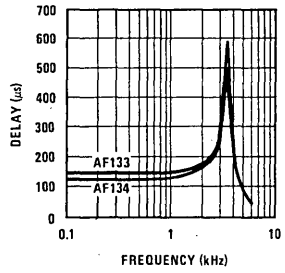


FIGURE 8. Group Delay as a Function of Frequency

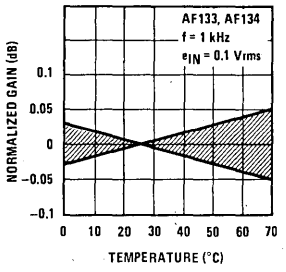


FIGURE 9. Normalized Gain Variation with Temperature

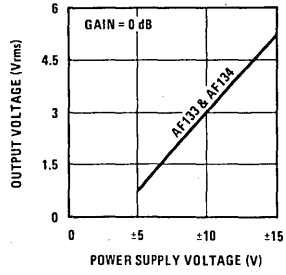


FIGURE 10. Output Voltage Swing vs Power Supply Voltage

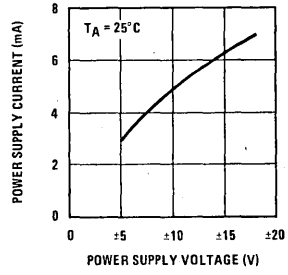


FIGURE 11. Power Supply Current vs Power Supply Voltage

AF150 Universal Wideband Active Filter

General Description

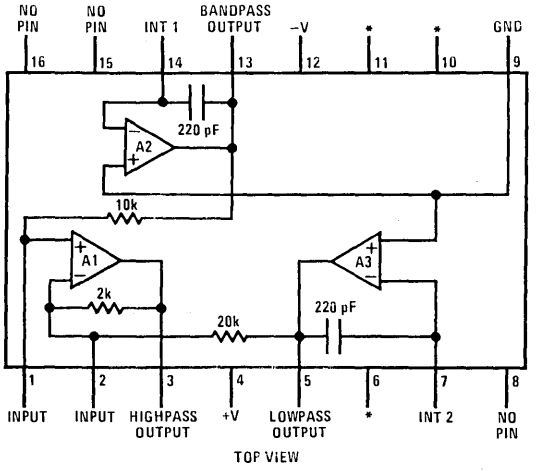
The AF150 wide band active filter is a general second order lumped RC network. Only four external resistors are required to program the AF150 for specific second order functions. Low pass, high pass and band pass functions are available simultaneously at separate outputs. Notch and all pass functions can be formed by summing the outputs with an external amplifier. Higher order filters are realized by cascading AF150 active filters with appropriate programming resistors.

Any of the classical filter configurations, such as Butterworth, Bessel, Cauer and Chebyshev can be formed.

Features

- Independent Q, frequency, gain adjustments
- Low sensitivity to external component variation
- Separate low pass, high pass, band pass outputs
- Inputs may be differential, inverting or non-inverting
- All pass and notch outputs may be formed
- Operates to 100 kHz
- Q range to 500
- Power supply range ±5V to ±18V
- High accuracy ±1% unadjusted
- Q frequency product 2×10^5

Connection Diagram



TOP VIEW

Ceramic Dual-In-Line Package HY13A
AF150-1CJ
AF150-2CJ

***Note:** Internally connected. DO NOT USE.

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	900 mW/Package (500 mW/Amp)
Differential Input Voltage	±36V
Output Short-Circuit Duration (Note 1)	Infinite
Operating Temperature	−25°C to +85°C
Storage Temperature	−25°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Specifications apply for V_S = ±15V, over −25°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Frequency Range	$f_c \times Q \leq 2 \times 10^5$			100k	Hz
	Q Range	$f_c \times Q \leq 2 \times 10^5$			500	Hz/Hz
	f_o Accuracy					
	AF150-1J	$f_c \times Q \leq 5 \times 10^4$, T_A = 25°C			±2.5	%
	AF150-2J	$f_c \times Q \leq 5 \times 10^4$, T_A = 25°C			±1.0	%
$\Delta f_o/\Delta T$	f_o Temperature Coefficient			±50	±150	ppm/°C
	Q Accuracy	$f_c \times Q \leq 5 \times 10^4$, T_A = 25°C			±7.5	%
$\Delta Q/\Delta T$	Q Temperature Coefficient			±300	±750	ppm/°C
PSRR	Power Supply Rejection Ratio		80	100		dB
CMRR	Common-Mode Rejection		80	100		dB
I_{os}	Input Offset Current	T_j = 25°C		3	50	pA
I_B	Input Bias Current	T_j = 25°C		30	200	pA
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	±12		V
I_s	Power Supply Current	V_S = ±15V, T_A = 25°C		15	30	mA

Note 1: Any of the amplifier's outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum package power dissipation will be exceeded.

Applications Information

CIRCUIT DESCRIPTION AND OPERATION

A schematic of the AF150 is shown in *Figure 1*. Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input.

By adding external resistors the circuit can be used to generate the second order transfer function:

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_o = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_o}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(high pass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer function becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(band pass)}$$

Applications Information (Continued)

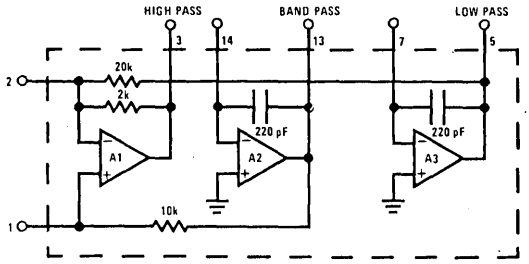


FIGURE 1. AF150 Schematic

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad \text{(low pass)}$$

Using an external op amp and the proper input and output connections, the circuit can also be used to generate the transfer functions for a notch and all pass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals ω_z^2 and a_3 equals 1. The transfer function becomes:

$$T(s) = \frac{s^2 + \omega_z^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad \text{(notch)}$$

In the all pass transfer function $a_3 = 1$, $a_2 = -\omega_o/Q$ and $a_1 = \omega_o^2$. The transfer function becomes:

$$T(s) = \frac{s^2 - \frac{\omega_o}{Q} s + \omega_o^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \qquad \text{(all pass)}$$

The relationships between the generalized coefficients and the external resistors will be found in the appendix. It is not, however, necessary to use these theoretical, if not "messy", equations to solve for the proper external resistor values. In general, it is assumed that the user has knowledge of the frequency and Q of the specific filter he is designing. For higher order filters of various types, the reader is directed to any of the available texts on filters (see bibliography) for information and tables concerning the location of the poles and zeros. Once the specifics of the filter are found from the tables, it is simply a matter of cascading the sections with proper attention to some general guidelines which are included later in the application section.

The following discussion gives a step-by-step procedure for designing filters with several examples given for clarity.

FREQUENCY TUNING

Two equal value frequency setting resistors are required for frequencies above 1 kHz. For lower frequencies, T tuning or the addition of external capacitors is required. Using external capacitors allows the user to go as low in frequency as he desires. T tuning and external capacitors can be used together.

Two resistor tuning for 1 kHz to 100 kHz

$$R_f = \frac{228.8 \times 10^6}{f_o}\ \Omega \qquad (1)$$

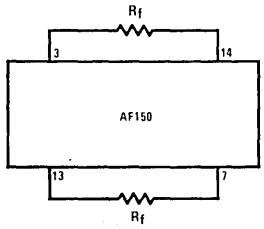
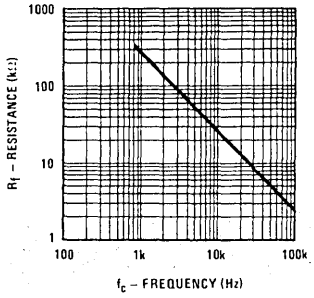


FIGURE 2. Resistive Tuning

GRAPH A. Resistive Tuning



Applications Information (Continued)

T resistive tuning for $f_o < 1$ kHz

$$R_S = \frac{R_T^2}{R_f - 2R_T} \qquad (2)$$

R_f from equation 1.

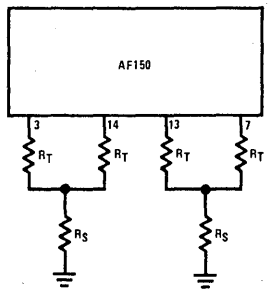
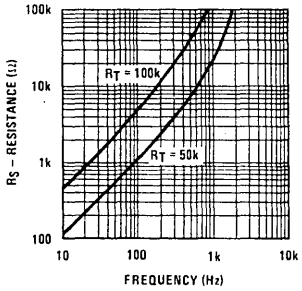


FIGURE 3. T Tuning

GRAPH B. T Tuning



If external capacitors are used for $f_o < 1$ kHz, then equation 3 should be used.

$$R_f = \frac{0.05033}{f_o\,(C + 220 \times 10^{-12})}\ \Omega \qquad (3)$$

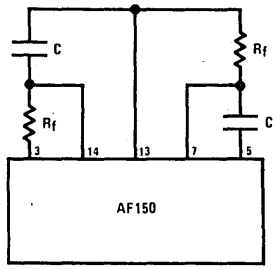


FIGURE 4. Low Frequency RC Tuning

Q DETERMINATION

Setting the Q requires one resistor from either pin 1 or pin 2 to ground. The value of the Q setting resistor depends on the input connection and input resistance as well as the value of the Q. The Q will be inversely proportional to the resistance from pin 1 to ground and directly proportional to resistance from pin 2 to ground.

NON-INVERTING CONNECTION*

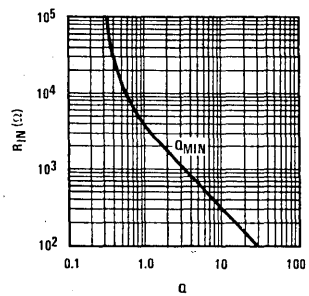
To determine the Q resistor, choose a value of input resistor, R_{IN}, *(Figures 5 and 6)* and calculate Q_{MIN} (graph C).

$$Q_{MIN} = \frac{1 + \frac{10^4}{R_{IN}}}{3.48}$$

If the Q required in the circuit is greater than Q_{MIN}, use the circuit configuration shown in *Figure 5* and equation 4 to calculate R_Q, the Q resistor. If the Q of the circuit is less than Q_{MIN}, use the circuit configuration shown in *Figure 6* and equation 5.

*The discussion of "non-inverting" and "inverting" has to do with the phase relationship between the input port and the *low pass* output port. Refer to *Figure 1* for other output port phase relationships.

GRAPH C. Q_{MIN}, Non-Inverting Input



Applications Information (Continued)

For $Q > Q_{MIN}$ in non-inverting mode:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}} \ \Omega \qquad (4)$$

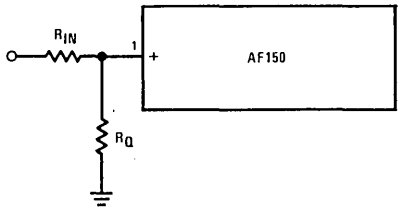
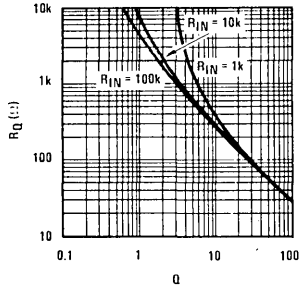


FIGURE 5. Q Tuning for $Q > Q_{MIN}$, Non-Inverting Input

GRAPH D. R_Q for $Q > Q_{MIN}$, Non-Inverting Input



For $Q < Q_{MIN}$ in non-inverting mode:

$$R_Q = \frac{2 \times 10^3}{0.3162 \left(1 + \frac{10^4}{R_{IN}}\right) \frac{}{Q} - 1.1} \ \Omega \qquad (5)$$

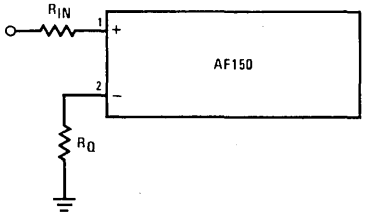
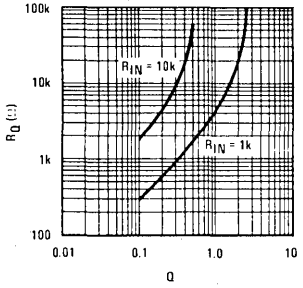


FIGURE 6. Q Tuning for $Q < Q_{MIN}$, Non-Inverting Input

GRAPH E. R_Q for $Q < Q_{MIN}$, Non-Inverting Input



INVERTING CONNECTION*

For any Q in inverting mode:

$$R_Q = \frac{10^4}{3.16Q \left(1.1 + \frac{2 \times 10^3}{R_{IN}}\right) - 1} \ \Omega \qquad (6)$$

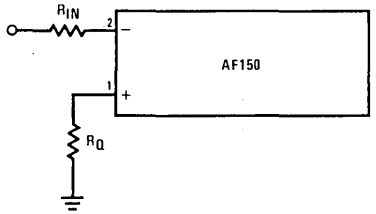
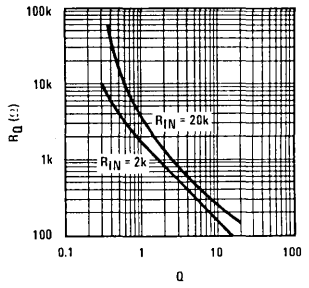


FIGURE 7. Q Tuning, Inverting Input

GRAPH F. Q Tuning, Inverting Input

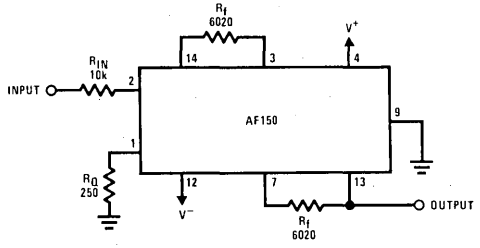


*The discussion of "non-inverting" and "inverting" has to do with the phase relationship between the input port and the *low pass* output port. Refer to *Figure 1* for other output port phase relationships.

DESIGN EXAMPLE

Non-Inverting Band Pass Filter

Center frequency 38 kHz = f_o, 10 Hz/Hz = Q, 10k = R_{IN}.



Using equation 1

$$R_f = \frac{228.8 \times 10^6}{f_o} \ \Omega$$

$$R_f = \frac{228.8 \times 10^6}{38 \times 10^3} = 6020\Omega$$

Applications Information (Continued)

Using equation 6

$$R_Q = \frac{10^4}{3.16Q\left(1.1 + \frac{2 \times 10^3}{R_{IN}}\right) - 1} \ \Omega$$

$R_Q = 250\Omega$

From equation 33, the center frequency gain is found to be 6.3 V/V (16 dB). If the center frequency gain is to be adjusted, equation 33 can be solved for R_Q in terms of R_{IN} and this substituted into equation 6 to find the required R_{IN} and R_Q.

NOTCH FILTERS

Notches can be generated by two simple methods: using RC input *(Figure 8)* or low pass/high pass summing *(Figure 9)*. The RC input method requires adding a capacitor to pin 14 and a resistor connects to pin 7. The summing method requires two resistors connected to the low pass and high pass output.

The difference between the two possible methods of generating a notch is that the capacitor connection requires a high quality precision capacitor and the gain of the circuit is difficult to adjust because the gain and zero location are both dependent on C_Z and R_Z. The amplifier summing method requires 3 precision resistors and an external operational amplifier. However, the gain can be adjusted independent of the notch frequency.

For input RC notch tuning:

$$R_Z = \frac{C_Z R_f \times 10^{12}}{220}\left(\frac{f_o}{f_z}\right)^2 \ \Omega \qquad (7)$$

f_z = frequency of notch (zero location)

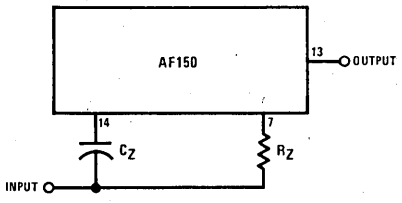
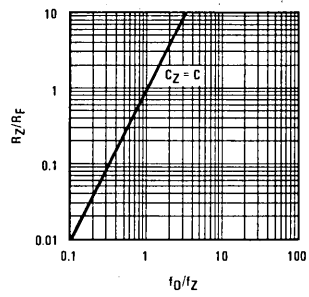


FIGURE 8. Input RC Notch

GRAPH G. Input RC Notch



For the low pass/high pass summing technique,

$$R_h = \left(\frac{f_z}{f_o}\right)^2 \frac{R_L}{10} \qquad (8)$$

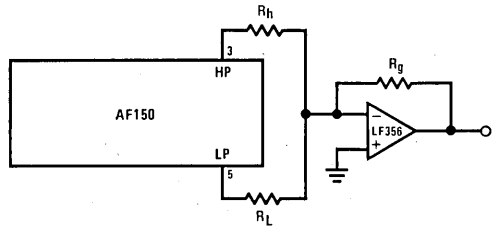
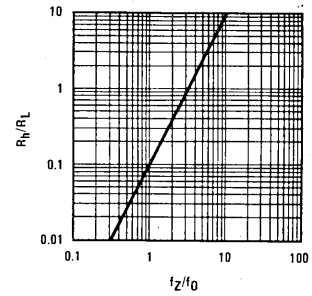


FIGURE 9. Output Notch

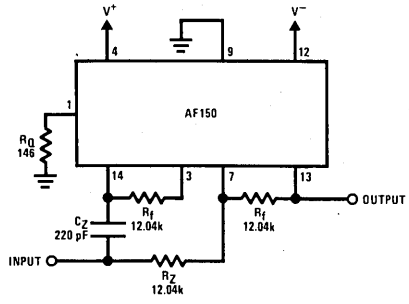
GRAPH H. Output Notch



DESIGN EXAMPLE

19 kHz notch using RC input.

Center frequency	19 kHz	f_o
Zero frequency	19 kHz	f_Z
	20	Q



Applications Information (Continued)

Using equation 1:

$$R_f = \frac{228.8 \times 10^6}{f_o}\ \Omega$$

$$R_f = 12{,}040\Omega$$

Using equation 4 with $R_{IN} = \infty$:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}}\ \Omega$$

$$R_Q = 146\Omega$$

Using equation 7:

$$R_Z = \left(\frac{C_Z R_F \times 10^{12}}{220}\right)\left(\frac{f_o}{f_z}\right)^2\ \Omega$$

$$R_Z = 12{,}040\Omega$$

DESIGN EXAMPLE

19 kHz notch using low pass/high pass summing

Center frequency	19 kHz	f_o
Zero frequency	19 kHz	f_Z
	20	Q

Using equation 1:

$$R_f = \frac{228.8 \times 10^6}{f_o}\ \Omega$$

$$R_f = 12{,}040\Omega$$

Using equation 4, choose $R_{IN} = 10\ k\Omega$:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}}\ \Omega$$

$$R_Q = 148\Omega$$

Using equation 8:

$$R_h = \left(\frac{f_Z}{f_o}\right)^2 \frac{R_L}{10}$$

Choose $R_L = 20k$, then $R_h = 2k$

TRIALS, TRIBULATIONS AND TRICKS

Certainly, there is no substitute for experience when applying active filters, working with op amps or riding a bicycle. However, the following section will discuss some of the finer points in more detail, and hopefully alleviate some of the fears and problems that might be encountered.

TUNING TIPS

In applications where 2 to 3% accuracy is not sufficient to provide the required filter response, the AF150 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the band pass (pin 13) output.

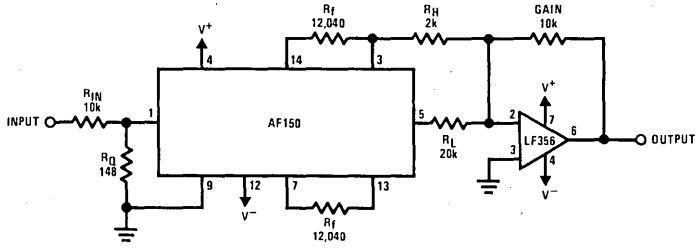
Before any tuning is attempted the low pass (pin 5) output should be checked to see that the output is not clipping. At the center frequency of the section the low pass output is 10 dB higher than the band pass output and 20 dB higher than the high pass. This should be kept in mind because if clipping occurs the results obtained when tuning will be incorrect.

Frequency Tuning

By adjusting the resistance between pins 7 and 13 the center frequency of a section can be adjusted. If the input is through pin 1 the phase shift at center frequency will be 180° and if the input is through pin 2 the phase shift at center frequency will be 0°. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

Q Tuning

The Q is tuned by adjusting the resistance between pin 1 or pin 2 and ground. Low Q tuning resistors will be from pin 2 to ground ($Q < 0.6$). High Q tuning resistors will be from pin 1 to ground. To tune the Q correctly, the signal source must have an output impedance very much lower than the input resistance of the filter since



Applications Information, (Continued)

the input resistance affects the Q. The input must be driven through the same resistance the circuit will see to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right) \times (f_o)$$

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q} \right) \times (f_o)$$

where f_o = center frequency

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair the notch can be tuned by adjusting the ratio of the summing resistors (low pass/high pass summing) or the input resistance (input RC).

In either case the signal is connected to the input and the proper resistor is adjusted for a null at the output.

Special Cases

When using the input RC notch the unit cannot be tuned through the normal input so an additional 100k resistor can be added at pin 1 and the unit can be tuned normally. Then the 100k input resistor should be grounded and the notch tuned through the normal RC input.

An alternative way of tuning is to tune using the Q resistor as the input. This requires the Q resistor be lifted from ground and connecting the signal source to the normally grounded end of the Q resistor. This has the problem that when the Q resistor is grounded after tuning, its value is decreased by the output impedance of the source. This technique has the advantage of not requiring an additional resistor.

TUNING PROCEDURE

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the low pass output pin 5.

Adjust the resistance between pins 13 and 7 until the phase shift between input and band pass output is 180°.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

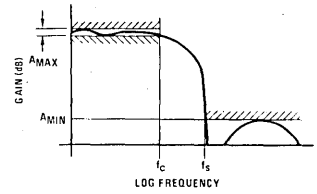
Zero Tuning

Set the oscillator output to the zero frequency and tune the zero resistor for a null at the output of the summing amplifier.

FILTER DESIGN

Since most filter tables are in terms of a normalized low pass prototype, the filter to be designed is usually reduced to a low pass prototype. After the low pass transfer function is found, it is transformed to obtain the transfer function for the actual filter desired. The low pass amplitude response which can be defined by four quantities, defined below:

Low Pass Response



A_{MAX} = the maximum peak-to-peak ripple in the pass band

A_{MIN} = the minimum attenuation in the stop band

f_c = the pass band cutoff frequency

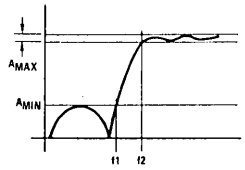
f_s = the stop band start frequency

By defining these four quantities for the low pass prototype the normalized pole and zero locations and the Q (quality) of the poles can be determined from tables or by computer programs.

To obtain the high pass from the low pass filter tables, A_{MAX} and A_{MIN} are the same as for the low pass case, but $f_c = 1/f_2$ and $f_s = 1/f_1$.

Applications Information (Continued)

High Pass Response



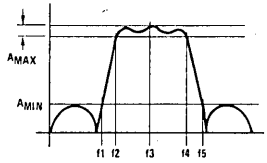
To obtain the band pass from the low pass filter tables, A_{MAX} and A_{MIN} are the same as for the low pass case, but:

$$f_c = 1 \qquad f_s = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 \cdot f_5} = \sqrt{f_2 \cdot f_4}$ i.e., geometric symmetry

$f_5 - f_1 = A_{MIN}$ bandwidth
$f_4 - f_2$ = Ripple bandwidth

Band Pass Response

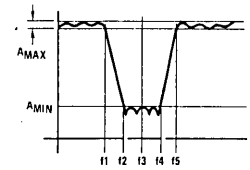


To obtain the notch from the low pass filter tables, A_{MAX} and A_{MIN} are the same as for the low pass case and

$$f_c = 1, \quad f_s = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 \cdot f_5} = \sqrt{f_2 \cdot f_4}$

Notch Response



Normalized Low Pass Transformed to Un-Normalized Low Pass

The normalized low pass filter has the pass band edge normalized to unity. The un-normalized low pass filter instead has the pass band edge at f_c. The normalized and un-normalized low pass filters are related by the transformation $s = s\omega_c$. This transforms the normalized pass band edge $s = j$ to the un-normalized pass band edge $s = j\omega_c$.

Normalized Low Pass Transformed to Un-Normalized High Pass

The transformation that can be used for low pass to high pass is $S = \omega_c/s$. Since S is inversely proportional to s, the low frequency and high frequency responses are interchanged. The normalized low pass $1/(S^2 + S/Q + 1)$ transforms to the un-normalized high pass:

$$\frac{s^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2}$$

Normalized Low Pass Transformed to Un-Normalized Band Pass

The transformation that can be used for low pass to band pass is:

$$S = \frac{s^2 + \omega_o^2}{BW \cdot s}$$

where ω_o^2 is the center frequency of the desired band pass filter and BW is the ripple bandwidth.

Normalized Low Pass Transformed to Un-Normalized Band Stop (Or Notch)

The bandstop filter has a reciprocal response to a band pass filter. Therefore, a bandstop filter can be obtained by first transforming the low pass prototype to a high pass and then performing the band pass transformation.

SELECTION OF TRANSFER FUNCTION

The selection of a function which approximates the shape of the response desired is a complicated process. Except in the simplest cases, it requires the use of tables or computer programs. The form of the transfer function desired is in terms of the pole and zero locations. The most common approximations found in tables are Butterworth, Chebychev, Elliptic and Bessel. The decision as to which approximation to use is usually a function of the requirements and system objectives. Butterworth filters are the simplest but have the disadvantage of requiring high order transfer functions to obtain sharp roll-offs.

The Chebychev function is a min/max approximation in the pass band. This approximation has the property that it is equiripple which means that the error oscillates between maximums and minimums of equal amplitude in the pass band. The Chebychev approximation, because of its equiripple nature, has a much steeper transition region than the Butterworth approximation.

The elliptic filter, also known as Cauer or Zolotarev filters, are equiripple in the pass band and stop band and have a steeper transition region than the Butterworth or the Chebychev.

For a specific low pass filter three quantities can be used to determine the degree of the transfer function: the maximum pass band ripple, the minimum stop band attenuation, and the transition ratio ($tr = \omega_s/\omega_c$). Decreasing A_{MAX}, increasing A_{MIN}, or decreasing tr will increase the degree of the transfer function. But for

Applications Information (Continued)

the same requirements the elliptic filter will require the lowest order transfer function. Tables and graphs are available in reference books such as "Reference Data for Radio Engineers", Howard W. Sams & Co., Inc., 5th Edition, 1970 and Erich Christian and Egon Eisenmann, "Filter Design Tables and Graphs", John Wiley and Sons, 1966.

For specific transfer functions and their pole locations such text as Louis Weinberg, "Network Analysis and Synthesis", McGraw Hill Book Company, 1962 and Richard W. Daniels, "Approximation Methods for Electronic Filter Design", McGraw-Hill Book Company, 1974, are available.

DESIGN OF CASCADED MULTISECTION FILTERS

The first step in designing is to define the response required and define the performance specifications:

1. Type of filter:
   Low pass, high pass, band pass, notch, all pass
2. Attenuation and frequency response
3. Performance
   Center frequency/corner frequency plus tolerance and stability
   Insertion loss/gain plus tolerance and stability
   Source impedance
   Load impedance
   Maximum output noise
   Power consumption
   Power supply voltage
   Dynamic range
   Maximum output level

Second step is to find the pole and zero location for the transfer function which meet the above requirements. This can be done by using tables and graphs or network synthesis. The form of the transfer function which is easiest to convert to a cascaded filter is a product of first and second order terms in these forms:

First Order	Second Order	
$\frac{K}{s+\omega_r}$	$\frac{K}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$	(low pass)
$\frac{Ks}{s+\omega_r}$	$\frac{Ks^2}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$	(high pass)
	$\frac{Ks}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$	(band pass)
	$\frac{K(s^2+\omega_z^2)}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$	(notch)
	$\frac{s^2-\frac{\omega_o}{Q}s+\omega_o^2}{s^2+\frac{\omega_o}{Q}s+\omega_o^2}$	(all pass)

Each of the second order functions is realizable by using an AF150 stage. By cascading these stages the desired transfer function is realized.

CASCADING SECOND ORDER STAGES

The primary concern in cascading second order stages is to minimize the difference in amplitude from input to output over the frequencies of interest. A computer program is probably required in very complicated cases but some general rules that can be used that will usually give satisfactory results are:

1. The highest Q pole pair should be paired with the zero pair closest in frequency.
2. If high pass and low pass stages are cascaded, the low pass sections should be the higher frequency and high pass sections the lower frequency.
3. In cascaded filters of more than two sections, the first section should be the section with Q closest to 0.707 and then additional stages should be added in order of least difference between first stage Q and their Q.

DESIGN EXAMPLES OF CASCADE CONNECTIONS

Example 1.

Consider a 4th order Butterworth low pass filter with a 10 kHz cutoff (−3 dB) frequency and input impedance $\geq 30\ k\Omega$.

From tables, the normalized filter parameters are:

F1 = 1.0 Q1 = 0.541
F2 = 1.0 Q2 = 1.306

Thus, relative to the design required

F1 = (1.0)(10 kHz) = 10 kHz
F2 = (1.0)(10 kHz) = 10 kHz

Section 1

F = 10 kHz, Q = 1.306

$$R_f = \frac{228.8 \times 10^6}{f_o}\ \Omega \qquad \text{(Using equation 1)}$$

$R_f = 22{,}880\Omega$

Select input resistor 31.6 kΩ

$$Q_{MIN} = \frac{1+\frac{10^4}{R_{IN}}}{3.48}$$

$Q_{MIN} = 0.378$

Applications Information (Continued)

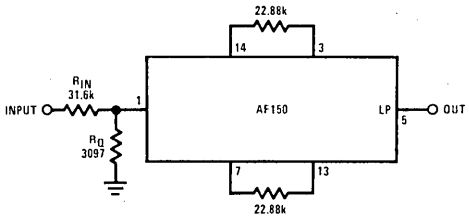
Thus, $Q > Q_{MIN}$

Therefore:

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}}\ \Omega \qquad \text{(Using equation 4)}$$

$R_Q = 3097\Omega$

First Stage



Section 2

$f_o = 10k$, $Q = 0.541$

Since f_o is the same as for the first section:

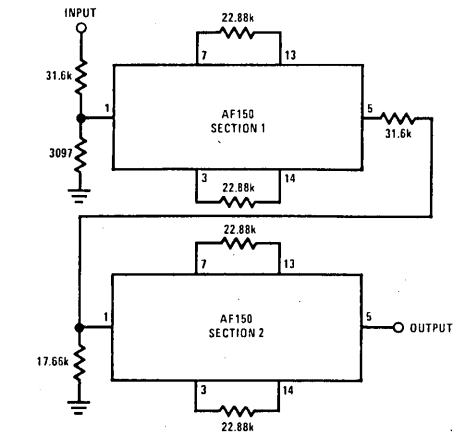
$R_f = 22.88\ k\Omega$

Select $R_{IN} = 31.6\ k\Omega$

$$R_Q = \frac{10^4}{3.48Q - 1 - \frac{10^4}{R_{IN}}}\ \Omega \qquad \text{(Using equation 4)}$$

$R_Q = 17{,}661\Omega$

Complete Filter, Example 1



Example 2.

Consider the design of a low pass filter with the following performance:

$f_c = 10$ kHz
$f_s = 11$ kHz
$A_{MAX} = 1$ dB
$A_{MIN} = 40$ dB

It is found that a 6th order elliptic filter will satisfy the above requirements. The parameters of the design are:

STAGE	f_o (kHz)	Q	f_z (kHz)
1	5.16	0.82	29.71
2	8.83	3.72	13.09
3	10.0	20.89	11.15

Stage 1

a) From equation 1, R_F is found to be 44.34k
b) From equation 4, R_Q is found to be 11.72k, assuming R_{IN} (arbitrary) is 10 kΩ.

To create the transmission zero, f_z, at 29.71 kHz, use equation 8.

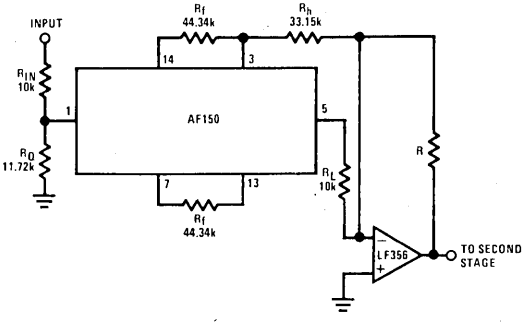
$$R_h = \left(\frac{f_z}{f_o}\right)^2 \frac{R_L}{10}, \text{ or } R_h = \left(\frac{29.71}{5.16}\right)^2 \frac{R_L}{10}$$

Thus,

$R_h = 3.315\ R_L$

If R_L is arbitrarily chosen as 10 kΩ, R_h = 33.15k.

Thus, the design of the first stage is:



where the feedback resistor, R, around the external op amp may be used to adjust the gain.

Applications Information (Continued)

Stage 2

The second stage design follows exactly the same procedure as the first stage design. The results are:

a) From equation 1, $R_f = 25.91k$
b) From equation 4, $R_Q = 913.6\Omega$, again assuming R_{IN} is arbitrarily 10k.

c) $R_h = \left(\frac{13.09}{8.83}\right)^2 \frac{R_L}{10}$ or $R_h = 0.22\ R_L$

Selecting $R_L = 10k$, then $R_h = 2.2k$, the second stage design is shown below.

Stage 3

The third stage design, again, is identical to the first 2 stages and the results are (for $R_{IN} = 10k$):

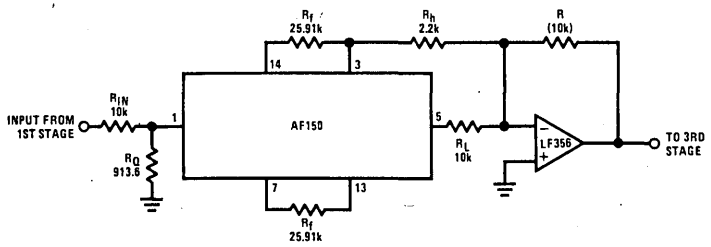
$$R_f = \frac{228.8 \times 10^6}{f_o} = 22.88k$$

$$R_Q = \frac{10^4}{3.48\Omega - 1 - \frac{10^4}{R_{IN}}} = 141.4\Omega$$

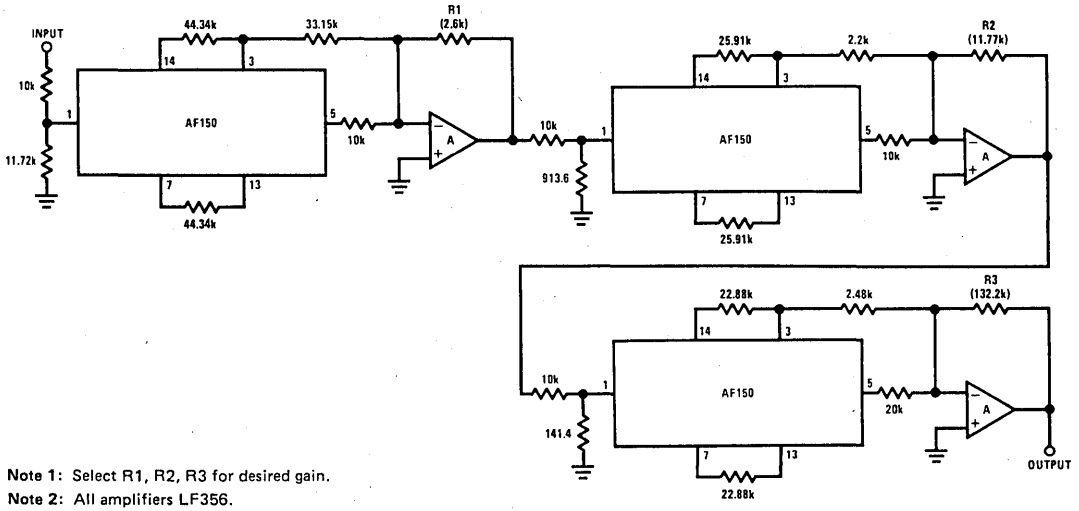
$$R_h = \left(\frac{f_z}{f_o}\right)^2 \frac{R_L}{10} = \left(\frac{11.5}{10}\right)^2 \frac{R_L}{10} \qquad R_h = 0.124\ R_L$$

Let $R_L = 20k$, $R_h = 2.48k$

Second Stage



Filter for Example 2



Note 1: Select R1, R2, R3 for desired gain.
Note 2: All amplifiers LF356.

Applications Information (Continued)

From equation 13, the DC gain of the first section is

$$A_{V1} = \frac{11}{1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}}$$

$$A_{V1} = \frac{11}{1 + \frac{10^4}{10^4} + \frac{10^4}{11.72 \times 10^3}} = 3.86\ V/V$$

Similarly, the DC gain of the second and third sections are:

$A_{V2} = 0.850$
$A_{V3} = 0.151$

Therefore, the overall DC gain is 0.495 and can be adjusted by selecting R1 with respect to 10k, R2 with respect to 10k or R3 with respect to 20k.

For convenience, a standard resistor value table is given below.

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.33 can represent 1.33Ω, 133Ω, 1.33 kΩ, 13.3 kΩ, 133 kΩ, 1.33 MΩ.

Standard 5% and 2% Resistance Values

OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	MEGOHMS	
10	27	68	180	470	1,200	3,300	8,200	22,000	56,000	150,000	0.24	0.62
11	30	75	200	510	1,300	3,600	9,100	24,000	62,000	160,000	0.27	0.68
12	33	82	220	560	1,500	3,900	10,000	27,000	68,000	180,000	0.30	0.75
13	36	91	240	620	1,600	4,300	11,000	30,000	75,000	200,000	0.33	0.82
15	39	100	270	680	1,800	4,700	12,000	33,000	82,000	220,000	0.36	0.91
16	43	110	300	750	2,000	5,100	13,000	36,000	91,000		0.39	1.0
18	47	120	330	820	2,200	5,600	15,000	39,000	100,000		0.43	1.1
20	51	130	360	910	2,400	6,200	16,000	43,000	110,000		0.47	1.2
22	56	150	390	1,000	2,700	6,800	18,000	47,000	120,000		0.51	1.3
24	62	160	430	1,100	3,000	7,500	20,000	51,000	130,000		0.56	1.5

Decade Table Determining 1/2% and 1% Standard Resistance Values

1.00	1.21	1.47	1.78	2.15	2.61	3.16	3.83	4.64	5.62	6.81	8.25
1.02	1.24	1.50	1.82	2.21	2.67	3.24	3.92	4.75	5.76	6.98	8.45
1.05	1.27	1.54	1.87	2.26	2.74	3.32	4.02	4.87	5.90	7.15	8.66
1.07	1.30	1.58	1.91	2.32	2.80	3.40	4.12	4.99	6.04	7.32	8.87
1.10	1.33	1.62	1.96	2.37	2.87	3.48	4.22	5.11	6.19	7.50	9.09
1.13	1.37	1.65	2.00	2.43	2.94	3.57	4.32	5.23	6.34	7.68	9.31
1.15	1.40	1.69	2.05	2.49	3.01	3.65	4.42	5.36	6.49	7.87	9.53
1.18	1.43	1.74	2.10	2.55	3.09	3.74	4.53	5.49	6.65	8.06	9.76

Appendix (See footnote)

The specific transfer functions for some of the most useful circuit configurations using the AF150 are illustrated in *Figures 10 through 16*. Also included are the gain equations for each transfer function in the frequency band of interest, the Q equation, center frequency equation and the Q determining resistor equation. Q_{MIN} is a function of R_{IN} (see graph C).

a) Non-inverting input *(Figure 10)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2 \left[\frac{1.1}{1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}}\right]}{\Delta} \text{(high pass)} \quad (9)$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1 \left[\frac{1.1}{1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}}\right]}{\Delta} \text{(band pass)} \quad (10)$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2 \left[\frac{1.1}{1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}}\right]}{\Delta} \text{(low pass)} \quad (11)$$

where

$$\Delta = s^2 + s\left[\frac{1.1}{1 + \frac{10^4}{R_Q} + \frac{10^4}{R_{IN}}}\right]\omega_1 + 0.1\,\omega_1\omega_2 \quad (12)$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s \to 0} = \frac{11}{\left(1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}\right)} \text{ (DC Gain)} \quad (13)$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s \to \infty} = \frac{1.1}{\left(1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}\right)} \text{ (High Freq. Gain)} \quad (14)$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega = \omega_0} = -\frac{\left(1 + \frac{10^4}{R_Q} + \frac{10^4}{R_{IN}}\right)}{\left(1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}\right)} \text{ (Center Freq. Gain)} \quad (15)$$

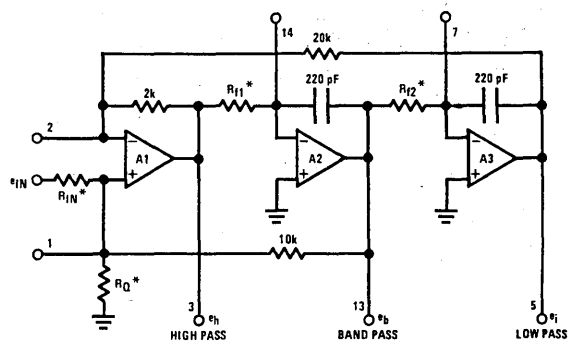
$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220} \qquad \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}$$

where

$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$, (see footnote)

$$Q = \left(\frac{1 + \frac{10^4}{R_{IN}} + \frac{10^4}{R_Q}}{1.1}\right)\sqrt{0.1\left(\frac{\omega_2}{\omega_1}\right)} \quad (16)$$

$$R_Q = \frac{10^4}{\left(\frac{1.1Q}{\sqrt{0.1\,\frac{\omega_2}{\omega_1}}}\right) - 1 - \frac{10^4}{R_{IN}}} \quad (17)$$



*External components

FIGURE 10. Non-Inverting Input ($Q > Q_{MIN}$)

FOOTNOTE:

It should be noted that in the text of this paper, ω_1 and ω_2 have been assumed equal, and hence $R_{f1} = R_{f2}$. No generality is lost in this assumption and it facilitates the design. However, for completeness, the equations given are exact.

Appendix (Continued)

b) Non-inverting input *(Figure 11)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}}\right]}{\Delta} \text{ (high pass)} \quad (18)$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}}\right]}{\Delta} \text{ (band pass)} \quad (19)$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}}\right]}{\Delta} \text{ (low pass)} \quad (20)$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{10^4}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2 \quad (21)$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s \to 0} = \frac{1.1 + \frac{2 \times 10^3}{R_Q}}{0.1\left(1 + \frac{R_{IN}}{10^4}\right)} \quad (22)$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s \to \infty} = \frac{1.1 + \frac{2 \times 10^3}{R_Q}}{1 + \frac{R_{IN}}{10^4}} \quad (23)$$

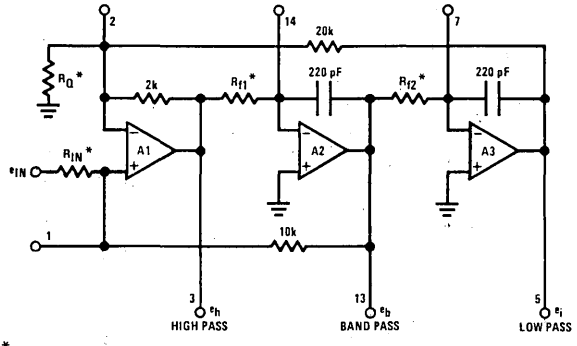
$$\left.\frac{e_b}{e_{IN}}\right|_{\omega = \omega_o} = -\frac{1 + \frac{10^4}{R_{IN}}}{1 + \frac{R_{IN}}{10^4}} \quad (24)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220}, \; \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1 + \frac{10^4}{R_{IN}}}{1.1 + \frac{2 \times 10^3}{R_Q}}\right] \sqrt{0.1\,\frac{\omega_2}{\omega_1}} \quad (25)$$

$$R_Q = \frac{2 \times 10^7}{\left(1 + \frac{10^4}{R_{IN}}\right)\left(\frac{\sqrt{0.1\,\frac{\omega_2}{\omega_1}}}{Q}\right) - 1.1} \quad (26)$$



*External components

FIGURE 11. Non-Inverting Input ($Q < Q_{MIN}$)

Appendix (Continued)

c) Inverting input *(Figure 12)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{-s^2\left(\frac{2\times10^3}{R_{IN}}\right)}{\Delta} \quad \text{(high pass)} \qquad (27)$$

$$\frac{e_b}{e_{IN}} = \frac{s\,\omega_1\left(\frac{2\times10^3}{R_{IN}}\right)}{\Delta} \quad \text{(band pass)} \qquad (28)$$

$$\frac{e_\ell}{e_{IN}} = \frac{-\omega_1\omega_2\left(\frac{2\times10^3}{R_{IN}}\right)}{\Delta} \quad \text{(low pass)} \qquad (29)$$

$$\omega_1 = \frac{10^{12}}{R_{f1}\cdot 220},\quad \omega_2 = \frac{10^{12}}{R_{f2}\cdot 220}$$

where

$$\Delta = s^2 + s\,\omega_1\left[\frac{1.1+\frac{2\times10^3}{R_{IN}}}{1+\frac{10^4}{R_Q}}\right] + 0.1\,\omega_1\,\omega_2 \qquad (30)$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{2\times10^4}{R_{IN}} \quad \text{(low pass) (DC gain)} \qquad (31)$$

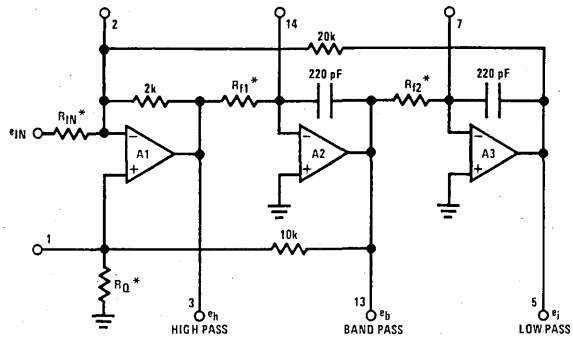
$$\left.\frac{e_h}{e_{IN}}\right|_{s\to\infty} = -\frac{2\times10^3}{R_{IN}} \quad \text{(high pass) (high freq. gain)} \qquad (32)$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = \frac{\frac{2\times10^3}{R_{IN}}\left(1+\frac{10^4}{R_Q}\right)}{1.1+\frac{2\times10^3}{R_{IN}}} \quad \begin{matrix}\text{(band pass)}\\ \text{(center freq. gain)}\end{matrix} \qquad (33)$$

$$\omega_0 = \sqrt{0.1\,\omega_1\,\omega_2}$$

$$Q = \left[\frac{1+\frac{10^4}{R_Q}}{1.1+\frac{10^4}{R_{IN}}}\right]\sqrt{0.1\,\frac{\omega_2}{\omega_1}} \qquad (34)$$

$$R_Q = \frac{10^4}{\frac{Q}{\sqrt{0.1\,\frac{\omega_2}{\omega_1}}}\left(1.1+\frac{2\times10^3}{R_{IN}}\right)-1} \qquad (35)$$



*External components

FIGURE 12. Inverting Input, Any Q

Appendix (Continued)

d) Differential input *(Figure 13)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left(\frac{2 \times 10^3}{R_{IN2}}\right)}{\Delta} \quad \text{(high pass)} \quad (36)$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left(\frac{2 \times 10^3}{R_{IN2}}\right)}{\Delta} \quad \text{(band pass)} \quad (37)$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2\left(\frac{2 \times 10^3}{R_{IN2}}\right)}{\Delta} \quad \text{(low pass)} \quad (38)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220}, \quad \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}$$

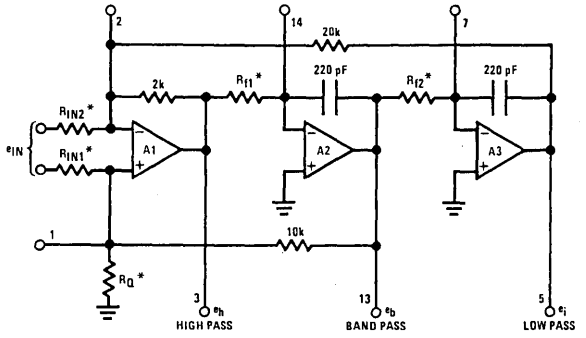
where

$$\Delta = s^2 + s\,\omega_1\left[\frac{1.1 + \frac{2 \times 10^3}{R_{IN2}}}{1 + \frac{10^4}{R_Q} + \frac{10^4}{R_{IN1}}}\right] + 0.1\,\omega_1\omega_2 \quad (39)$$

$$\omega_0 = \sqrt{0.1\,\omega_1\,\omega_2} \quad (40)$$

$$Q = \left[\frac{1 + \frac{10^4}{R_Q} + \frac{10^4}{R_{IN1}}}{1.1 + \frac{2 \times 10^3}{R_{IN2}}}\right]\sqrt{0.1\,\frac{\omega_2}{\omega_1}} \quad (41)$$

$$R_Q = \frac{10^4}{\frac{Q}{\sqrt{0.1\,\frac{\omega_2}{\omega_1}}}\left(1.1 + \frac{2 \times 10^3}{R_{IN2}}\right) - 1 - \frac{10^4}{R_{IN1}}} \quad (42)$$



*External components

FIGURE 13. Differential Input

Appendix (Continued)

e) Notch filter *(Figure 14)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = \frac{(s^2 + \omega_z^2)\left[\frac{1.1}{1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}}\right]\frac{R_g}{R_h}}{s^2 + s\,\omega_1\left[\frac{1.1}{1 + \frac{10^4}{R_Q} + \frac{10^4}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2} \quad (45)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220}, \quad \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}, \quad \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\omega_z = \omega_0\sqrt{\frac{10\,R_h}{R_L}}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to 0} = \frac{11}{\left(1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}\right)}\frac{R_g}{R_L} \quad \text{(DC gain)} \quad (46)$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to \infty} = \frac{1.1}{\left(1 + \frac{R_{IN}}{10^4} + \frac{R_{IN}}{R_Q}\right)}\frac{R_g}{R_h} \quad \text{(high freq. gain)} \quad (47)$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega = \omega_z} = 0 \quad (48)$$

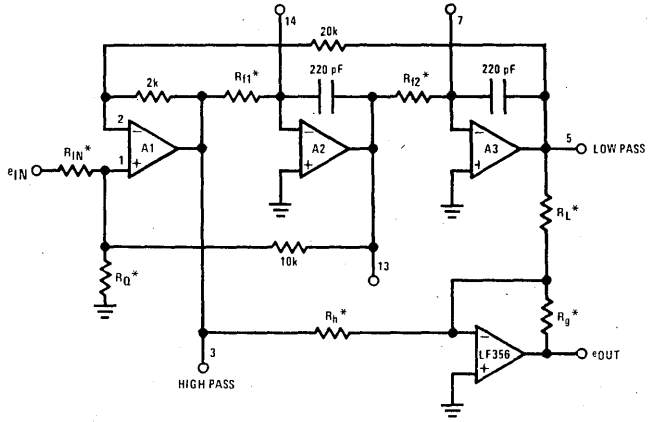


FIGURE 14. Notch Filter Using an External Amplifier

Appendix (Continued)

j) Input notch filter *(Figure 15)* transfer function equations are:

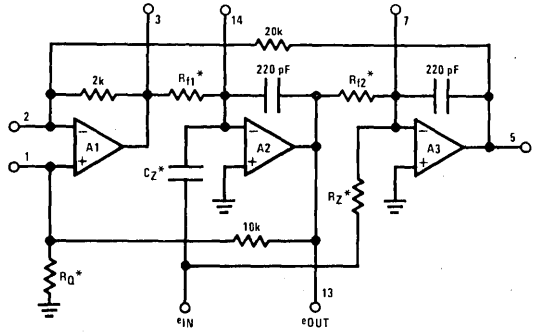
$$\frac{e_{IN}}{e_n} = -\frac{\frac{C_Z}{220 \times 10^{-12}}\left[s^2 + \omega_Z{}^2\right]}{s^2 + s\,\omega_1\left[\frac{1.1\,R_Q}{10^4 + R_Q}\right] + \omega_0{}^2} \quad (49)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220}, \quad \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}$$

$$\omega_Z = \omega_0 \sqrt{\frac{R_{f2} \cdot 220 \times 10^{-12}}{R_Z C_Z}}, \quad \omega_0 = \sqrt{0.1\,\omega_1\omega_2} \quad (50)$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to 0} = \frac{-R_{F2}}{R_Z} \quad (51)$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to \infty} = -\frac{C_Z}{220 \times 10^{-12}} \quad (52)$$



*External components

FIGURE 15. Input Notch Filter Using 3 Amplifiers

g) All pass *(Figure 16)* transfer function equations are:

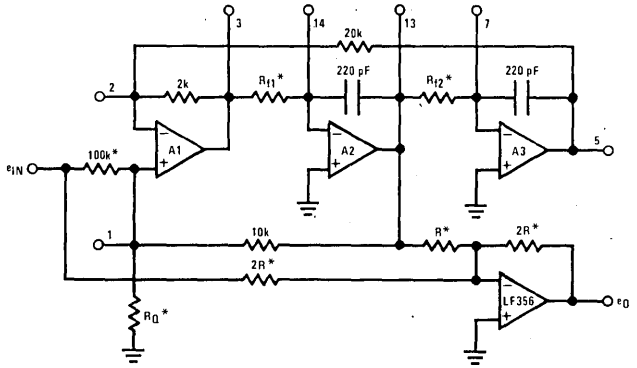
$$\frac{e_o}{e_{IN}} = -\left[\frac{s^2 - s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{R_Q}}\right] + \omega_o{}^2}{s^2 + s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{R_Q}}\right] + \omega_0{}^2}\right] \quad (53)$$

$$Q = \frac{\left[2 + \frac{10^4}{R_Q}\right]}{1.1}\sqrt{0.1\,\frac{\omega_2}{\omega_1}} \quad (54)$$

$$\omega_1 = \frac{10^{12}}{R_{f1} \cdot 220}, \quad \omega_2 = \frac{10^{12}}{R_{f2} \cdot 220}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

Time delay at ω_0 is $\frac{2Q}{\omega_0}$ seconds



*External components

FIGURE 16. All Pass

Definition of Terms

A_{MAX}	Maximum pass band peak-to-peak ripple
A_{MIN}	Minimum stop band loss
f_z	Frequency of jw axis pole pair
f_o	Frequency of complex pole pair
Q	Quality of pole
f_c	Pass band edge
f_s	Stop band edge
R_f	Pole frequency determining resistance
R_z	Zero Frequency determining resistance
R_Q	Pole quality determining resistance
f_H	Frequency above center frequency at which the gain decreases by 3 dB for a band pass filter
f_L	Frequency below center frequency at which the gain decreases by 3 dB for a band pass filter

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AF151 Dual Universal Active Filter

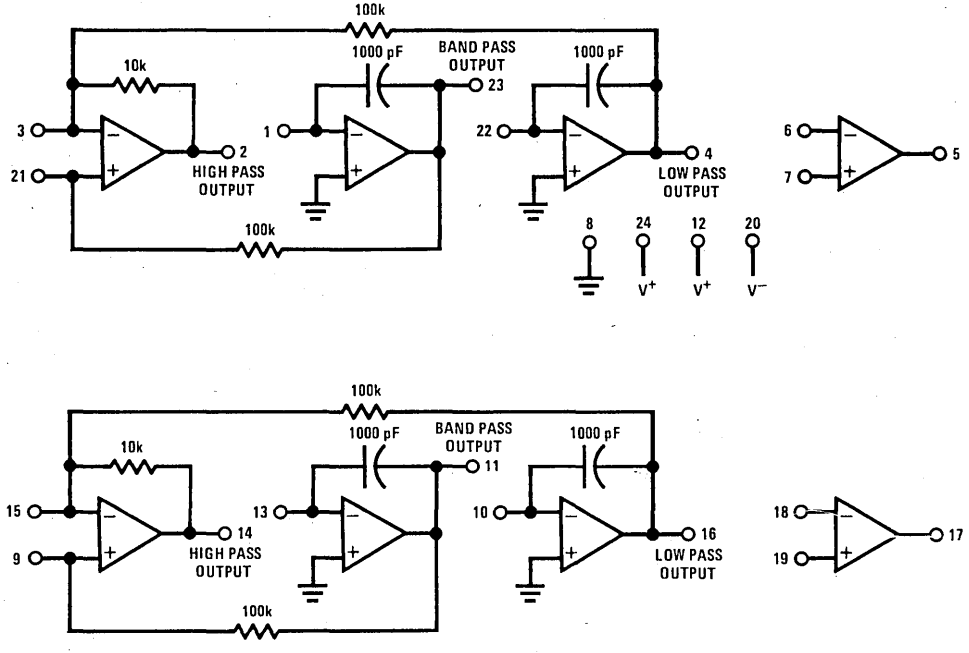
General Description

The AF151 consists of 2 general purpose state variable active filters in a single package. By using only 4 external resistors for each section, various second order functions may be formed. Low pass, high pass and band pass functions are available simultaneously at separate outputs. In addition, there are 2 uncommitted operational amplifiers which are available for buffering or for forming all pass and notch functions. Any of the classical filter configurations, such as Butterworth, Bessel, Cauer and Chebyshev can be easily formed.

Features

- Independent Q, frequency and gain adjustment
- Very low sensitivity to external component variation
- Separate low pass, high pass and band pass outputs
- Operation to 10 kHz
- Q range to 500
- Wide power supply range—±5V to ±18V
- Accuracy—±1%
- Fourth order functions in one package

Circuit Diagrams



Ceramic Dual-In-Line Package HY24A
AF151-1CJ
AF151-2CJ

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation	900 mW/Package
Differential Input Voltage	±36V
Output Short-Circuit Duration (Note 1)	Infinite
Operating Temperature	−25°C to +85°C
Storage Temperature	−25°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Complete Active Filter)

Specifications apply for V_S = ±15V and over −25°C to +85°C unless otherwise specified. (Specifications apply for each section).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_c \times Q \leq 50{,}000$			10k	Hz
Q Range	$f_c \times Q \leq 50{,}000$			500	Hz/Hz
f_o Accuracy					
AF151-1C	$f_c \times Q \leq 10{,}000$, T_A = 25°C			±2.5	%
AF151-2C	$f_c \times Q \leq 10{,}000$, T_A = 25°C			±1.0	%
f_o Temperature Coefficient			±50	±150	ppm/°C
Q Accuracy	$f_c \times Q \leq 10{,}000$, T_A = 25°C			±7.5	%
Q Temperature Coefficient			±300	±750	ppm/°C
Power Supply Current	V_S = ±15V		2.5	4.5	mA

Electrical Characteristics (Internal Op Amp) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current			4	50	nA
Input Bias Current			30	200	nA
Input Resistance			2.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2$k, V_{OUT} = ±10V	25	160		V/mV
Output Voltage Swing	R_L = 10 kΩ	±12	±14		V
	R_L = 2 kΩ	±10	±13		V
Input Voltage Range		±12			V
Common-Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ	77	96		dB
Output Short-Circuit Current			25		mA
Slew Rate (Unity Gain)			0.6		V/μs
Small Signal Bandwidth			1		MHz
Phase Margin			60		Degrees

Note 1: Any of the amplifiers can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: Specifications apply for V_S = ±15V, T_A = 25°C.

Applications Information

The AF151 consists of 2 identical filter sections and 2 uncommitted op amps. The op amps may be used for buffering inputs and outputs, summing amplifiers (for notch filter generation), adjusting gain through the filter sections, additional passive networks to create higher order filters, or simply used elsewhere in the user's system.

The design equations given apply to both sections; however, for clarity, only the pin designations for section 1 will be shown in the examples and discussion.

See the AF100 data sheet for additional information on this type of filter.

The design equations assume that the user has knowledge of the frequency and Q values for the particular design to be synthesized. If this is not the case, various references and texts are available to help the user in determining these parameters. A bibliography of recommended texts can also be found in the AF100 data sheet.

CIRCUIT DESCRIPTION AND OPERATION

A schematic of one section of the AF151 is shown in *Figure 1*. Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input. Amplifier A4 is an uncommitted amplifier.

By adding external resistors the circuit can be used to generate the second order system.

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_o = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_o}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(high pass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer functions becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(band pass)}$$

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(low pass)}$$

Using proper input and output connections the circuit can also be used to generate the transfer functions for a notch and all pass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals ω_z^2 and a_3 equals 1. The transfer function becomes:

$$T(s) \quad \frac{s^2 + \omega_z^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(notch)}$$

In the all pass transfer function $a_1 = \omega_o^2$, $a_2 = -\omega_o/Q$ and $a_3 = 1$. The transfer function becomes:

$$T(s) \quad \frac{s^2 - \frac{\omega_o}{Q} s + \omega_o^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(all pass)}$$

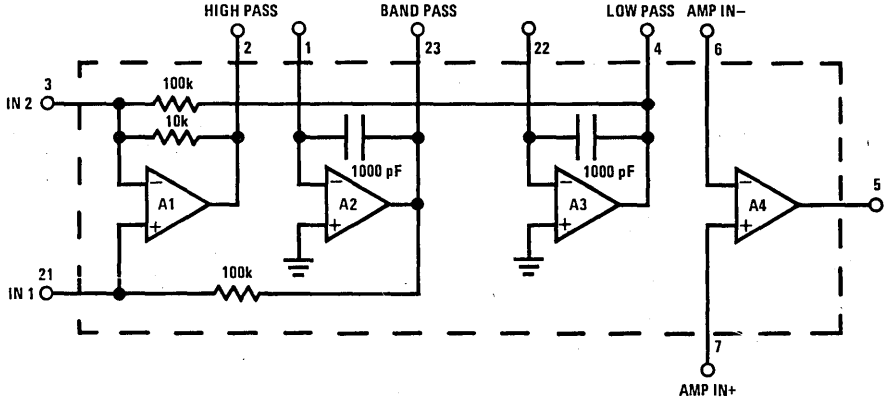


FIGURE 1. AF151 Schematic (Section 1)

Applications Information (Continued)

FREQUENCY CALCULATIONS

For operation above 200 Hz, the frequency of each section of the AF151 is set by 2 equal valued resistors. These resistors couple the output of the first op amp (pin 2) to the input of the second op amp (pin 1) and the output of the second op amp (pin 23) to the input of the third op amp (pin 22).

The value for R_f is given by:

$$R_f = \frac{50.33 \times 10^6}{f_o}\ \Omega \qquad (1)$$

For operation below 200 Hz, "T" tuning should be used as shown in *Figure 3*.

For this configuration,

$$R_S = \frac{R_T^2}{R_f - 2R_T} \qquad (2)$$

where R_T or R_S can be chosen arbitrarily, once R_f is found from equation 1.

Q CALCULATIONS

To set the Q of each section of the AF151, one resistor is required. The value of the Q setting resistor depends on the input connection (inverting or non-inverting) and the input resistance. Because the input resistance does affect the Q, it is often desirable to use one of the uncommitted op amps to provide a buffer between the signal source impedance and the input resistor used to set the Q.

To determine which connection is required for a particular Q, arbitrarily select a value of R_{IN} *(Figure 4)* and calculate Q_{MIN} according to equation 3.

$$Q_{MIN} = \frac{1 + \frac{10^5}{R_{IN}}}{3.48} \qquad (3)$$

If the Q required for the circuit is greater than Q_{MIN}, use equation 4 to calculate the value of R_Q and the connection shown in *Figure 4*.

$$R_Q = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}} \qquad (4)$$

If the Q required for the circuit is less than Q_{MIN}, use equation 5 to calculate the value of R_Q and the connection shown in *Figure 5*.

$$R_Q = \frac{10^4}{\frac{0.3162}{Q}\left(1 + \frac{10^5}{R_{IN}}\right) - 1.1} \qquad (5)$$

Both connections shown in *Figures 4 and 5* are "non-inverting" relative to the phase relationship between the input signal and the low pass output.

For any Q, equation 6 may be used with the "inverting" connection shown in *Figure 6*.

$$R_Q = \frac{10^5}{3.16\,Q\left(1.1 + \frac{10^4}{R_{IN}}\right) - 1} \qquad (6)$$

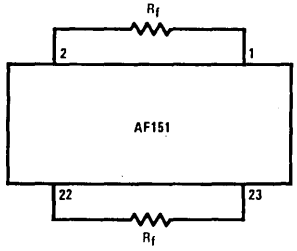


FIGURE 2. Frequency Tuning

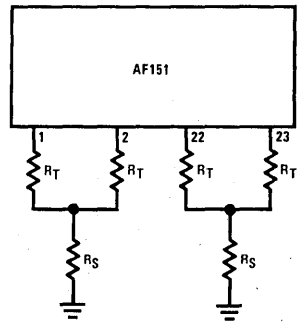


FIGURE 3. "T" Tuning for Low Frequency

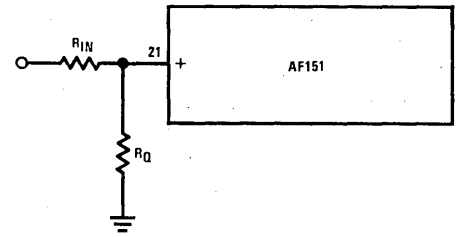


FIGURE 4. Connection for Q > Q_{MIN}

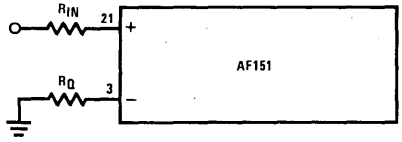


FIGURE 5. Connection for Q < Q_{MIN}

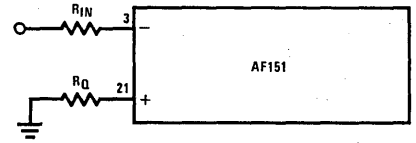


FIGURE 6. Connection for Any Q, Inverting

Applications Information (Continued)

NOTCH TUNING

When the low pass output and the high pass output are summed together, the result is a notch *(Figure 7)*.

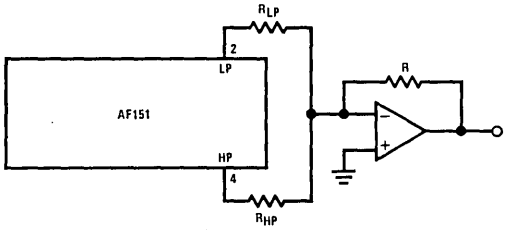


FIGURE 7. Notch Filter

The relationship between R_{LP}, R_{HP}, f_o and f_z, the location of the notch, is given by equation 7.

$$R_{HP} = \left(\frac{f_z}{f_o}\right)^2 \frac{R_{LP}}{10} \qquad (7)$$

Again, it is advantageous to use one of the uncommitted op amps to perform this summing function to prevent loading of this stage or the resistors R_{LP} and R_{HP} from effecting the Q of subsequent stages. Resistor R can be used to set the gain of the filter section.

GAIN CALCULATIONS

The following list of equations will be helpful in calculating the relationship between the external components and various important parameters. The following definitions are use:

A_L – Gain from input to low pass output at DC
A_H – Gain from input to high pass output at high frequency
A_B – Gain from input to band pass output at center frequency

For *Figure 4*:

$$A_L = \frac{11}{\Delta}$$

$$A_H = \frac{1.1}{\Delta}$$

$$A_B = \frac{-\left(1 + \frac{10^5}{R_Q} + \frac{10^5}{R_{IN}}\right)}{\Delta}$$

$$\Delta = 1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}$$

For *Figure 5:*

$$A_L = \frac{11 + \frac{10^5}{R_Q}}{\Delta}$$

$$A_H = \frac{1.1 + \frac{10^4}{R_Q}}{\Delta}$$

$$A_B = \frac{-\left(1 + \frac{10^5}{R_{IN}}\right)}{\Delta}$$

$$\Delta = 1 + \frac{R_{IN}}{10^5}$$

For *Figure 6:*

$$A_L = -\frac{10^5}{R_{IN}}$$

$$A_H = -\frac{10^4}{R_{IN}}$$

$$A_B = \frac{\frac{10^5}{R_{IN}}\left(1 + \frac{10^5}{R_Q}\right)}{11 + \frac{10^5}{R_{IN}}}$$

For *Figure 7*:

At low frequency, when $f_o < f_z$, the gain to the output of the summing op amp is:

$$A_L = \frac{11\left(\frac{R}{R_{LP}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)}$$

At high frequency, when $f_o > f_z$, the gain to the output of the summing op amp is:

$$A_H = \frac{1.1\left(\frac{R}{R_{HP}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)}$$

At the notch, ideally the gain is zero (0).

TUNING TIPS

In applications where 2% to 3% accuracy is not sufficient to provide the required filter response, the AF151 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the band pass output.

Before any tuning is attempted, the low pass output should be checked to see that the output is not clipping. At the center frequency of the section, the low pass output is 10 dB higher than the band pass output and 20 dB higher than the high pass. This should be kept in mind because if clipping occurs, the results obtained when tuning will be incorrect.

Applications Information (Continued)

Frequency Tuning

By adjusting resistor R_f, center frequency of a section can be adjusted. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

Q Tuning

The Q is tuned by adjusting the R_Q resistor. To tune the Q correctly, the signal source must have an output impedance very much lower than the input resistance of the filter since the input resistance affects the Q. The input must be driven through the same resistance the circuit will "see" to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right) \times (f_o)$$

where f_o = center frequency

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q}\right) \times (f_o)$$

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair, the notch can be tuned by adjusting the ratio of the summing resistors (low pass/high pass summing).

In either case, the signal is connected to the input and the proper resistor is adjusted for a null at the output.

TUNING PROCEDURE

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the low pass output.

Adjust the R_f resistor until the phase shift between input and band pass output is 180° or 0°, depending upon the connection.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

Zero Tuning (Notch Tuning)

Set the oscillator output to the zero frequency and tune one of the summing resistors for a null at the output of the summing amplifier.

Gain Adjust

Set the oscillator to any desired frequency and the gain can be adjusted by measuring the output of the summing amplifier and adjusting the feedback resistance.

DESIGN EXAMPLE

Assume 2 band pass filters are required to separate FSK data.

f1 = 800 Hz, Q = 40
f2 = 1000 Hz, Q = 50

The gain through each filter is to be 10 V/V (20 dB).

Since the design is similar for both sections, only the first section design will be shown for the example.

(a) From equation 1

$$R_f = \frac{50.33 \times 10^6}{f_o} = \frac{50.33 \times 10^6}{800}$$

$$\boxed{R_f = 62.9k}$$

(b) Checking Q_{MIN} from equation 3, arbitrarily let R_{IN} = 300k.

$$Q_{MIN} = \frac{1 + \frac{10^5}{R_{IN}}}{3.48} = \frac{1 + \frac{10^5}{3 \times 10^5}}{3.48} = 0.383$$

Since the Q required for the design (Q = 40), is greater than Q_{MIN}, the circuit of *Figure 4* or *Figure 6* may be used. Arbitrarily we shall select the circuit of *Figure 4*.

(c) From equation 4, R_Q is found to be

$$R_Q = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}} = \frac{10^5}{(3.48)(40) - 1 - \frac{10^5}{3 \times 10^5}}$$

or $\boxed{R_Q = 725\Omega}$

(d) Calculate the center frequency gain for *Figure 4*.

$$A_B = \frac{-\left(1 + \frac{10^5}{R_Q} + \frac{10^5}{R_{IN}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)} = \frac{-(1 + 137.9 + 0.333)}{(1 + 3.0 + 414)}$$

$$A_B = 0.333 \text{ V/V}$$

Since the gain at f_o is 0.333 V/V, a gain of 10 V/V can be obtained by using the uncommitted operational amplifier with a gain of 30.03 as shown in *Figure 8*.

Applications Information (Continued)

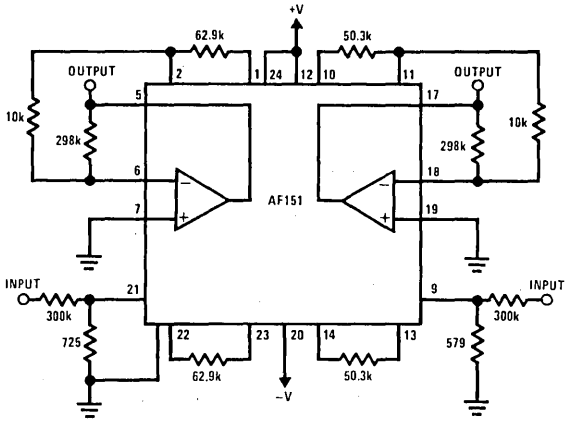


FIGURE 8. Dual Band Pass Filter

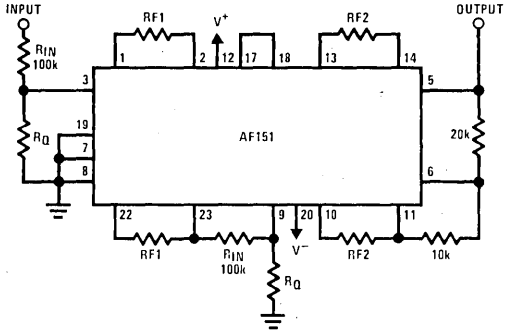


FIGURE 9. Telephone Multifrequency (MF) Band Pass Filter

FREQ	BW	f_c	f1	Q1 & Q2	f2	RF1	RF2	RQ
700	75	698.4	665.6	17	732.8	75.62k	68.68k	1.749k
900	75	898.7	865.8	21.8	932.9	58.13k	53.95k	1.354k
1100	75	1098.8	1065.7	26.7	1132.9	47.23k	44.43k	1.100k
1300	75	1298.9	1265.8	31.6	1332.9	39.76k	37.76k	926.2Ω
1500	75	1499.0	1465.8	36.4	1532.9	34.34k	32.83k	802.1Ω
1700	75	1699.1	1665.9	41.3	1733.0	30.21k	29.04k	705.6Ω

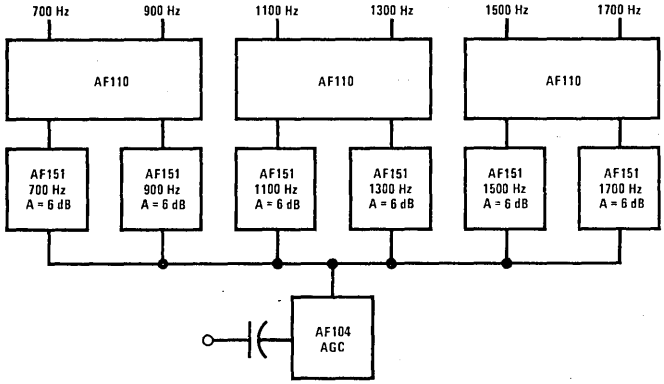
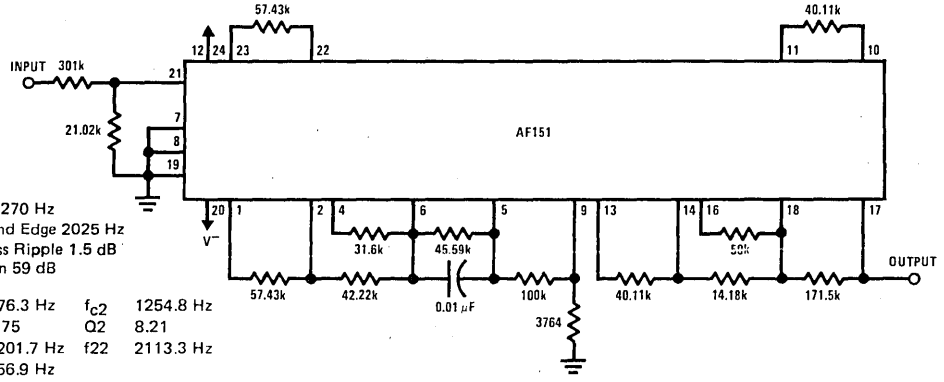


FIGURE 10. MF Tone Receiver



Cutoff 1270 Hz
Stop Band Edge 2025 Hz
Band Pass Ripple 1.5 dB
Rejection 59 dB

f_{c1}	876.3 Hz	f_{c2}	1254.8 Hz
Q1	1.75	Q2	8.21
f_{z1}	3201.7 Hz	f22	2113.3 Hz
f_R	356.9 Hz		

FIGURE 11. Low Pass Low Speed Asynchronous FSK Modem Filter

Applications Information (Continued)

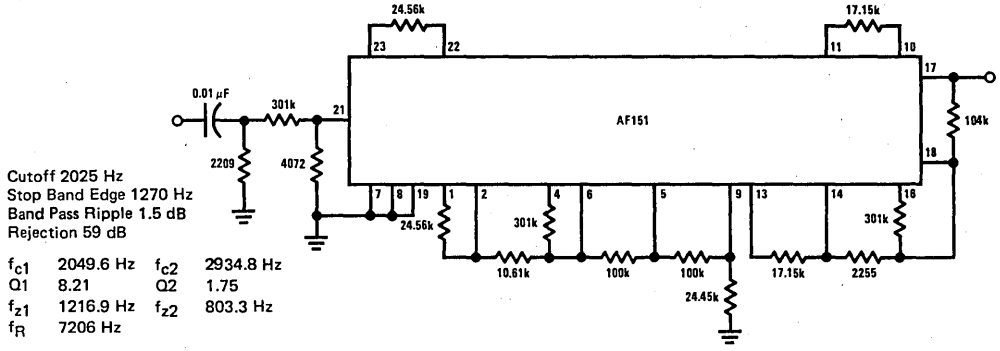


FIGURE 12. High Pass Low Speed Asynchronous FSK Modem Filter

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example,1.33 can represent 1.33Ω, 133Ω, 1.33 kΩ, 13.3 kΩ, 133 kΩ 1.33 MΩ.

Standard 5% and 2% Resistance Values

OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	MEGOHMS	
10	27	68	180	470	1,200	3,300	8,200	22,000	56,000	150,000	0.24	0.62
11	30	75	200	510	1,300	3,600	9,100	24,000	62,000	160,000	0.27	0.68
12	33	82	220	560	1,500	3,900	10,000	27,000	68,000	180,000	0.30	0.75
13	36	91	240	620	1,600	4,300	11,000	30,000	75,000	200,000	0.33	0.82
15	39	100	270	680	1,800	4,700	12,000	33,000	82,000	220,000	0.36	0.91
16	43	110	300	750	2,000	5,100	13,000	36,000	91,000		0.39	1.0
18	47	120	330	820	2,200	5,600	15,000	39,000	100,000		0.43	1.1
20	51	130	360	910	2,400	6,200	16,000	43,000	110,000		0.47	1.2
22	56	150	390	1,000	2,700	6,800	18,000	47,000	120,000		0.51	1.3
24	62	160	430	1,100	3,000	7,500	20,000	51,000	130,000		0.56	1.5

Decade Table Determining 1/2% and 1% Standard Resistance Values

1.00	1.21	1.47	1.78	2.15	2.61	3.16	3.83	4.64	5.62	6.81	8.25
1.02	1.24	1.50	1.82	2.21	2.67	3.24	3.92	4.75	5.76	6.98	8.45
1.05	1.27	1.54	1.87	2.26	2.74	3.32	4.02	4.87	5.90	7.15	8.66
1.07	1.30	1.58	1.91	2.32	2.80	3.40	4.12	4.99	6.04	7.32	8.87
1.10	1.33	1.62	1.96	2.37	2.87	3.48	4.22	5.11	6.19	7.50	9.09
1.13	1.37	1.65	2.00	2.43	2.94	3.57	4.32	5.23	6.34	7.68	9.31
1.15	1.40	1.69	2.05	2.49	3.01	3.65	4.42	5.36	6.49	7.87	9.53
1.18	1.43	1.74	2.10	2.55	3.09	3.74	4.53	5.49	6.65	8.06	9.76

National Semiconductor

Active Filters

PRELIMINARY

AF160 Universal Wideband Active Filter

General Description

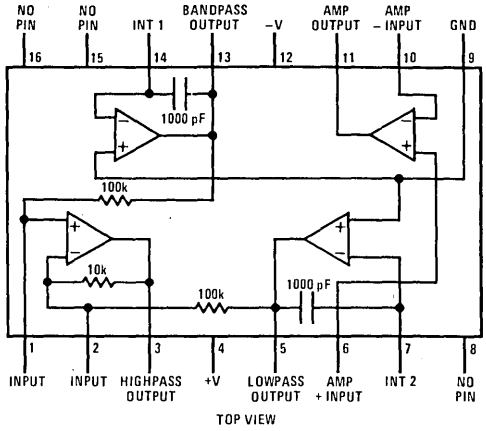
The AF160 state variable active filter is a general second order lumped RC network. Only four external resistors program the AF160 for specific second order functions. Lowpass, highpass, and bandpass functions are available simultaneously at separate outputs. Notch and allpass functions are available by summing the outputs in the uncommitted output summing amplifier. Higher order systems are realized by cascading AF160 active filters with appropriate programming resistors.

Any of the classical filter configurations, such as Butterworth, Bessel, Cauer, and Chebyshev can be formed. The AF160 is pin compatible with the AF100J.

Features

- Military or commercial specification
- Independent Q, frequency, gain adjustments
- Low sensitivity to external component variation
- Separate lowpass, highpass, bandpass outputs
- Inputs may be differential, inverting, or non-inverting
- Allpass and notch outputs may be formed using uncommitted amplifier
- Operates to 40 kHz
- Q range to 500
- Power supply range ±5.0 V to ±18 V
- Frequency accuracy ±1% unadjusted
- Q frequency product ≤ 200,000
- BIFET™ input amplifier, pin compatible with AF100J

Connection Diagram



TOP VIEW

Ceramic Dual-In-Line Package
Order Numbers
AF160-1CJ, AF160-2CJ
NS Package Number HY13A

Absolute Maximum Ratings

Supply Voltage ±18V
Power Dissipation 900 mW/Package (500 mW/Amp)
Differential Input Voltage ±36V
Output Short Circuit Duration (Note 1) Infinite
Lead Temperature (Soldering, 10 seconds) 300°C

Operating Temperature
AF160-1CJ, AF160-2CJ, AF160-1CG, AF160-2CG −25°C to +85°C
AF160-1G, AF160-2G −55°C to +125°C
Storage Temperature
AF160-1G, AF160-2G −65°C to +125°C
AF160-1CG, AF160-2CG, AF160-1CJ, AF160-2CJ −25°C to +100°C

Electrical Characteristics (Complete Active Filter) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_C \times Q \leq 200{,}000$			100k	Hz
Q Range	$f_C \times Q \leq 200{,}000$			500	Hz/Hz
f_O Accuracy					
AF160-1, AF160-1C	$f_C \times Q \leq 40{,}000$, $T_A = 25°C$			±2.5	%
AF160-2, AF160-2C	$f_C \times Q \leq 40{,}000$, $T_A = 25°C$			±1.0	%
f_O Temperature Coefficient			±50	±150	ppm/°C
Q Accuracy	$f_C \times Q \leq 40{,}000$, $T_A = 25°C$			±7.5	%
Q Temperature Coefficient			±300	±750	ppm/°C
Power Supply Current	$V_S = ±15V$		7.2	11	mA

Electrical Characteristics (Internal Op Amp) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$, $T_A = 25°C$		5	10	mV
Input Offset Current	$T_J = 25°C$		25	100	pA
Input Bias Current			50	200	pA
Large Signal Voltage Gain	$R_L \geq 2k$, $V_{OUT} = ±10V$	25	100		V/mV
Output Voltage Swing	$R_L = 10\,k\Omega$	±12	±13.5		V
Input Voltage Range		±11	+15/−12		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$	70	100		dB
Slew Rate (Unity Gain)			13		V/μs
Small Signal Bandwidth			4		MHz

Note 1: Any of the amplifiers can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted, as the maximum junction temperature will be exceeded.

Note 2: Specifications apply for $V_S = ±15V$, over −25°C to +85°C for the AF160-1C and AF160-2C and over −55°C to +125°C for the AF160-1 and AF160-2, unless otherwise specified.

Note 3: Specifications apply for $V_S = ±15V$, $T_A = 25°C$.

Applications Information

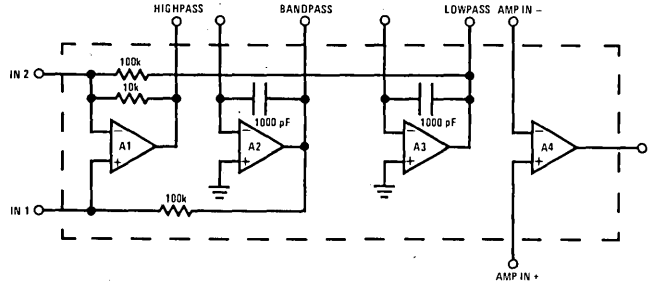


FIGURE 1. AF160 Schematic

CIRCUIT DESCRIPTION AND OPERATION

A schematic of the AF160 is shown in *Figure 1.* Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input. Amplifier A4 is an uncommitted amplifier.

By adding external resistors the circuit can be used to generate the second order system

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_0 = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_0}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(highpass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer function becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(bandpass)}$$

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(lowpass)}$$

Using proper input and output connections the circuit can also be used to generate the transfer functions for a notch and allpass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals 1, and a_3 equals ω_Z^2. The transfer function becomes:

$$T(s) = \frac{s^2 + \omega_Z^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(notch)}$$

In the allpass transfer function $a_1 = 1$, $a_2 = -\omega_0/Q$ and $a_3 = \omega_0^2$. The transfer function becomes:

$$T(s) = \frac{s^2 - \frac{\omega_0}{Q} s + \omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \qquad \text{(allpass)}$$

COMMON CONFIGURATIONS

The specific transfer functions for some of the most useful circuit configurations using the AF160 are illustrated in *Figures 2 through 8.* Also included are the gain equations for each transfer function in the frequency band of interest, the Q equation, center frequency equation and the Q determining resistor equation.

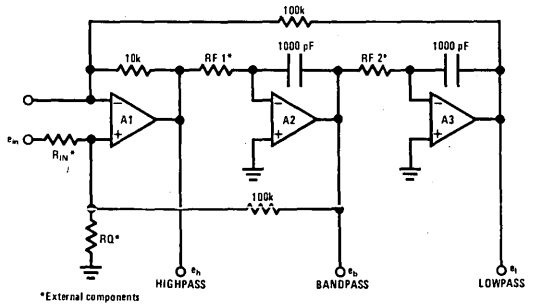


FIGURE 2. Non-inverting Input ($Q > Q_{MIN}$, See Q Tuning Section)

Applications Information (Continued)

a) Non-inverting input *(Figure 2)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left[\frac{1.1}{1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left[\frac{1.1}{1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}}\right]}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \omega_1\omega_2\left[\frac{\frac{1.1}{1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}}}{\Delta}\right] \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\left[\frac{1.1}{1+\frac{10^5}{RQ}+\frac{10^5}{R_{IN}}}\right]\omega_1 + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{11}{\left(1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}\right)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to \infty} = \frac{1.1}{\left(1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}\right)}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{\left(1+\frac{10^5}{RQ}+\frac{10^5}{R_{IN}}\right)}{\left(1+\frac{R_{IN}}{10^5}+\frac{R_{IN}}{RQ}\right)}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left(\frac{1+\frac{10^5}{R_{IN}}+\frac{10^5}{RQ}}{1.1}\right)\sqrt{0.1\left(\frac{\omega_2}{\omega_1}\right)}$$

$$RQ = \frac{10^5}{\left(\frac{1.1Q}{\sqrt{0.1\frac{\omega_2}{\omega_1}}}\right) - 1 - \frac{10^5}{R_{IN}}}$$

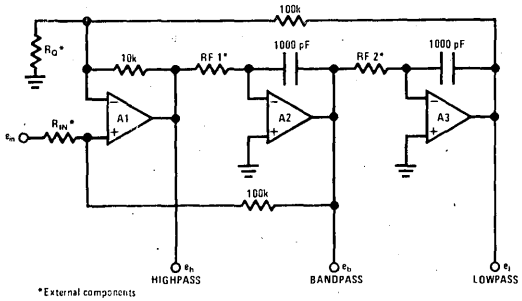


FIGURE 3. Non-Inverting Input ($Q < Q_{MIN}$, See Q Tuning Section)

b) Non-inverting input *(Figure 3)* transfer equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2\left[\frac{1.1+\frac{10^4}{RQ}}{1+\frac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1\left[\frac{1.1+\frac{10^4}{RQ}}{1+\frac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(bandpass)}$$

$$\frac{e_\ell}{e_{IN}} = \frac{\omega_1\omega_2\left[\frac{1.1+\frac{10^4}{RQ}}{1+\frac{R_{IN}}{10^5}}\right]}{\Delta} \quad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1\left[\frac{1.1+\frac{10^4}{RQ}}{1+\frac{10^5}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_\ell}{e_{IN}}\right|_{s\to 0} = \frac{1.1+\frac{10^4}{RQ}}{0.1\left(1+\frac{R_{IN}}{10^5}\right)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s\to \infty} = \frac{1.1+\frac{10^4}{RQ}}{1+\frac{R_{IN}}{10^5}}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega=\omega_0} = -\frac{1+\frac{10^5}{R_{IN}}}{1+\frac{R_{IN}}{10^5}}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1+\frac{10^5}{R_{IN}}}{1.1+\frac{10^4}{RQ}}\right]\sqrt{0.1\frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^4}{\left(1+\frac{10^5}{R_{IN}}\right)\left(\frac{\sqrt{0.1\frac{\omega_2}{\omega_1}}}{Q}\right) - 1.1}$$

Applications Information (Continued)

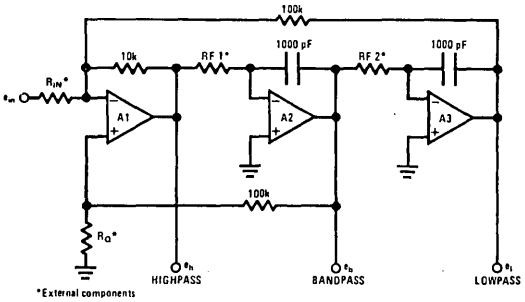


FIGURE 4. Inverting Input

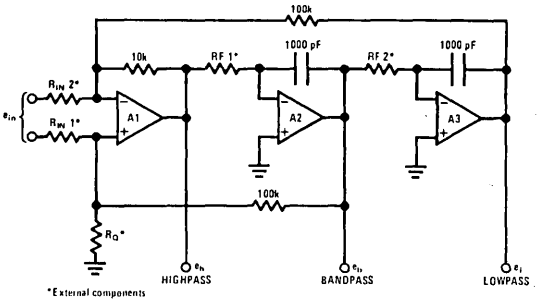


FIGURE 5. Differential Input

c) Inverting input *(Figure 4)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{-s^2 \dfrac{10^4}{R_{IN}}}{\Delta} \qquad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{s\,\omega_1 \dfrac{10^4}{R_{IN}}}{\Delta} \qquad \text{(bandpass)}$$

$$\frac{e_l}{e_{IN}} = \frac{-\omega_1\,\omega_2 \dfrac{10^4}{R_{IN}}}{\Delta} \qquad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \dfrac{10^4}{R_{IN}}}{1 + \dfrac{10^5}{R_Q}} \right] + 0.1\,\omega_1\omega_2$$

$$\left.\frac{e_l}{e_{IN}}\right|_{s \to 0} = -\frac{10^5}{R_{IN}} \qquad \text{(lowpass)}$$

$$\left.\frac{e_h}{e_{IN}}\right|_{s \to \infty} = -\frac{10^4}{R_{IN}} \qquad \text{(highpass)}$$

$$\left.\frac{e_b}{e_{IN}}\right|_{\omega = \omega_0} = \frac{\dfrac{10^4}{R_{IN}}\left(1 + \dfrac{10^5}{RQ}\right)}{1.1 + \dfrac{10^4}{R_{IN}}} \qquad \text{(bandpass)}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1 + \dfrac{10^5}{RQ}}{1.1 + \dfrac{10^4}{R_{IN}}} \right] \sqrt{0.1\,\frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^5}{\dfrac{Q}{\sqrt{0.1\,\dfrac{\omega_2}{\omega_1}}}\left(1.1 + \dfrac{10^4}{R_{IN}}\right) - 1}$$

d) Differential input *(Figure 5)* transfer function equations are:

$$\frac{e_h}{e_{IN}} = \frac{s^2 \dfrac{10^4}{R_{IN2}}}{\Delta} \qquad \text{(highpass)}$$

$$\frac{e_b}{e_{IN}} = \frac{-s\,\omega_1 \dfrac{10^4}{R_{IN2}}}{\Delta} \qquad \text{(bandpass)}$$

$$\frac{e_l}{e_{IN}} = \frac{\omega_1\,\omega_2 \dfrac{10^4}{R_{IN2}}}{\Delta} \qquad \text{(lowpass)}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

where

$$\Delta = s^2 + s\,\omega_1 \left[\frac{1.1 + \dfrac{10^4}{R_{IN2}}}{1 + \dfrac{10^5}{RQ} + \dfrac{10^5}{R_{IN1}}} \right] + 0.1\,\omega_1\omega_2$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$Q = \left[\frac{1 + \dfrac{10^5}{RQ} + \dfrac{10^5}{R_{IN1}}}{1.1 + \dfrac{10^4}{R_{IN2}}} \right] \sqrt{0.1\,\frac{\omega_2}{\omega_1}}$$

$$RQ = \frac{10^5}{\dfrac{Q}{\sqrt{0.1\,\dfrac{\omega_2}{\omega_1}}}\left(1.1 + \dfrac{10^4}{R_{IN2}}\right) - 1 - \dfrac{10^5}{R_{IN1}}}$$

Applications Information (Continued)

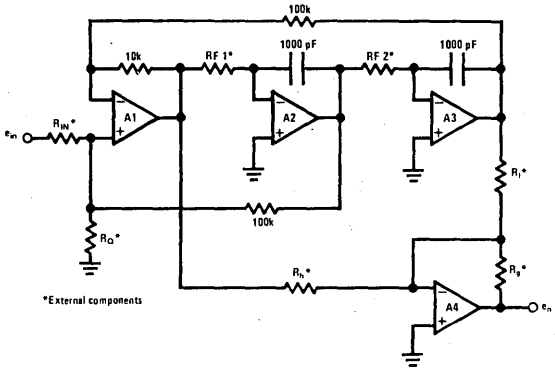


FIGURE 6. Output Notch Using All Four Amplifiers

e) Output notch *(Figure 6)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = \frac{(s^2 + \omega_Z^2)\left[\frac{1.1}{1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}}\right]\frac{R_g}{R_h}}{s^2 + s\,\omega_1\left[\frac{1.1}{1 + \frac{10^5}{RQ} + \frac{10^5}{R_{IN}}}\right] + 0.1\,\omega_1\omega_2}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}} \qquad \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\omega_Z = \omega_0\sqrt{\frac{10\,R_h}{R_\ell}}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to 0} = \frac{11}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}\right)}\frac{R_g}{R_\ell}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{s \to \infty} = \frac{1.1}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{RQ}\right)}\frac{R_g}{R_h}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega = \omega_Z} = 0$$

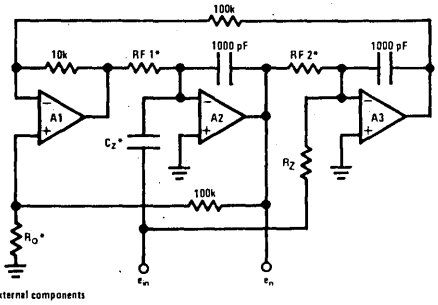


FIGURE 7. Input Notch Using Three Amplifiers

j) Input notch *(Figure 7)* transfer function equations are:

$$\frac{e_n}{e_{IN}} = -\frac{\frac{C_Z}{10^{-9}}\left[s^2 + \omega_Z^2\right]}{s^2 + s\,\omega_1\left[\frac{1.1\,RQ}{10^5 + RQ}\right] + \omega_0^2}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

$$\omega_Z = \omega_0\sqrt{\frac{RF2 \times 10^{-9}}{R_Z\,C_Z}} \qquad \omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to 0} = -\frac{R_{F2}}{R_Z}$$

$$\left.\frac{e_n}{e_{IN}}\right|_{\omega \to \infty} = -\frac{C_Z}{10^{-9}}$$

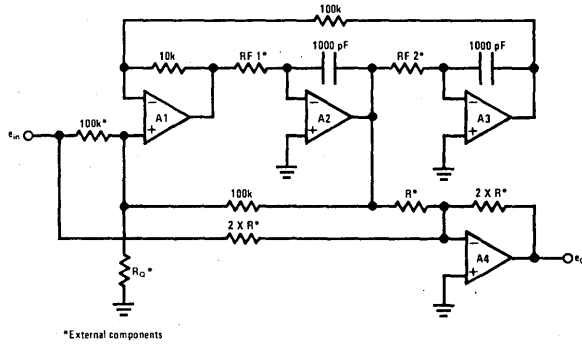


FIGURE 8. Allpass

g) Allpass *(Figure 8)* transfer function equations are:

$$\frac{e_o}{e_{IN}} = -\left[\frac{s^2 - s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{RQ}}\right] + \omega_0^2}{s^2 + s\,\omega_1\left[\frac{1.1}{2 + \frac{R_{IN}}{RQ}}\right] + \omega_0^2}\right]$$

$$Q = \frac{2 + \frac{10^5}{RQ}}{1.1}\sqrt{0.1\frac{\omega_2}{\omega_1}}$$

$$\omega_1 = \frac{10^9}{R_{F1}} \qquad \omega_2 = \frac{10^9}{R_{F2}}$$

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2}$$

Time delay at $\omega_0 = \frac{2Q}{\omega_0}$ seconds

FREQUENCY TUNING

To tune the AF160 two resistors are required for frequencies between 200 Hz and 10 kHz. For lower frequencies "T" tuning or addition of external capacitors

Applications Information (Continued)

is required. Using external capacitors allows the user to go as low in frequency as he desires. "T" tuning and external capacitors can be used together.

Two resistor tuning for 200 Hz to 10 kHz

$$R_f = \frac{50.33 \times 10^6}{f_o}\ \Omega$$

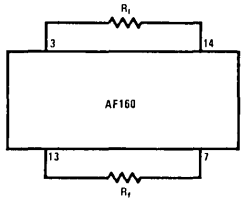
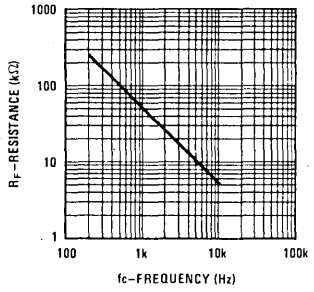


FIGURE 9. Resistive Tuning

GRAPH A. Resistive Tuning



"T" resistive tuning for $f_O < 200$ Hz

$$R_s = \frac{R_t^2}{R_f - 2R_t} \qquad R_t < \frac{R_F}{2}$$

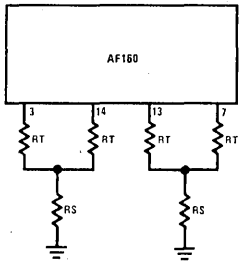
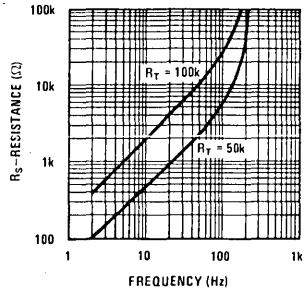


FIGURE 10. T Tuning

GRAPH B. "T" Tuning



RC tuning for $f_O < 200$ Hz

$$R_f = \frac{0.05033}{f_o\,(C + 1 \times 10^{-9})}$$

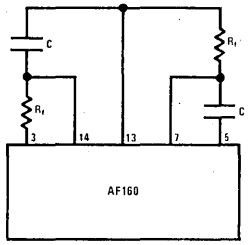
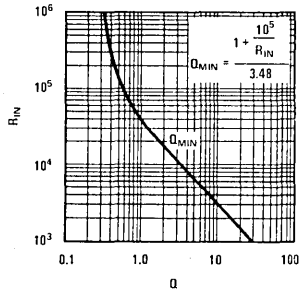


FIGURE 11. Low Frequency RC Tuning

Q TUNING

To tune the Q of an AF160 requires one resistor from pins 1 or 2 to ground. The value of the Q tuning resistor depends on the input connection and input resistance as well as the value of the Q. The Q of the unit is inversely proportional to resistance to ground at pin 1 and directly proportional to resistance to ground from pin 2.

GRAPH C. Q_{MIN}, Non-Inverting Input



For $Q > Q_{MIN}$ in non-inverting mode:

$$RQ = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}}$$

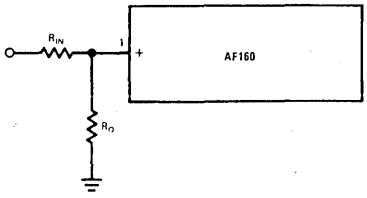
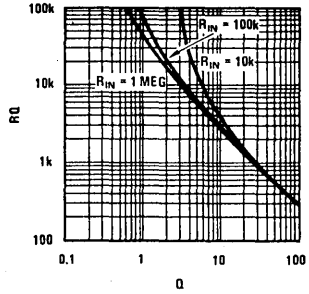


FIGURE 12. Q Tuning for $Q > Q_{MIN}$, Non-Inverting Input

Applications Information (Continued)

GRAPH D. Q > Q_{MIN}, Non-Inverting Input



For $Q < Q_{MIN}$ in non-inverting mode:

$$RQ = \frac{10^4}{0.3162 \left(\frac{\left(1 + \frac{10^5}{R_{IN}}\right)}{Q}\right) - 1.1}$$

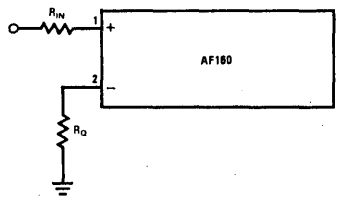
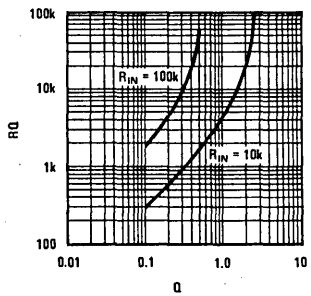


FIGURE 13. Q Tuning for $Q < Q_{MIN}$, Non-Inverting Input

GRAPH E. Q < Q_{MIN}, Non-Inverting Input



For any Q in inverting mode:

$$RQ = \frac{10^5}{3.16Q \left(1.1 + \frac{10^4}{R_{IN}}\right) - 1}$$

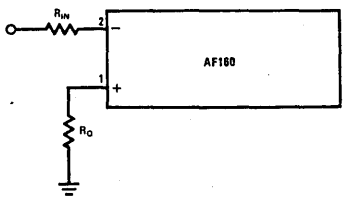
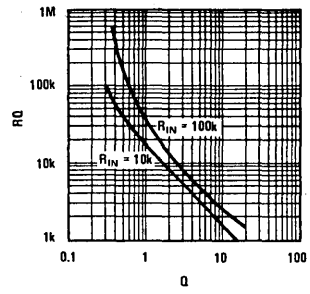


FIGURE 14. Q Tuning Inverting Input

GRAPH F. Q Tuning, Inverting Input



NOTCH TUNING

Two methods to generate notches are the RC input and lowpass/highpass summing. The RC input method requires adding a capacitor and resistor connected to the two integrator inputs. The capacitor connects to "Int 1" and the resistor connects to "Int 2." The output summing requires two resistors connected to the lowpass and highpass output.

For input RC notch tuning:

$$R_Z = \frac{R_F \times 10^{-9}}{C_Z} \left(\frac{f_O}{f_Z}\right)^2$$

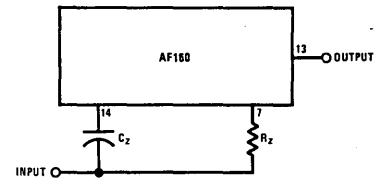
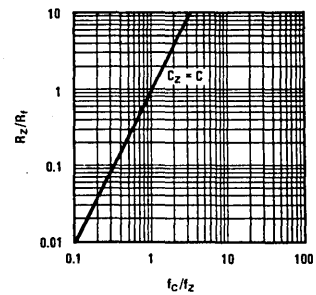


FIGURE 15. Input RC Notch

GRAPH G. Input RC Notch



For output notch tuning:

$$R_{HP} = \left(\frac{f_Z}{f_O}\right)^2 \frac{R_{LP}}{10}$$

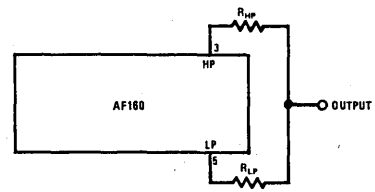
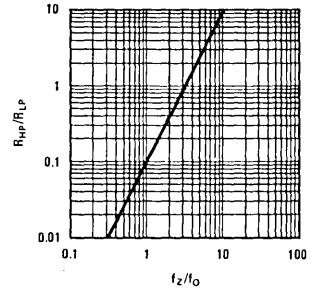


FIGURE 16. Output Notch

Applications Information (Continued)

GRAPH H. Output Notch



TUNING TIPS

In applications where 2 to 3% accuracy is not sufficient to provide the required filter response, the AF160 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the bandpass (pin 13) output.

Before any tuning is attempted the lowpass (pin 7) output should be checked to see that the output is not clipping. At the center frequency of the section the lowpass output is 10 dB higher than the bandpass output and 20 dB higher than the highpass. This should be kept in mind because if clipping occurs the results obtained when tuning will be incorrect.

Frequency Tuning

By adjusting the resistance between pins 7 and 13 the center frequency of a section can be adjusted. If the input is through pin 1 the phase shift at center frequency will be 180° and if the input is through pin 2 the phase shift at center frequency will be 0°. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

"Q" Tuning

The "Q" is tuned by adjusting the resistance between pin 1 or 2 and ground. Low Q tuning resistors will be from pin 2 to ground ($Q < 0.6$). High Q tuning resistors will be from pin 1 to ground. To tune the Q correctly the signal source must have an output impedance very much lower than the input resistance of the filter since the input resistance affects the Q. The input must be driven through the same resistance the circuit will see to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right) \times (f_O)$$

where f_O = center frequency

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q} \right) \times (f_O)$$

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair the notch can be tuned by adjusting the ratio of the summing resistors (lowpass/highpass summing) or the input resistance (input RC).

In either case the signal is connected to the input and the proper resistor is adjusted for a null at the output.

Special Cases

When using the input RC notch the unit cannot be tuned through the normal input so an additional 100k resistor can be added at pin 1 and the unit can be tuned normally. Then the 100k input resistor should be grounded and the notch tuned through the normal RC input.

An alternative way of tuning is to tune using the Q resistor as the input. This requires the Q resistor be lifted from ground and connecting the signal source to the normally grounded end of the Q resistor. This has the problem that when the Q resistor is grounded after tuning, its value is decreased by the output impedance of the source. This technique has the advantage of not requiring an additional resistor.

TUNING PROCEDURE (See *Figure 17*)

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the lowpass output pin 5.

Adjust the resistance between pins 13 and 7 until the phase shift between input and bandpass output is 180°.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

Zero Tuning

Set the oscillator output to the zero frequency and tune the zero resistor for a null at the output of the summing amplifier.

Gain Adjust

Set the oscillator to any desired frequency and the gain can be adjusted by measuring the output of the summing amplifier and adjusting the feedback resistance.

Applications Information (Continued)

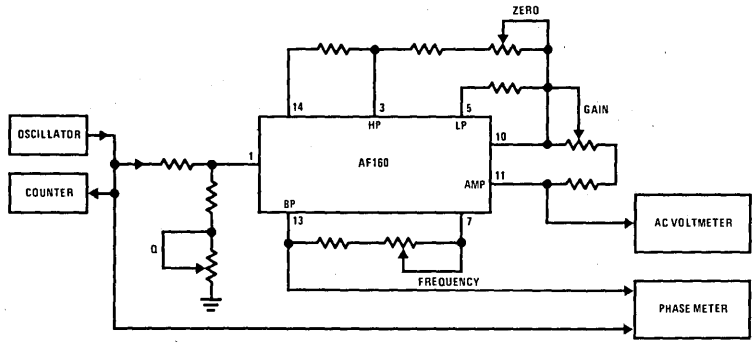


FIGURE 17. Filter Tuning Setup

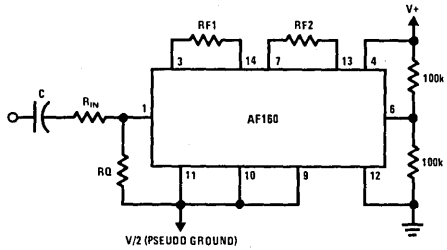


FIGURE 18. Single Power Supply Connection Using Uncommitted Amplifier to Split Supply

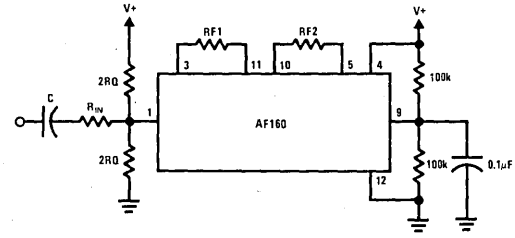
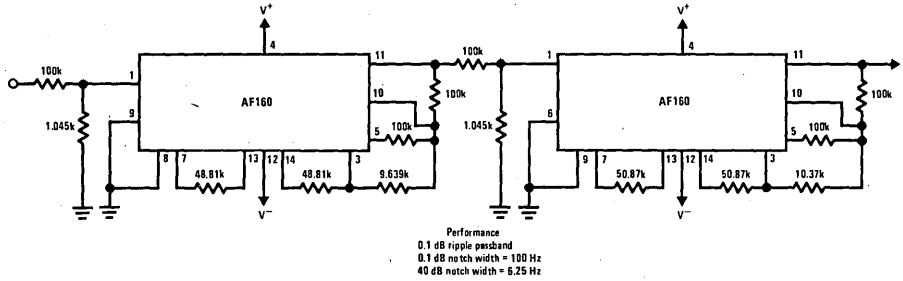


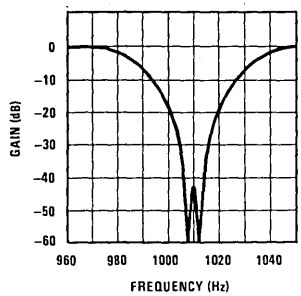
FIGURE 19. Single Power Supply Connection Using Resistive Dividers



4th Order 1010 Hz Notch

STAGE 1

F_c = 1031.1 Hz
Q = 28.34
F_z = 1012.2 Hz



STAGE 2

F_c = 989.3 Hz
Q = 28.34
F_z = 1007.8 Hz

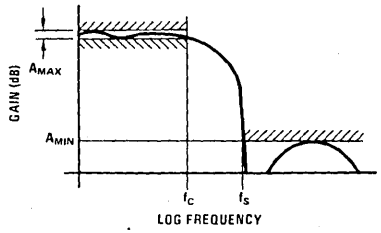
FIGURE 20. 1010 Hz Notch—Telephone Holding Tone Reject Filter

FILTER DESIGN

Since most filter tables are in terms of a normalized lowpass prototype, the filter to be designed is usually reduced to a lowpass prototype. After the lowpass transfer function is found, it is transformed to obtain the transfer function for the actual filter desired. *Graph I* shows the lowpass amplitude response which can be defined by four quantities.

Applications Information (Continued)

GRAPH I. Lowpass Prototype Response



A_{MAX} = the maximum peak to peak ripple in the passband.

A_{MIN} = the minimum attenuation in the stopband.

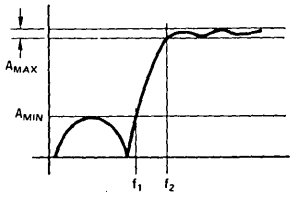
f_C = the passband cutoff frequency.

f_S = the stopband start frequency.

By defining these four quantities for the lowpass prototype the normalized pole and zero locations and the Q (quality) of the poles can be determined from tables or by computer programs.

To obtain the lowpass prototype for the highpass filter (*Graph J*) A_{MAX} and A_{MIN} are the same as for the lowpass case but $f_C = 1/f_2$ and $f_S = 1/f_1$.

GRAPH J. Highpass Response



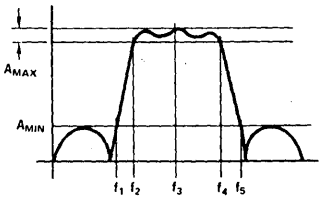
To obtain the lowpass prototype for a bandpass filter (*Graph K*) A_{MAX} and A_{MIN} are the same as for the lowpass case but

$$f_C = 1 \quad f_S = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 f_5} = \sqrt{f_2 f_4}$ i.e. geometric symmetry

$f_5 - f_1$ = A_{MIN} bandwidth
$f_4 - f_2$ = Ripple bandwidth

GRAPH K. Bandpass Response

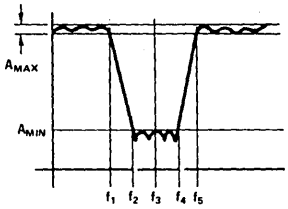


To obtain the lowpass prototype for the notch filter (*Graph L*) A_{MAX} and A_{MIN} are the same as for the lowpass case and

$$f_C = 1 \qquad f_S = \frac{f_5 - f_1}{f_4 - f_2}$$

where $f_3 = \sqrt{f_1 f_5} = \sqrt{f_2 f_4}$

GRAPH L. Notch Response



Normalized Lowpass Transformed To Un-Normalized Lowpass

The normalized lowpass filter has the passband edge normalized to unity. The un-normalized lowpass filter instead has the passband edge at f_C. The normalized and un-normalized lowpass filters are related by the transformation $s = s\omega_c$. This transforms the normalized passband edge $s = j$ to the un-normalized passband edge $s = j\omega_C$.

Normalized Lowpass Transformed To Un-Normalized Highpass

The transformation that can be used for lowpass to highpass is $S = \omega_C/s$. Since S is inversely proportional to s, the low frequency and high frequency responses are interchanged. The normalized lowpass $1/(S^2 + S/Q+1)$ transforms to the un-normalized highpass

$$\frac{s^2}{s^2 + \frac{\omega_C}{Q}s + \omega_C{}^2}$$

Normalized Lowpass Transformed To Un-Normalized Bandpass

The transformation that can be used for lowpass to bandpass is $S = (s^2 + \omega_0{}^2)$ BWs where $\omega_0{}^2$ is the center frequency of the desired bandpass filter and BW is the ripple bandwidth.

Normalized Lowpass Transformed To Un-Normalized Bandstop (Or Notch)

The bandstop filter has a reciprocal response to a bandpass filter. Therefore a bandstop filter can be obtained by first transforming the lowpass prototype to a highpass and then performing the bandpass transformation.

SELECTION OF TRANSFER FUNCTION

The selection of a function which approximates the shape of the response desired is a complicated process. Except in the simplest cases it requires the use of tables or computer programs. The form of the transfer function desired is in terms of the pole and zero locations. The most common approximations found in tables are Butterworth, Tschebycheff, Elliptic, and Bessel. The decision as to which approximation to use is usually a function of the requirements and system objectives. Butterworth filters are the simplest but have the disadvantage of requiring high order transfer functions to obtain sharp roll-offs.

Applications Information (Continued)

The Tschebycheff function is a min/max approximation in the passband. This approximation has the property that it is equiripple which means that the error oscillates between maximums and minimums of equal amplitude in the passband. The Tschebycheff approximation, because of its equiripple nature, has a much steeper transition region than the Butterworth approximation.

The elliptic filter, also known as Cauer or Zolotarev filters, are equiripple in the passband and stopband and have a steeper transition region than the Butterworth or the Tschebycheff.

For a specific lowpass filter three quantities can be used to determine the degree of the transfer function: the maximum passband ripple, the minimum stopband attenuation, and the transition ratio ($tr = \omega_S/\omega_C$). Decreasing A_{MAX}, increasing A_{MIN}, or decreasing tr will increase the degree of the transfer function. But for the same requirements the elliptic filter will require the lowest order transfer function. Tables and graphs are available in reference books such as "Reference Data for Radio Engineers," Howard W. Sams & Co., Inc., 5th Edition, 1970 and Erich Christian and Egon Eisenmann, "Filter Design Tables and Graphs," John Wiley and Sons, 1966.

For specific transfer functions and their pole locations such text as Louis Weinberg, "Network Analysis and Synthesis," McGraw Hill Book Company, 1962 and Richard W. Daniels, "Approximation Methods for Electronic Filter Design," McGraw-Hill Book Company, 1974, are available.

DESIGN OF CASCADED MULTISECTION FILTERS

The first step in designing is to define the response required and define the performance specifications:

1. Type of filter:
   Lowpass, highpass, bandpass, notch, allpass
2. Attenuation and frequency response
3. Performance
   Center frequency/corner frequency plus tolerance and stability
   Insertion loss/gain plus tolerance and stability
   Source impedance
   Load impedance
   Maximum output noise
   Power consumption
   Power supply voltage
   Dynamic range
   Maximum output level

Second step is to find the pole and zero location for the transfer function which meet the above requirements. This can be done by using tables and graphs or network synthesis. The form of the transfer function which is easiest to convert to a cascaded filter is a product of first and second order terms in these forms:

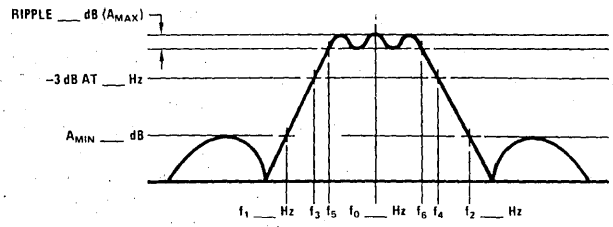
First Order	Second Order	
$\frac{K}{s+\omega_R}$	$\frac{K}{s^2+\frac{\omega_0}{Q}s+\omega_0{}^2}$	(low pass)
$\frac{Ks}{s+\omega_R}$	$\frac{Ks^2}{s^2+\frac{\omega_0}{Q}s+\omega_0{}^2}$	(highpass)
	$\frac{Ks}{s^2+\frac{\omega_0}{Q}s+\omega_0{}^2}$	(bandpass)
	$\frac{K(s^2+\omega_Z{}^2)}{s^2+\frac{\omega_0}{Q}s+\omega_0{}^2}$	(notch)
	$\frac{s^2-\frac{\omega_0}{Q}s+\omega_0{}^2}{s^2+\frac{\omega_0}{Q}s+\omega_0{}^2}$	(allpass)

Each of the second order functions is realizable by tuning an AF160 stage. By cascading these stages the desired transfer function is realized.

CASCADING SECOND ORDER STAGES

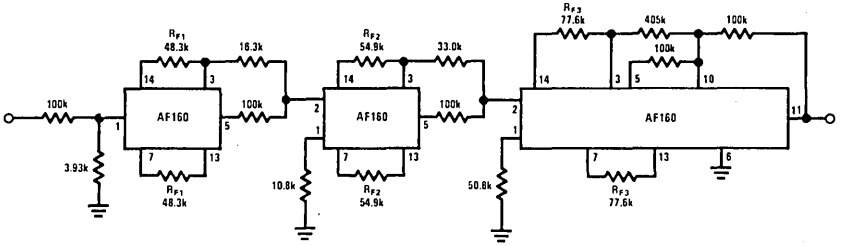
The primary concern in cascading second order stages is to minimize the maximum difference in amplitude from input to output over the frequencies of interest. A computer program is probably required in very complicated cases but some general rules that can be used that will usually give satisfactory results are:

GRAPH M. Generalized Model Response



Applications Information (Continued)

1. The highest "Q" pole pair should be paired with the zero pair closest in frequency.
2. If highpass and lowpass stages are cascaded the lowpass sections should be the higher frequency and highpass sections the lower frequency.
3. In cascaded filters of more than two sections the first section should be the section with "Q" closest to 0.707 and then additional stages should be added in order of least difference between first stage Q and their Q.



Lowpass Elliptic Filter

$F_C = 1$

$F_S = 1.3$

$A_{MAX} = 0.1$ dB

$A_{MIN} = 40$ dB

$N = 6$

$f_{O1} = 1.0415 \quad Q_1 = 7.88 \quad f_{Z1} = 1.329 \quad f_Z/f_O = 1.28 \quad \left(\frac{f_Z}{f_O}\right)^2 = 1.63$

$f_{O2} = 0.9165 \quad Q_2 = 1.79 \quad f_{Z2} = 1.664 \quad f_Z/f_O = 1.82 \quad \left(\frac{f_Z}{f_O}\right)^2 = 3.30$

$f_{O3} = 0.649 \quad Q_3 = 0.625 \quad f_{Z3} = 4.1285 \quad f_Z/f_O = 6.36 \quad \left(\frac{f_Z}{f_O}\right)^2 = 40.5$

$$R_{F1} = \frac{(503.3)}{f_{O1} \times f_C} \times 10^5 \qquad R_{F2} = \frac{(503.3)}{f_{O2} \times f_C} \times 10^5 \qquad R_{F3} = \frac{(503.3)}{f_{O3} \times f_C}$$

at 1000 Hz = f_C

$R_{F1} = 48.3k \qquad R_{F2} = 54.9k \qquad R_{F3} = 77.6k$

6th Order Elliptic Filter

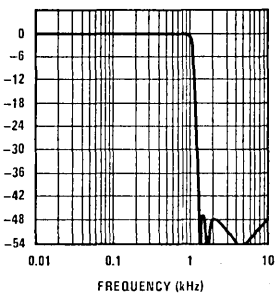


FIGURE 21. Lowpass Elliptic Filter Example

Applications Information (Continued)

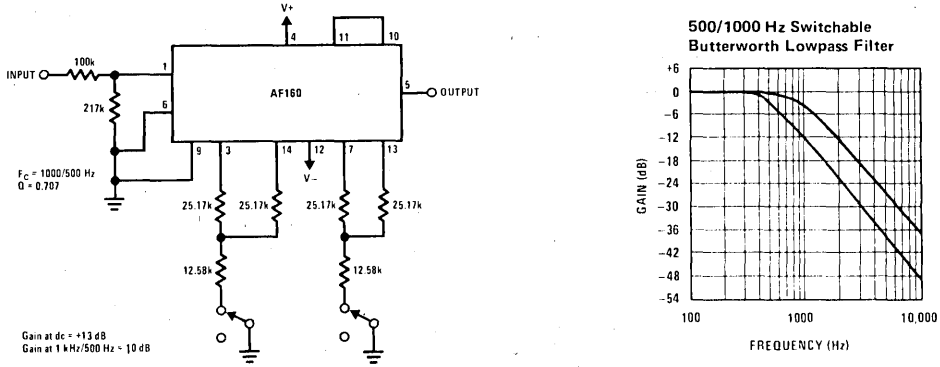
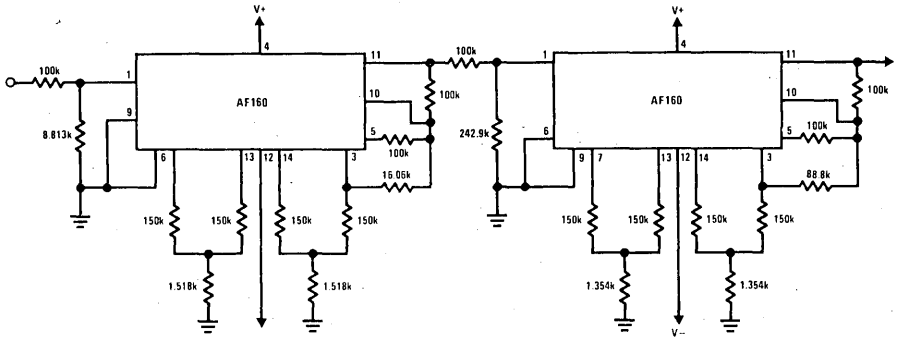
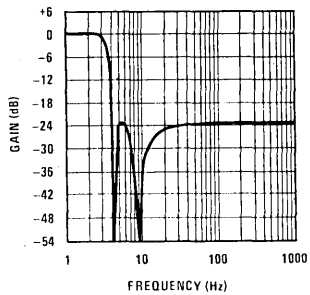


FIGURE 22. Switchable Filter Example: 500 Hz/1000 Hz Butterworth Lowpass





STAGE 1

F_C = 3.328 Hz
Q = 3.84
F_Z = 4.218 Hz

STAGE 2

F_C = 2.975 Hz
Q = 0.693
F_Z = 8.865 Hz

FIGURE 23. EEG Delta Filter–3 Hz Lowpass

Applications Information (Continued)

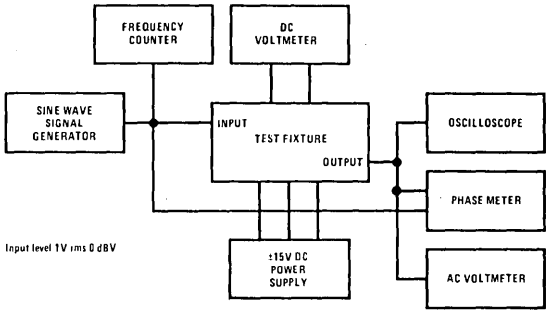


FIGURE 25. Test Circuit Block Diagram

COMPUTER AIDED DESIGN EXAMPLE*

This design is an example of a 60 Hz notch filter. The response is to have the following specifications:

Maximum passband ripple 0.1 dB

Minimum rejection 35 dB

0.1 dB bandwidth 15 Hz max

−35 dB bandwidth 1.5 Hz min

The steps in the design of this filter are:

1. Design a lowpass "prototype" for the filter.
2. Transformation of the lowpass prototype into a notch filter design.
3. Using the pole and zero locations found in step two calculate the value of the resistors required to build the filter.
4. Draw a schematic of filter using values obtained in step three.

*Computer programs shown are user interactive. Underlined copy is user input, non-underlined copy is computer response, and line indications in parenthesis are included for easy identification of data common to several programs.

PROGRAM NO. 1

```
RUN

THIS PROGRAM DESIGNS BUTTERWORTH CHEBYCHEFF OR ELLIPTIC NORMALIZED
LOWPASS FILTERS
WHAT TYPE OF FILTER ? B-C-E

ELLIPTIC
 DO YOU KNOW THE ORDER OF THE FILTER ? Y/N
? NO
INPUT FC,FS,AMAX,AMIN
? 1, 10, .1, 35
     FC                  1.000
     FS                 10.000
     AMAX                 .100
     AMIN               35.000
     N                   2.000
     ATT AT FS         −35.671     (ATTENUATION IN dB)
IS THIS SATISFACTORY ? Y/N
? YES

   F                   Q
    1.823 (Line 1.1)       .775 (Line 1.2)
   Z
   14.124 (Line 1.3)
```

Applications Information (Continued)

PROGRAM NO. 2
(DETERMINES UN-NORMALIZED POLE + ZERO LOCATIONS OF FIRST SECTION)
(DATA ENTERED FROM PROGRAM NO. 1)

```
RUN
WHAT TYPE FILTER BANDPASS OR NOTCH
? NOTCH
ENTER # OF POLE PAIRS? 1

ENTER # OF JW AXIS ZEROS? 1

  ENTER # OF REAL POLES? 0

  ENTER # OF ZEROS AT ZERO? 0

  ENTER # OF COMPLEX ZEROS? 0

ENTER # OF REAL ZEROS? 0

   ENTER F & Q OF EACH POLE PAIR
? 1.823, .775  (FROM LINE 1.1 AND LINE 1.2)

ENTER VALUES OF JW AXIS ZEROS
? 14.124  (FROM LINE 1.3)

ENTER FREQUENCY SCALING FACTOR
? 1
  ENTER THE # OF FILTERS TO BE DESIGNED
? 1
  ENTER THE C.F. AND BW OF EACH FILTER
? 60, 15
```

OUTPUT OF PROGRAM NO. 2
TRANSFORMED POLE/ZERO LOCATIONS
FIRST SECTION

POLE LOCATIONS

CENTER FREQ.		Q	
56.93601	*(From Line 2.3)*	11.31813	*(From Line 2.4)*
63.228877	*(From Line 2.5)*	11.31813	*(From Line 2.6)*

JW AXIS ZEROS

59.471339 *(From Line 2.1)*
60.533361 *(From Line 22*

PROGRAM NO. 3
(CHECK OF FILTER RESPONSE USING PROGRAM NO. 2 DATA BASE)

```
RUN

NUMERATOR (ZEROS)
A(I)S^2+R(I)S+Z(I)^2
 1     0     59.471339     (From Line 2.1)
 1     0     60.533361     (From Line 2.2)

REAL POLE

COMPLEX POLE PAIRS

        F          Q
1     56.93601   11.31813   (From Lines 2.3 and 2.4)
2     63.228877  11.31813   (From Lines 2.5 and 2.6)
```

RUN

FREQUENCY	NOR. GAIN (DB)	PHASE	DELAY	NOR. DELAY	FREQUENCY	NOR. GAIN (DB)	PHASE	DELAY	NOR. DELAY
40.000	.032	347.69	.002275	5.847169	60.600	−47.102	169.17	.050801	108.232021
45.000	.060	342.20	.004107	8.749738	60.800	−33.650	165.48	.051677	110.096278
50.000	.100	330.70	.009983	21.268142	61.000	−27.577	161.72	.052809	112.508334
55.000	−.795	290.54	.046620	99.324027	61.200	−23.418	157.87	.054167	115.403169
56.000	−2.298	270.61	.063945	136.234562	61.400	−20.198	153.92	.055712	118.694436
57.000	−5.813	245.51	.072894	155.299278	61.600	−17.554	149.85	.057391	122.270086
58.000	−12.748	220.19	.065758	140.096912	61.800	−15.308	145.65	.059136	125.989157
58.200	−14.740	215.54	.063369	135.006390	62.000	−13.362	141.33	.060869	129.681062
58.400	−17.032	211.06	.060979	129.914831	63.000	−6.557	118.23	.065975	140.559984
58.600	−19.722	206.76	.058692	125.043324	64.000	−2.936	95.30	.059402	126.556312
58.800	−22.983	202.61	.056588	120.561087	65.000	−1.215	76.38	.045424	96.774832
59.000	−27.172	198.60	.054724	116.589928	66.000	−.463	62.43	.032614	69.484716
59.200	−33.235	194.72	.053139	113.212012	67.000	−.138	52.44	.023498	50.062947
59.400	−46.300	190.94	.051856	110.478482	70.000	.091	35.43	.010452	22.267368
59.600	−42.909	7.24	.050888	108.417405	75.000	.085	23.44	.004250	9.054574
59.800	−36.897	3.60	.050242	107.040235	80.000	.060	17.80	.002310	4.921727
60.00	−35.567	360.00	.049916	106.346516	85.000	.043	14.50	.001460	3.110493
60.200	−36.887	356.41	.049907	106.326777	90.000	.032	12.31	.001011	2.154297
60.400	−42.757	352.81	.050206	106.963750					

Applications Information (Continued)

PROGRAM NO. 4

DESIGN OF FIRST SECTION

```
)RUN
WHICH FILTER AF160-J OR G ?
? J
WHAT TYPE OF FILTER SECTION? HIGHPASS-BANDPASS-LOWPASS-NOTCH-ALLPASS
? NOTCH
INPUT FC AND Q VALUES
? 56.93601, 11.31813  (FROM LINES 2.3 AND 2.4)
INPUT REAL POLE AND CAPACITOR VALUES IF NONE ENTER 0
? 0
INPUT ZERO LOCATION
? 59.471339      (FROM LINE 2.1)
ARE TUNING INSTRUCTIONS REQUIRED ?
? YES
```

TUNING INSTRUCTION

PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 180 DEG. AT 56.93601 HZ.
IF TUNING IS REQUIRED, RF2 FROM PINS 7 TO 13 SHOULD BE ADJUSTED.
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 135 DEG. AT 59.506798HZ.
OR 225 DEG. AT 54.476284 HZ.
IF TUNING IS REQUIRED RQ FROM 1 OR 2 TO GROUND SHOULD BE ADJUSTED
GAIN AT PIN 11 AT 59.471339 SHOULD BE 0 IF NOT
ADJUST RHP FROM PIN 3 TO 10 FOR NULL

FC= 56.93601 Q= 11.31813 F(L-3DB) = 54.476284 F(H-3DB) = 59.506798

GAIN AT F)) FC= .00DB

FUNCTION	CONNECTION FROM	TO	VALUE OF EXTERNAL RESISTORS IN OHMS
R IN	INPUT	1	100000.000
RQ	1	GND	2675.931
RF1	3	14	883960.996
RF2	7	13	883960.996
RLP	5	10	100000.000
RHP	3	10	10910.418
RG	10	11	357910.697
+V		4	
-V		12	
GND		9	
GND		6	
OUTPUT	PIN 11		

Applications Information (Continued)

PROGRAM NO. 4

DESIGN OF SECOND SECTION

WHAT TYPE OF FILTER SECTION? HIGHPASS-BANDPASS-LOWPASS-NOTCH-ALLPASS
? NOTCH
INPUT FC AND Q VALUES
? 63.228877, 11.31813 *(FROM LINES 2.5 AND 2.6)*
INPUT REAL POLE AND CAPACITOR VALUES IF NONE ENTER 0
? 0
INPUT ZERO LOCATION
? 60.533361 *(FROM LINE 2.2)*
ARE TUNING INSTRUCTIONS REQUIRED ?
? YES

TUNING INSTRUCTION

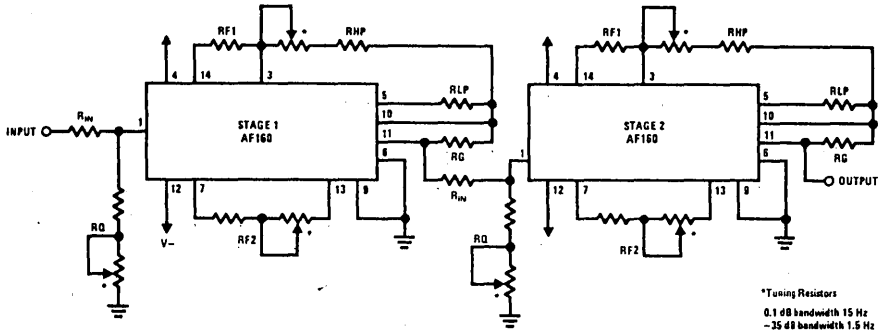
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 180 DEG. AT 63.228877 HZ.
IF TUNING IS REQUIRED RF2 FROM PINS 7 TO 13 SHOULD BE ADJUSTED
PHASE SHIFT FROM INPUT TO PIN 13 SHOULD BE 135 DEG. AT 66.083802 HZ.
OR 225 DEG. AT 60.497289 HZ.
IF TUNING IS REQUIRED RQ FROM 1 OR 2 TO GROUND SHOULD BE ADJUSTED
GAIN AT PIN 11 AT 60.533361 SHOULD BE 0 IF NOT
ADJUST RHP FROM PIN 3 TO 10 FOR NULL

FC= 63.228877 Q= 11.31813 F(L-3DB)= 60.497289 F(H-3DB)= 66.083802

GAIN AT F((FC= .00DB

FUNCTION	CONNECTION FROM	CONNECTION TO	VALUE OF EXTERNAL RESISTORS IN OHMS
R IN	INPUT	1	100000.000
RQ	1	GND	2675.931
RF1	3	14	795984.596
RF2	7	13	795984.596
RLP	5	10	100000.000
RHP	3	10	9165.552
RG	10	11	328044.920
+V		4	
-V		12	
GND		9	
GND		6	
OUTPUT	PIN 11		

Applications Information (Continued)



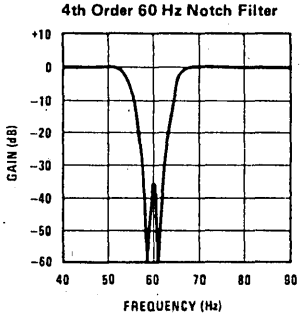


FIGURE 26. Implementation of a 60 Hz Notch From Computer Calculations

DEFINITION OF TERMS

A_{MAX}	Maximum passband peak-to-peak ripple
A_{MIN}	Minimum stopband loss
f_Z	Frequency of jw axis pair
f_O	Frequency of complex pole pair
Q	Quality of pole
f_C	Passband edge
f_S	Stopband edge
A_{HP}	Gain from input to highpass output
A_{BP}	Gain from input to bandpass output
A_{LP}	Gain from input to lowpass output
A_{AMP}	Gain from input to output of amplifier
R_f	Pole frequency determining resistance
R_Z	Zero Frequency determining resistance
R_Q	Pole Quality determining resistance
f_H	Frequency above center frequency at which the gain decreases by 3 dB for a bandpass filter
f_L	Frequency below center frequency at which the gain decreases by 3 dB for a bandpass filter
BW	The bandwidth of a bandpass filter
N	Order of the denominator of a transfer function

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E. Christian and E. Eisenmann, *"Filter Design Tables and Graphs,"* John Wiley & Sons, New York, 1966

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National Semiconductor

Active Filters

PRELIMINARY

AF161 Dual Universal Active Filter

General Description

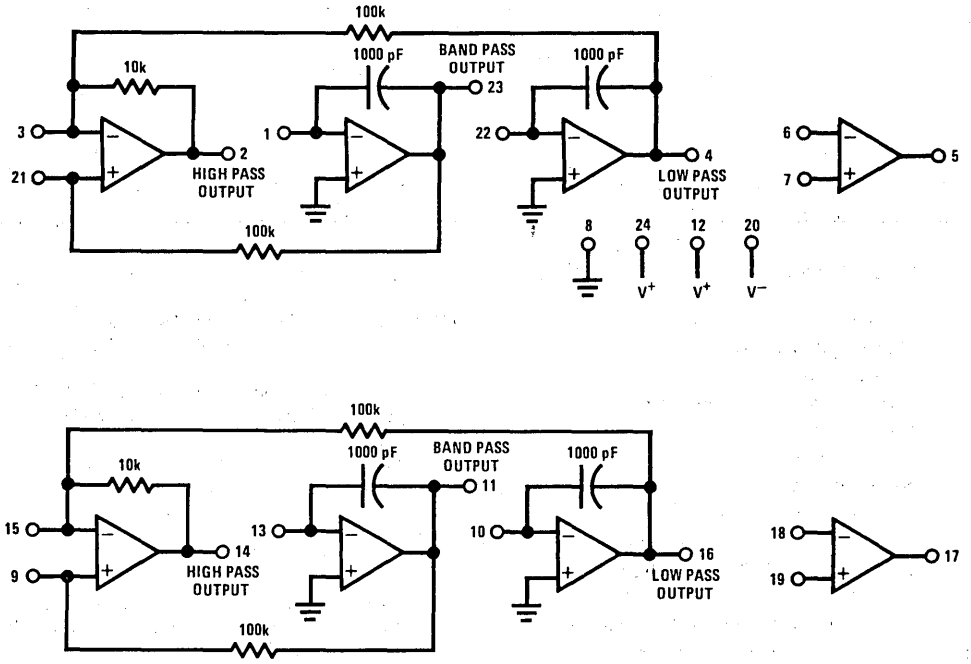
The AF161 consists of 2 general purpose state variable active filters in a single package. By using only 4 external resistors for each section, various second order functions may be formed. Low pass, high pass, and band pass functions are avaiable simultaneously at separate outputs. In addition, there are 2 uncommitted operational amplifiers which are available for buffering or for forming all pass and notch functions. Any of the classical filter configurations, such as Butterworth, Bessel, Cauer, and Chebyshev can be easily formed. The AF161 is pin compatible with the AF151.

BIFET is a trademark of National Semiconductor Corporation

Features

- Independent Q, frequency and gain adjustment
- Very low sensitivity to external component variation
- Separate low pass, high pass and band pass outputs
- Operation to 40 kHz
- Q range to 500
- Wide power supply range ±5.0 V to ±18 V
- Accuracy ±1%
- Fourth order functions in one package
- BIFET™ input amplifiers, pin compatible with AF151J

Connection Diagram



Ceramic Dual-In-Line Package HY24A
AF161-1CJ
AF161-2CJ

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation	900 mW/Package
Differential Input Voltage	±36V
Output Short-Circuit Duration (Note 1)	Infinite
Operating Temperature	−25°C to +85°C
Storage Temperature	−25°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Complete Active Filter)

Specifications apply for V_S = ±15V and over −25°C to +85°C unless otherwise specified. (Specifications apply for each section).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_c \times Q \leq 200{,}000$			100k	Hz
Q Range	$f_c \times Q \leq 200{,}000$			500	Hz/Hz
f_o Accuracy					
AF161-1C	$f_c \times Q \leq 40{,}000$, T_A = 25°C			±2.5	%
AF161-2C	$f_c \times Q \leq 40{,}000$, T_A = 25°C			±1.0	%
f_o Temperature Coefficient			±50	±150	ppm/°C
Q Accuracy	$f_c \times Q \leq 10{,}000$, T_A = 25°C			±7.5	%
Q Temperature Coefficient			±300	±750	ppm/°C
Power Supply Current	V_S = ±15V		14.4	22	mA

Electrical Characteristics (Internal Op Amp) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$ @ 25°C		5	10	mV
Input Offset Current			25	100	pA
Input Bias Current			50	200	pA
Large Signal Voltage Gain	$R_L \geq 2k$, V_{OUT} = ±10V	25	100		V/mV
Output Voltage Swing	$R_L = 10\,k\Omega$	±12	±13.5		V
Input Voltage Range		±11	+15/−12		V
Common-Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$	70	100		dB
Slew Rate (Unity Gain)			13		V/μs
Small Signal Bandwidth			4		MHz

Note 1: Any of the amplifiers can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: Specifications apply for V_S = ±15V, T_A = 25°C.

Applications Information

The AF161 consists of 2 identical filter sections and 2 uncommitted op amps. The op amps may be used for buffering inputs and outputs, summing amplifiers (for notch filter generation), adjusting gain through the filter sections, additional passive networks to create higher order filters, or simply used elsewhere in the user's system.

The design equations given apply to both sections; however, for clarity, only the pin designations for section 1 will be shown in the examples and discussion.

See the AF100 data sheet for additional information on this type of filter.

The design equations assume that the user has knowledge of the frequency and Q values for the particular design to be synthesized. If this is not the case, various references and texts are available to help the user in determining these parameters. A bibliography of recommended texts can also be found in the AF100 data sheet.

CIRCUIT DESCRIPTION AND OPERATION

A schematic of one section of the AF161 is shown in *Figure 1*. Amplifier A1 is a summing amplifier with inputs from integrator A2 to the non-inverting input and integrator A3 to the inverting input. Amplifier A4 is an uncommitted amplifier.

By adding external resistors the circuit can be used to generate the second order system.

$$T(s) = \frac{a_3 s^2 + a_2 s + a_1}{s^2 + b_2 s + b_1}$$

The denominator coefficients determine the complex pole pair location and the quality of the poles where

$\omega_o = \sqrt{b_1}$ = the radian center frequency

$Q = \frac{\omega_o}{b_2}$ = the quality of the complex pole pair

If the output is taken from the output of A1, numerator coefficients a_1 and a_2 equal zero, and the transfer function becomes:

$$T(s) = \frac{a_3 s^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(high pass)}$$

If the output is taken from the output of A2, numerator coefficients a_1 and a_3 equal zero and the transfer functions becomes:

$$T(s) = \frac{a_2 s}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(band pass)}$$

If the output is taken from the output of A3, numerator coefficients a_3 and a_2 equal zero and the transfer function becomes:

$$T(s) = \frac{a_1}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(low pass)}$$

Using proper input and output connections the circuit can also be used to generate the transfer functions for a notch and all pass filter.

In the transfer function for a notch function a_2 becomes zero, a_1 equals ω_z^2 and a_3 equals 1. The transfer function becomes:

$$T(s) \quad \frac{s^2 + \omega_z^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(notch)}$$

In the all pass transfer function $a_1 = \omega_o^2$, $a_2 = -\omega_o/Q$ and $a_3 = 1$. The transfer function becomes:

$$T(s) \quad \frac{s^2 - \frac{\omega_o}{Q} s + \omega_o^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad \text{(all pass)}$$

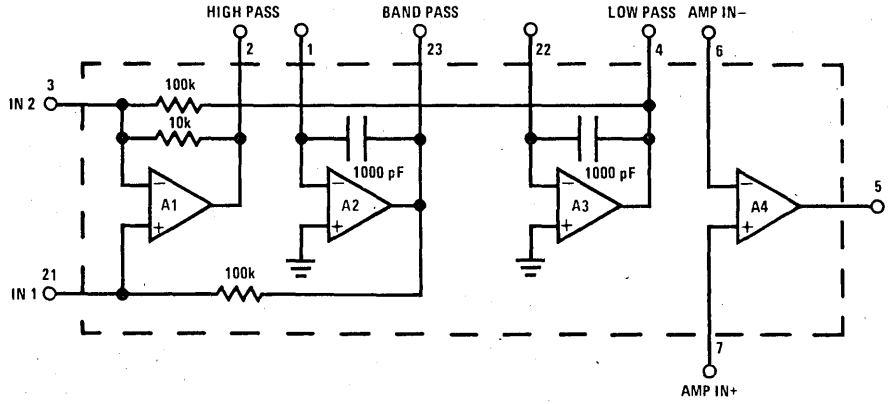


FIGURE 1. AF161 Schematic (Section 1)

Applications Information (Continued)

FREQUENCY CALCULATIONS

For operation above 200 Hz, the frequency of each section of the AF161 is set by 2 equal valued resistors. These resistors couple the output of the first op amp (pin 2) to the input of the second op amp (pin 1) and the output of the second op amp (pin 23) to the input of the third op amp (pin 22).

The value for R_f is given by:

$$R_f = \frac{50.33 \times 10^6}{f_o} \ \Omega \qquad (1)$$

For operation below 200 Hz, "T" tuning should be used as shown in *Figure 3*.

For this configuration,

$$R_S = \frac{R_T^2}{R_f - 2R_T} \qquad (2)$$

where R_T or R_S can be chosen arbitrarily, once R_f is found from equation 1.

Q CALCULATIONS

To set the Q of each section of the AF161, one resistor is required. The value of the Q setting resistor depends on the input connection (inverting or non-inverting) and the input resistance. Because the input resistance does affect the Q, it is often desirable to use one of the uncommitted op amps to provide a buffer between the signal source impedance and the input resistor used to set the Q.

To determine which connection is required for a particular Q, arbitrarily select a value of R_{IN} *(Figure 4)* and calculate Q_{MIN} according to equation 3.

$$Q_{MIN} = \frac{1 + \frac{10^5}{R_{IN}}}{3.48} \qquad (3)$$

If the Q required for the circuit is greater than Q_{MIN}, use equation 4 to calculate the value of R_Q and the connection shown in *Figure 4*.

$$R_Q = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}} \qquad (4)$$

If the Q required for the circuit is less than Q_{MIN}, use equation 5 to calculate the value of R_Q and the connection shown in *Figure 5*.

$$R_Q = \frac{10^4}{\frac{0.3162}{Q}\left(1 + \frac{10^5}{R_{IN}}\right) - 1.1} \qquad (5)$$

Both connections shown in *Figures 4 and 5* are "non-inverting" relative to the phase relationship between the input signal and the low pass output.

For any Q, equation 6 may be used with the "inverting" connection shown in *Figure 6*.

$$R_Q = \frac{10^5}{3.16\,Q\left(1.1 + \frac{10^4}{R_{IN}}\right) - 1} \qquad (6)$$

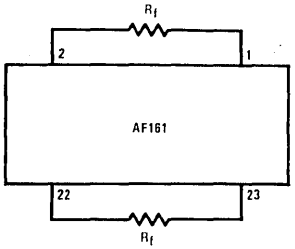


FIGURE 2. Frequency Tuning

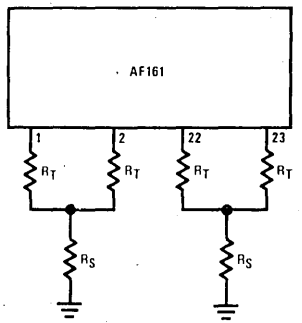


FIGURE 3. "T" Tuning for Low Frequency

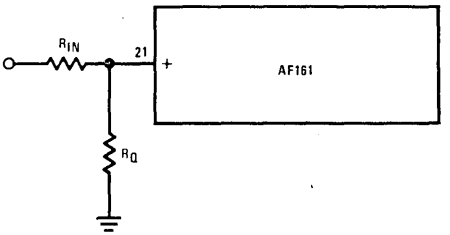


FIGURE 4. Connection for $Q > Q_{MIN}$

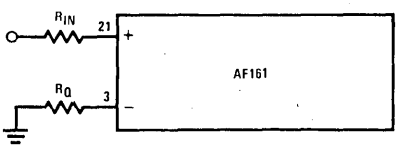


FIGURE 5. Connection for $Q < Q_{MIN}$

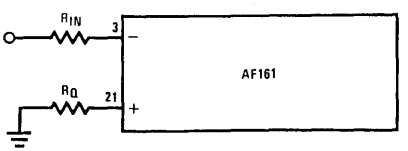


FIGURE 6. Connection for Any Q, Inverting

Applications Information (Continued)

NOTCH TUNING

When the low pass output and the high pass output are summed together, the result is a notch *(Figure 7)*.

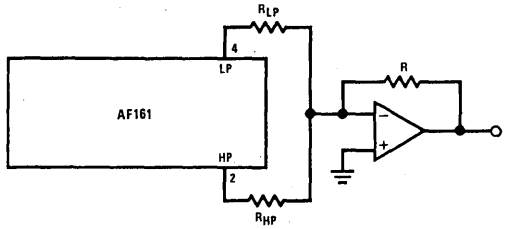


FIGURE 7. Notch Filter

The relationship between R_{LP}, R_{HP}, f_o and f_z, the location of the notch, is given by equation 7.

$$R_{HP} = \left(\frac{f_z}{f_o}\right)^2 \frac{R_{LP}}{10} \qquad (7)$$

Again, it is advantageous to use one of the uncommitted op amps to perform this summing function to prevent loading of this stage or the resistors R_{LP} and R_{HP} from effecting the Q of subsequent stages. Resistor R can be used to set the gain of the filter section.

GAIN CALCULATIONS

The following list of equations will be helpful in calculating the relationship between the external components and various important parameters. The following definitions are use:

A_L – Gain from input to low pass output at DC
A_H – Gain from input to high pass output at high frequency
A_B – Gain from input to band pass output at center frequency

For *Figure 4*:

$$A_L = \frac{11}{\Delta}$$

$$A_H = \frac{1.1}{\Delta}$$

$$A_B = \frac{-\left(1 + \frac{10^5}{R_Q} + \frac{10^5}{R_{IN}}\right)}{\Delta}$$

$$\Delta = 1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}$$

For *Figure 5:*

$$A_L = \frac{11 + \frac{10^5}{R_Q}}{\Delta}$$

$$A_H = \frac{1.1 + \frac{10^4}{R_Q}}{\Delta}$$

$$A_B = \frac{-\left(1 + \frac{10^5}{R_{IN}}\right)}{\Delta}$$

$$\Delta = 1 + \frac{R_{IN}}{10^5}$$

For *Figure 6:*

$$A_L = -\frac{10^5}{R_{IN}}$$

$$A_H = -\frac{10^4}{R_{IN}}$$

$$A_B = \frac{\frac{10^5}{R_{IN}}\left(1 + \frac{10^5}{R_Q}\right)}{11 + \frac{10^5}{R_{IN}}}$$

For *Figure 7*:

At low frequency, when $f_o < f_z$, the gain to the output of the summing op amp is:

$$A_L = \frac{11\left(\frac{R}{R_{LP}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)}$$

At high frequency, when $f_o > f_z$, the gain to the output of the summing op amp is:

$$A_H = \frac{1.1\left(\frac{R}{R_{HP}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)}$$

At the notch, ideally the gain is zero (0).

TUNING TIPS

In applications where 2% to 3% accuracy is not sufficient to provide the required filter response, the AF161 stages can be tuned by adding trim pots or trim resistors in series or parallel with one of the frequency determining resistors and the Q determining resistor.

When tuning a filter section, no matter what output configuration is to be used in the circuit, measurements are made between the input and the band pass output.

Before any tuning is attempted, the low pass output should be checked to see that the output is not clipping. At the center frequency of the section, the low pass output is 10 dB higher than the band pass output and 20 dB higher than the high pass. This should be kept in mind because if clipping occurs, the results obtained when tuning will be incorrect.

Applications Information (Continued)

Frequency Tuning

By adjusting resistor R_f, center frequency of a section can be adjusted. Adjusting center frequency by phase is the most accurate but tuning for maximum gain is also correct.

Q Tuning

The Q is tuned by adjusting the R_Q resistor. To tune the Q correctly, the signal source must have an output impedance very much lower than the input resistance of the filter since the input resistance affects the Q. The input must be driven through the same resistance the circuit will "see" to obtain precise adjustment.

The lower 3 dB (45°) frequency, f_L, and the upper 3 dB (45°) frequency, f_H, can be calculated by the following equations:

$$f_H = \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right) \times (f_o)$$

where f_o = center frequency

$$f_L = \left(\sqrt{\left(\frac{1}{2Q}\right)^2 + 1} - \frac{1}{2Q}\right) \times (f_o)$$

When adjusting the Q, set the signal source to either f_H or f_L and adjust for 45° phase change or a 3 dB gain change.

Notch Tuning

If a circuit has a jw axis zero pair, the notch can be tuned by adjusting the ratio of the summing resistors (low pass/high pass summing).

In either case, the signal is connected to the input and the proper resistor is adjusted for a null at the output.

TUNING PROCEDURE

Center Frequency Tuning

Set oscillator to center frequency desired for the filter section, adjust amplitude and check that clipping does not occur at the low pass output.

Adjust the R_f resistor until the phase shift between input and band pass output is 180° or 0°, depending upon the connection.

Q Tuning

Set oscillator to upper or lower 45° frequency (see tuning tips) and tune the Q resistor until the phase shift is 135° (upper 45° frequency) or 225° (lower 45° frequency).

Zero Tuning (Notch Tuning)

Set the oscillator output to the zero frequency and tune one of the summing resistors for a null at the output of the summing amplifier.

Gain Adjust

Set the oscillator to any desired frequency and the gain can be adjusted by measuring the output of the summing amplifier and adjusting the feedback resistance.

DESIGN EXAMPLE

Assume 2 band pass filters are required to separate FSK data.

f1 = 800 Hz, Q = 40
f2 = 1000 Hz, Q = 50

The gain through each filter is to be 10 V/V (20 dB).

Since the design is similar for both sections, only the first section design will be shown for the example.

(a) From equation 1

$$R_f = \frac{50.33 \times 10^6}{f_o} = \frac{50.33 \times 10^6}{800}$$

$$\boxed{R_f = 62.9k}$$

(b) Checking Q_{MIN} from equation 3, arbitrarily let R_{IN} = 300k.

$$Q_{MIN} = \frac{1 + \frac{10^5}{R_{IN}}}{3.48} = \frac{1 + \frac{10^5}{3 \times 10^5}}{3.48} = 0.383$$

Since the Q required for the design (Q = 40), is greater than Q_{MIN}, the circuit of *Figure 4* or *Figure 6* may be used. Arbitrarily we shall select the circuit of *Figure 4*.

(c) From equation 4, R_Q is found to be

$$R_Q = \frac{10^5}{3.48Q - 1 - \frac{10^5}{R_{IN}}} = \frac{10^5}{(3.48)(40) - 1 - \frac{10^5}{3 \times 10^5}}$$

or $\boxed{R_Q = 725\Omega}$

(d) Calculate the center frequency gain for *Figure 4*.

$$A_B = \frac{-\left(1 + \frac{10^5}{R_Q} + \frac{10^5}{R_{IN}}\right)}{\left(1 + \frac{R_{IN}}{10^5} + \frac{R_{IN}}{R_Q}\right)} = \frac{-(1 + 137.9 + 0.333)}{(1 + 3.0 + 414)}$$

$$A_B = 0.333 \text{ V/V}$$

Since the gain at f_o is 0.333 V/V, a gain of 10 V/V can be obtained by using the uncommitted operational amplifier with a gain of 30.03 as shown in *Figure 8*.

Applications Information (Continued)

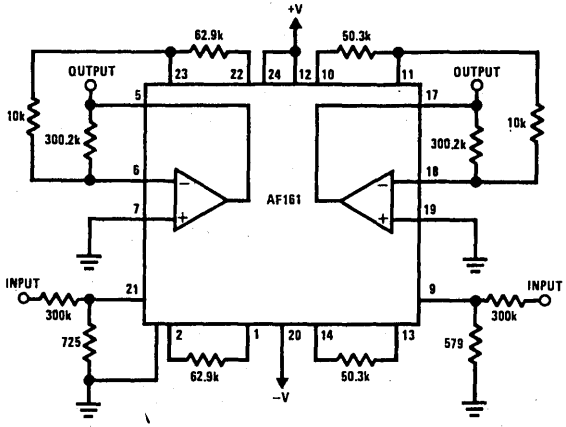


FIGURE 8. Dual Band Pass Filter

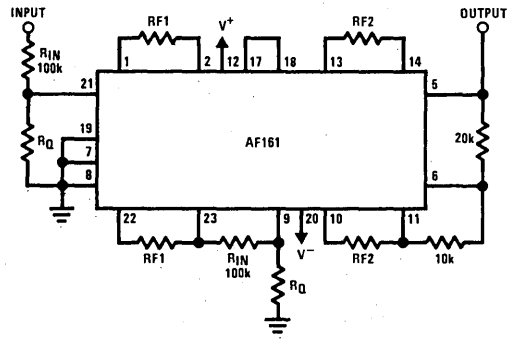


FIGURE 9. Telephone Multifrequency (MF) Band Pass Filter

FREQ	BW	f_c	f1	Q1 & Q2	f2	RF1	RF2	RQ
700	75	698.4	665.6	17	732.8	75.62k	68.68k	1.749k
900	75	898.7	865.8	21.8	932.9	58.13k	53.95k	1.354k
1100	75	1098.8	1065.7	26.7	1132.9	47.23k	44.43k	1.100k
1300	75	1298.9	1265.8	31.6	1332.9	39.76k	37.76k	926.2Ω
1500	75	1499.0	1465.8	36.4	1532.9	34.34k	32.83k	802.1Ω
1700	75	1699.1	1665.9	41.3	1733.0	30.21k	29.04k	705.6Ω

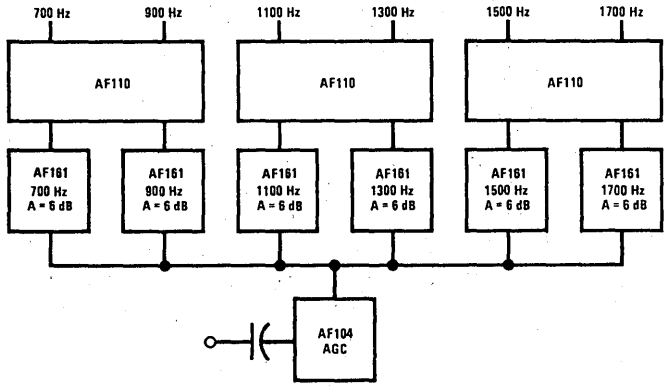
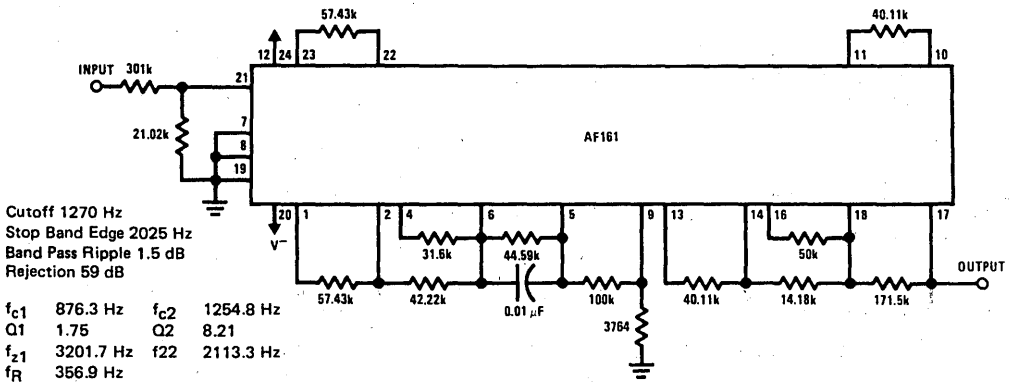


FIGURE 10. MF Tone Receiver

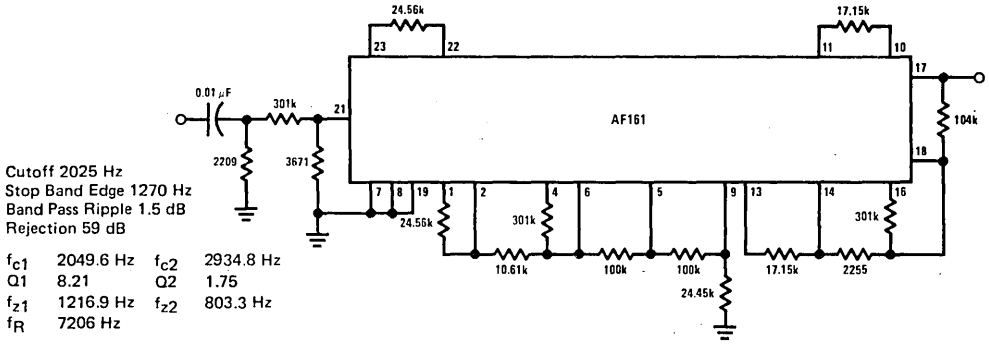


Cutoff 1270 Hz
Stop Band Edge 2025 Hz
Band Pass Ripple 1.5 dB
Rejection 59 dB

f_{c1}	876.3 Hz	f_{c2}	1254.8 Hz
Q1	1.75	Q2	8.21
f_{z1}	3201.7 Hz	f22	2113.3 Hz
f_R	356.9 Hz		

FIGURE 11. Low Pass Low Speed Asynchronous FSK Modem Filter

Applications Information (Continued)



Cutoff 2025 Hz
Stop Band Edge 1270 Hz
Band Pass Ripple 1.5 dB
Rejection 59 dB

f_{c1}	2049.6 Hz	f_{c2}	2934.8 Hz
Q1	8.21	Q2	1.75
f_{z1}	1216.9 Hz	f_{z2}	803.3 Hz
f_R	7206 Hz		

FIGURE 12. High Pass Low Speed Asynchronous FSK Modem Filter

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.33 can represent 1.33Ω, 133Ω, 1.33 kΩ, 13.3 kΩ, 133 kΩ 1.33 MΩ.

Standard 5% and 2% Resistance Values

OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	MEGOHMS	
10	27	68	180	470	1,200	3,300	8,200	22,000	56,000	150,000	0.24	0.62
11	30	75	200	510	1,300	3,600	9,100	24,000	62,000	160,000	0.27	0.68
12	33	82	220	560	1,500	3,900	10,000	27,000	68,000	180,000	0.30	0.75
13	36	91	240	620	1,600	4,300	11,000	30,000	75,000	200,000	0.33	0.82
15	39	100	270	680	1,800	4,700	12,000	33,000	82,000	220,000	0.36	0.91
16	43	110	300	750	2,000	5,100	13,000	36,000	91,000		0.39	1.0
18	47	120	330	820	2,200	5,600	15,000	39,000	100,000		0.43	1.1
20	51	130	360	910	2,400	6,200	16,000	43,000	110,000		0.47	1.2
22	56	150	390	1,000	2,700	6,800	18,000	47,000	120,000		0.51	1.3
24	62	160	430	1,100	3,000	7,500	20,000	51,000	130,000		0.56	1.5

Decade Table Determining 1/2% and 1% Standard Resistance Values

1.00	1.21	1.47	1.78	2.15	2.61	3.16	3.83	4.64	5.62	6.81	8.25
1.02	1.24	1.50	1.82	2.21	2.67	3.24	3.92	4.75	5.76	6.98	8.45
1.05	1.27	1.54	1.87	2.26	2.74	3.32	4.02	4.87	5.90	7.15	8.66
1.07	1.30	1.58	1.91	2.32	2.80	3.40	4.12	4.99	6.04	7.32	8.87
1.10	1.33	1.62	1.96	2.37	2.87	3.48	4.22	5.11	6.19	7.50	9.09
1.13	1.37	1.65	2.00	2.43	2.94	3.57	4.32	5.23	6.34	7.68	9.31
1.15	1.40	1.69	2.05	2.49	3.01	3.65	4.42	5.36	6.49	7.87	9.53
1.18	1.43	1.74	2.10	2.55	3.09	3.74	4.53	5.49	6.65	8.06	9.76

Section 15

Precision Networks

15

National Semiconductor

Precision Networks

RA201 Precision Instrumentation Amplifier Resistor Network

General Description

The RA201 is a family of precision instrumentation amplifier networks. This device, when combined with 3 operational amplifiers, provides a precision instrumentation amplifier with common-mode rejection up to 100 dB. All gain setting resistors are provided within the device. This feature assures excellent thermal tracking and thermal matching of all resistors. This network is manufactured using a high stability thin-film technology. Thin-film resistors provide tracking temperature coefficients of better than 5 ppm/°C. The thin-film resistors are laser trimmed to guarantee resistor matching to 0.05% for the RA201-2, and 0.1% for the RA201-1.

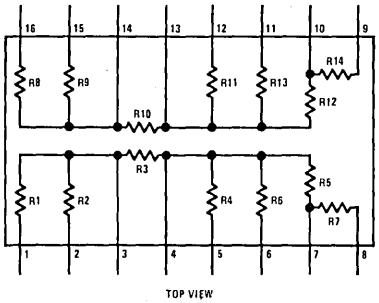
Other applications include process control interfacing and precision decade dividers.

Features

- Gain programmable
- Matching accuracies to 0.05%
- Matching temperature coefficient to 5 ppm/°C
- Absolute temperature coefficient to 80 ppm/°C
- Close thermal proximity of all resistors
- Standard dual-in-line package
- Low-cost

Connection Diagram

Dual-In-Line Package

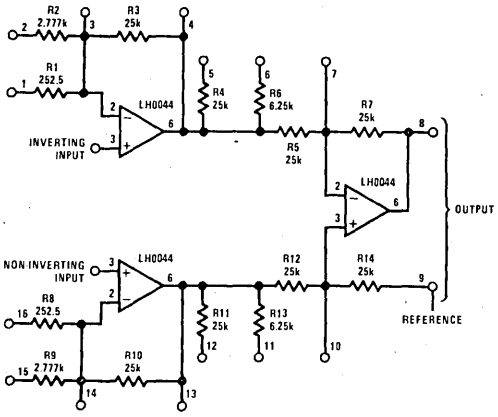


TOP VIEW

R1 = 252.525 . . Ω
R2 = 2.777 . . . kΩ
R3 = 25k
R4 = 25k
R5 = 25k
R6 = 6.25k
R7 = 25k
R8 = 252.525 . . . Ω
R9 = 2.777 . . . kΩ
R10 = 25k
R11 = 25k
R12 = 25k
R13 = 6.25k
R14 = 25k

R3:R2 = 9:1
R3:R1 = 99:1
R3||R2 = 2.50k
R3||R1 = 250.0Ω
R5||R6 = 5.0k

Typical Application



Overall Gain	Input Stage Gain	Output Stage Gain	Jumper Pins on RA201
X1	X1	X1	
X2	X1	X2	5 to 7, 12 to 10
X5	X1	X5	6 to 7, 11 to 10
X10	X10	X1	2 to 15
X20	X10	X2	2 to 15, 5 to 7, 12 to 10
X50	X10	X5	2 to 15, 6 to 7, 11 to 10
X100	X100	X1	1 to 16
X200	X100	X2	1 to 16, 5 to 7, 12 to 10
X500	X100	X5	1 to 16, 6 to 7, 11 to 10
X995	X199	X5	1 to 14, 6 to 7, 11 to 10

Precision Instrumentation Amplifier

Absolute Maximum Ratings

Rated Voltage Between Sections	200V
Rated Voltage Across Resistors	(Note 1)
Package Power Dissipation at 25°C (See Curve)	2.0W
Individual Resistor Power at 25°C	0.25W
Operating Temperature Range	
RA201-1N, RA201-2N	−25°C to +85°C
RA201-1D, RA201-2D	−55°C to +125°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $T_A = 25°C$ (Note 2)

Parameter	Conditions; Resistors Tested	Typ.	RA201-2 Max.	RA201-1 Max.	Units
Input Stage × 10	R2:R3	1:9	±0.01	±0.2	%
	R9:R10	1:9	±0.01	±0.2	%
Input Stage × 100	R1:R3	1:99	±1.0	±1.0	%
	R8:R10	1:99	±1.0	±1.0	%
Output Stage × 1	R7:R5	1:1	±0.05	±0.1	%
	R14:R12	1:1	±0.05	±0.1	%
Output Stage × 2	(R4||R5):R7	1:2	±0.05	±0.1	%
	(R12||R11):R14	1:2	±0.05	±0.1	%
Output Stage × 5	(R6||R5):R7	1:5	±0.05	±0.1	%
	(R12||R13):R14	1:5	±0.05	±0.1	%
Output Stage CMRR	(R7:R5):(R14:R12), (Note 3)	1:1	±0.05	±0.1	%
Absolute Tolerance	R3, R10	25kΩ	±5.0	±5.0	%
Absolute Tempco		80			ppm/°C

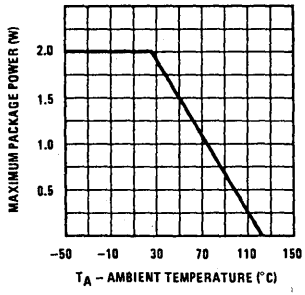
Note 1: Rated voltage is limited by the individual resistor power rating of 0.25W. For example, a 25k resistor could withstand a maximum of $V = \sqrt{(0.25)(25{,}000)} = 79V$. This rating may need to be reduced to be consistent with maximum package power if several resistors are dissipating power simultaneously.

Note 2: Resistor ratios shown apply at $T_A = 25°C$; for $T_{MIN} \leq T_A \ T_{MAX}$ the ratio tolerances are double the specifications shown.

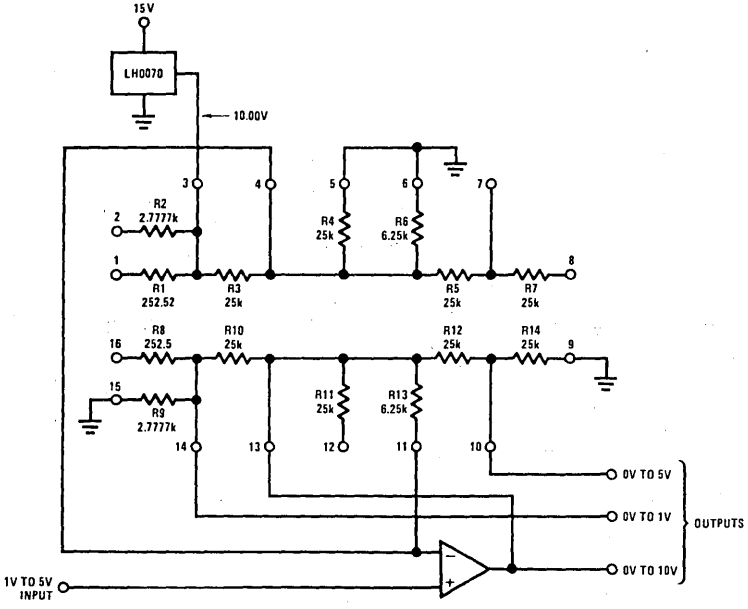
Note 3: This test guarantees the CMRR contributed by resistance mismatch. In low gain applications, all 3 amplifiers contribute strongly to the overall CMRR. In high gain applications, the degradation due to resistor mismatch and output stage CMRR are divided by the gain of the input stage.

Typical Performance Characteristics

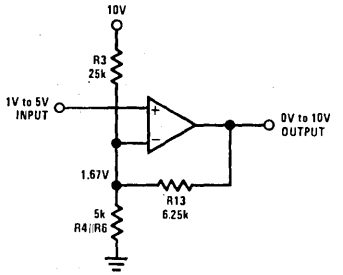
Power Derating



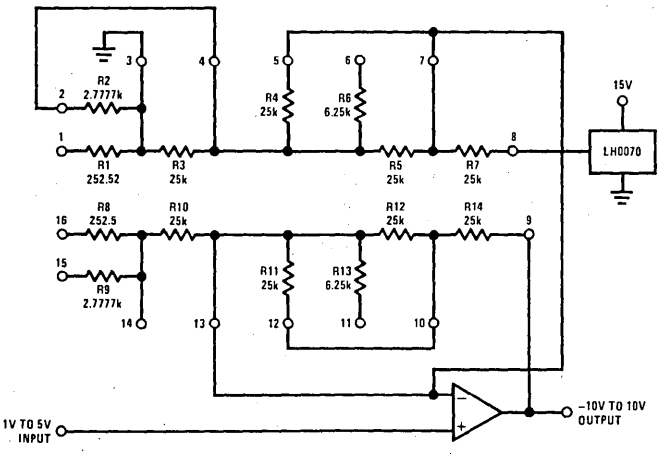
Applications Information



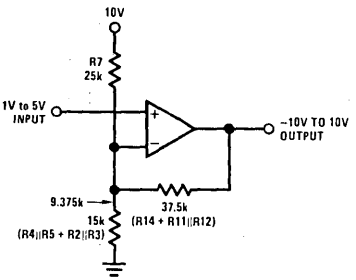
RA201 Process Control Interface No. 1



Equivalent Circuit

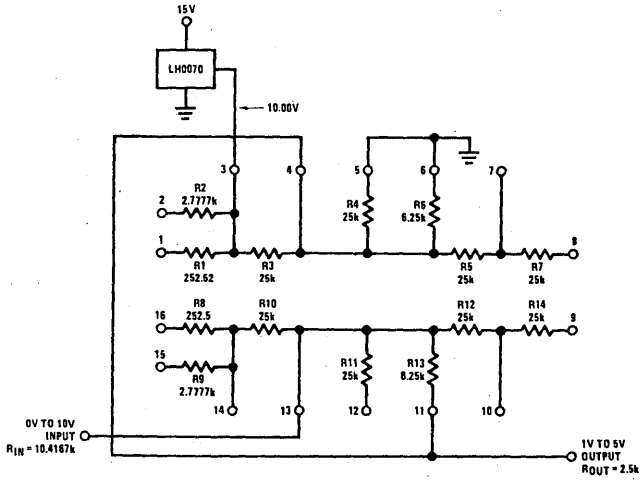


RA201 Process Control Interface No. 2

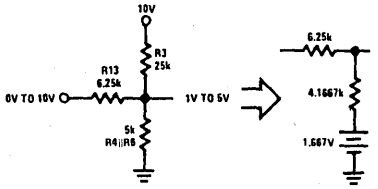


Equivalent Circuit

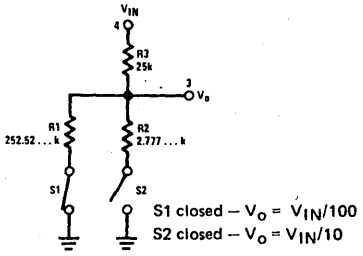
Applications Information (Continued)



RA201 Process Control Interface No. 3



Equivalent Circuit



Precision Decade Divider

Ordering Information

Part Number	Accuracy	Package	Temperature Range
RA201-1D	0.1%	D16C	−55°C to +125°C
RA201-2D	0.05%	D16C	−55°C to +125°C
RA201-1N	0.1%	N16A	−25°C to +85°C
RA201-2N	0.05%	N16A	−25°C to +85°C

Section 16

16

883/RETS

Reliability
Electrical
Test
Specifications

National Semiconductor

883B/RETS™ Program

The National Semiconductor 883B/RETS™ Program was conceived with the intent of offering our customers a standardized, off-the-shelf, integrated circuit fully compliant to the current revision of MIL-STD-883.

The following specification outlines the program qualification, quality conformance and processing requirements. Records and data substantiating the testing as specified herein are controlled and administered through National Semiconductor Quality Assurance and Reliability group (located in Santa Clara, California) and are available for review.

As a complement to this program, the National Quality system is designed to encompass the requirements of MIL-Q-9858 and associated documents.

John Montesi, Director
Quality Assurance and Reliability
National Semiconductor Corporation

883B/RETS™ Products from National Semiconductor

1.0 Scope

1.1 Purpose

This specification establishes the requirements for screening and processing of integrated circuits in accordance with MIL-STD-883, Class B.

1.2 Intent

This specification is intended to provide the user with the ability to procure standardized, off-the-shelf integrated circuits manufactured by National Semiconductor Corporation that are fully compliant to MIL-STD-883.

2.0 Applicable Documents

The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

2.1 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	General Specification for Microcircuits
MIL-C-45662	Calibration System Requirements
MIL-Q-9858	Quality System Requirements

2.2 Standards

Military

MIL-STD-105	Sampling Procedures and Tables
MIL-STD-883	Test Methods and Procedures for Microelectronics

2.3 Detail Specifications

The detail specification for a particular 883B/RETS™ microcircuit is the National Semiconductor RETS (Reliability Electrical Test Specification, see *Figure 1*). The RETS is a detailed listing of the parameters, forcing functions and limits on the test tapes used to test 883B/RETS microcircuits.

3.0 General Requirements

The individual requirements shall be as specified herein and in accordance with the applicable detail specification. The static and dynamic electrical performance requirements for the integrated circuits and electrical test methods shall be as specified in the detail specification.

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3.1. Process Conditioning, Testing, Reliability and Quality Assurance Screening

Process conditioning, screening and testing shall be as specified in Section 4.0

MIL-STD-883 Q.A. Process Level	Applicable Process Flow Chart	Suffix Level Indicator
B	*Figure 2*	/883B

3.1.1 Qualification

The 883B/RETS microcircuits furnished under this specification shall be products which have been produced and tested and have passed the qualification tests specified herein. Successful qualification for a given level results in qualification approval for that level and all lower products assurance levels of that device (reference Appendix E MIL-M-38510D).

3.1.2 Alternate Qualifications

In lieu of meeting the requirements of 3.1.1, the manufacturer may establish qualification by performing an intial, one time qualification test. Qualification testing shall be performed on each generic family supplied. Upon successful completion of the qualification program, the manufacturer shall remain qualified for a period not to exceed 12 months.

3.2 Quality Conformance Inspection

The 883B/RETS microcircuits furnished under this specification shall be products which have been produced and tested in conformance with all the provisions of this specification for the applicable level. Devices which have been accepted as conforming to a given product assurance level may be furnished as conforming to any other level for which they meet or exceed the quality conformance requirements.

3.3 Marking

3.3.1 Marking on Each Device

The following marking shall be placed on each microcircuit:

a) Index point (see 3.3.4)
b) Part number (see 3.3.5)
c) Product assurance level (see 3.3.6)
d) Inspection for identification code (see 3.3.8)
e) Manufacturer's identification (see 3.3.9)

3.3.2 Marking on Initial Container

All of the marking specified in 3.3.1, except the index point, shall appear on the initial protection or wrapping for delivery.

RETS111X (2)
Revision B

Burn-In-Circuits (1)
H: 8358HR; F: 8359HR; D: 8665HR

Test Conditions (Unless Otherwise Specified)
V_{CC}=15V, V_{CM}=0V, V_{OUT}=1.4V with respect to V_{CC-}, V_{56}=0V, R_S=0V

Test System: Teradyne J-273 (1)

NOTES	Parameter	Symbol	Conditions		Δ Test Number	Test Number	RL-111XRI Subgroup 1 +25°C Min.	RL-111XRI Subgroup 1 +25°C Max.	RL-111XHG Subgroup 2 +125°C Min.	RL-111XHG Subgroup 2 +125°C Max.	RL-111XLG Subgroup 3 −55°C Min.	RL-111XLG Subgroup 3 −55°C Max.	Optional Drift Δ Limits (25°C) (note 3)	Units of Measure
	Input Offset Voltage	V_{IO}	V_{CM}=+13.5V, −14.5V and 0V	(note 4)	105, 113	5, 13, 20		3.0		4.0		4.0	±0.5	mV
			R_S=50KΩ, V_{CM}=+13.5V, −14.5V and 0V		106, 114, 121	6, 14, 21		3.0		4.0		4.0	±0.5	mV
			V_{85}=V_{86}=0V, V_{CM}=+13.5V, −14.5V, 0V			8, 16, 23		3.0						mV
			V_{85}=V_{86}=0V, V_{CM}=+13.5V, −14.5V, 0V, R_S=50KΩ			9, 17, 24		3.0						mV
			V+=4.5V, V−=0V, V_{OUT}=0.4V, V_{CM}=3V, 0.5V			27, 29		5.0		6.0		6.0		mV
			V+=4.5V, V−=0V, V_{OUT}=0.4V, V_{CM}=3V, 0.5V			28, 30		3.0		4.0		4.0		mV
	Input Offset Current	I_{IO}	R_S=50KΩ, V_{CM}=+13.5V, −14.5V and 0V			7, 15, 22		10		20		20		nA
			V_{85}=V_{86}=0V, R_S=50KΩ, V_{CM}=13.5V, −14.5V, 0V			10, 18, 25		30						nA
	Input Bias Current	I_{IB}	R_S=50KΩ, V_{CM}=+13.5V, −14.5V, 0V	(note 5)	126	11, 19, 26		100		100		150	±10	nA
	Large Signal Gain	A_{VS}	R_L=1KΩ, V_{OUT}=−12V to +35.0V			31	40		30		30			V/mV
	Emitter Follower Gain	A_{VEF}	R_L=600Ω, V_I=−15V to +12V			32	10		8.0		8.0			V/mV
	Common Mode Rejection Ratio	CM_{RR}	+13.5V ≥ V_{CM} ≥ −14.5V			12	80		80		80			dB
6	Negative Supply Current	I_{CC-}			101	1.0		−5.0		−5.0		−15	±0.5	mA
6	Positive Supply Current	I_{CC+}				2.0		6.0		6.0		15		mA
	Input Leakage Current	I_{IL1}	V_{CC}=±18V, V_{28}=1V, V_{38}=30V, V_{OUT}=50V with respect to V_{CC-}			3.0		10		30				nA
		I_{IL2}	V_{CC}=±V_{28}=30V, V_{38}=1V, V_{OUT}=50V with respect to V_{CC-}			4		10		30				nA
	Output Leakage Current	I_{LOUT}	V_{CC}=±18V, 15+15=5mA, V_{OUT}=35V with respect to V_{CC-}			33		10		500				nA
	Ground Leakage Current	I_{LG}	As in I_{LOUT}			34		25		500				nA
	Saturation Voltage	V_{SAT}	I_{OUT}=50mA, V_{IN}=−5mV			35		1.5						V
			I_{OUT}=8ma, V_{IN}=−6mV			36		0.4		0.4		0.4		V
2	Strobe ON Current	I_{STR}						4.0						mA

Note 4: Δ computed at V_{CM}=+13.5V and −14.5V only
Note 5: Δ computed at V_{CM}=0V only
Note 6: −55°C tests are for continuity check only

SAMPLE ONLY

The RETS details National's standard electrical testing with the following key information clearly identified.

A. RETS number and revision level.
B. Standard Burn-in circuits.
C. Basic Test system, test tapes and revisions.
D. Test numbers (including Δ tests)
E. Recommended Δ's (which are standard on 883S/RETS™ microcircuits)
F. Special test equipment (where applicable).
G. Clear definition of test conditions.
H. Clear footnotes, where necessary.
I. Part number and function.

Note 1: Parameter tested go no go only, cannot be data logged.
Note 2: Guaranteed parameter, no testing is available.
Note 3: Drift limits apply to Class S devices only.

Device: LM111 (1) **Function:** Voltage Comparator

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Class B

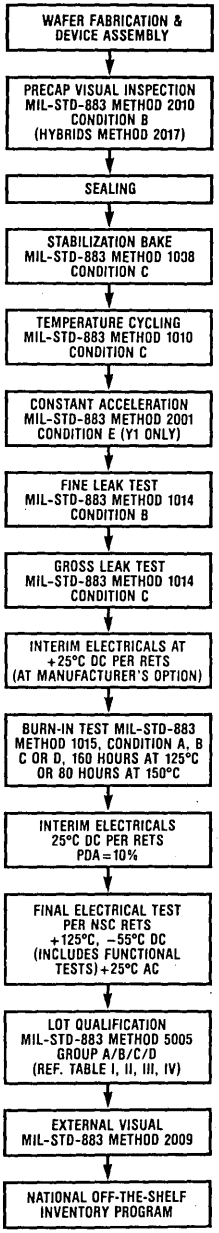

Figure 2. 883B/RETS™ Product Screening Flow (per MIL-STD-883)

3.3.3 Marking Permanence

Marking shall be permanent in nature and remain legible after testing. Damage to marking caused by mechanical fixturing in Group B, C, and D tests shall not be cause for lot rejection.

3.3.4 Index Point

The index point indicating the starting point for numbering of leads and/or mechanical orientation of the integrated circuit may be a tab, color dot, or other suitable indicator.

3.3.5 Part Number

The part number shall be the National Semiconductor generic part number.

3.3.6 Product Assurance Level

Integrated circuits shall be marked with a code indicating the product assurance level to which they have been tested and found to conform. The code shall consist of /883 followed by the letter B.

3.3.7 Formation of Lots

Microcircuits shall be assembled into inspection lots in accordance with MIL-M-38510.

3.3.8 Inspection Lot Identification Code

Integrated circuits shall be marked by a 4-digit date code indicating the date the lot was sealed. The first 2 numbers in the code shall be the last 2 digits of the number of the year. The third and fourth numbers shall be 2 digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero.

3.3.9 Manufacturer's Identification

Integrated circuits shall be marked with the name, logo, or trademark of the manufacturer.

4.0 Conditions and Methods of Test:

Conditions and methods of test shall be in accordance with Method 5004 of MIL-STD-883 and as specified herein on a 100% basis. The general requirements of MIL-STD-883 apply as applicable. This section establishes the stress screening tests and quality conformance inspection tests for this program. The purpose of these tests is to assure the quality and reliability of the product to a particular process level commensurate with the product's intended application.

4.1 Internal Visual Inspection (Precap)

Internal visual inspection shall be performed per MIL-STD-883, Method 2010, Condition B. Hybrid internal visual shall be performed per Method 2017.

4.2 Stabilization Bake

Stabilization bake shall be performed per MIL-STD-883, Method 1008, Condition C. The devices shall be stored for 24 hours minimum at 150°C minimum. No end point measurements shall be performed.

4.3 Temperature Cycling

Temperature cycling shall be performed per MIL-STD-883, Method 1010, Condition C, 10 cycles, from −65°C to +150°C.

4.4 Constant Acceleration

Constant acceleration shall be performed per MIL-STD-883, Method 2001, Condition E, at 30,000 G's, in Y1 plane only.

4.5 Hermeticity

Hermeticity tests shall be performed per the following:

Fine Leak Testing

Fine leak testing shall be performed per MIL-STD-883, Method 1014, Condition B. The criterion for rejection will be in accordance with MIL-STD-883.

Gross Leak Testing

Gross leak testing shall be performed per MIL-STD-883, Method 1014, Condition C. The rejection criterion will be per MIL-STD-883.

4.6 Interim Electrical Parameters

Interim electrical parameters shall be the 25°C DC parameters, specified in the detail specification (RETS). (Interim electrical parameters are performed at the manufacturer's option.)

4.7 Burn-In

Burn-in shall be performed per MIL-STD-883, Method 1015; Conditions A, B, C or D on all Class B devices. (Burn-in condition varies with product type.) Burn-in shall be performed for 160 hours at 125°C (or for 80 hours at 150°C as allowed by Method 1015).

4.8 Final Electrical Parameters

Final electrical parameters shall be as specified in the applicable detail specification (RETS). DC testing shall be performed at 25°C, −55°C, 125°C. AC testing shall be performed at 25°C. The PDA (Percent Defective Allowable) shall be 10% maximum and shall only apply to DC measurements at 25°C.

4.9 External Visual Inspection

All 883B/RETS™ microcircuits shall receive external visual inspection per MIL-STD-883, Method 2009.

5.0 Quality Assurance Provisions

5.1 Quality Conformance Inspection

Quality conformance inspection shall be in accordance with Tables I, II, III and IV. Inspection lot sampling shall be in accordance with Method 5005 of MIL-STD-883. Inspection lots failing to meet quality conformance inspection for a given product assurance level shall be rejected. Sample selection shall be in accordance with MIL-M-38510.

5.1.1 Group A Inspection

Group A inspection shall consist of the electrical parameters in the RETS (Reliability Electrical Test Specification). If an inspection lot is made up of a collection of sublots, each sublot shall be subjected to Group A, as specificed (see Table I). Group A may be done in-line

5.1.2 Group B Inspection

Group B inspection consists of construction testing. This sample test sequence includes physical dimensions, resistance to solvents, internal visual and mechanical, bond strength and solderability (see Table II). Group B qualifies the inspection sublot from which the sample is selected and all generically similar devices manufactured within the same inspection lot. Group B may be done in-line.

5.1.3 Group C Inspection

Group C inspection consists of die stress testing. This sample test sequence includes operating life, temperature cycling, constant acceleration, hermeticity, visual examination and end point electricals (see Table III). Group C qualifies the lot from which the sample is selected and all generically similar die types for a period of 90 days.

5.1.4 Group D Inspection

Group D testing further stresses the package and the die. The Group D tests include physical dimensions, lead integrity, hermeticity, thermal shock, temperature cycling, moisture resistance, mechanical shock, vibration variable frequency, constant acceleration, salt atmosphere, visual examination, and end point electricals (see Table IV). Group D qualifies the lot from which the sample is selected and all devices built in the same package for a period of 6 months.

Table I. Group A Electrical Test

Subgroups	Class B LTPD
Subgroup 1 Static tests at 25°C	5
Subgroup 2 Static tests at maximum rated operating temperature	7
Subgroup 3 Static tests at minimum rated operating temperature	7
Subgroup 4 (note 1) Dynamic tests at 25°C	5
Subgroup 5 (note 1) Dynamic tests at maximum rated operating temperature	7
Subgroup 6 (note 1) Dynamic tests at minimum rated operating temperature	7
Subgroup 7 (note 1) Functional tests at 25°C	5
Subgroup 8 (note 1) Functional tests at maximum and minimum rated operating temperature	10
Subgroup 9 Switching tests at 25°C	7

Note 1: These subgroups will be performed concurrently with subgroups 1-3.

Table II. Group B Inspection

Test	Method	Conditions	Class B
Subgroup 1 Physical dimension	2016		2 devices (No failures)
Subgroup 2 a) Resistance to solvents	2015		4 devices (No failures)
Subgroup 3 Solderability	2003	Soldering temperature of 260 ± 10°C	15 leads (3 units min. No failures)
Subgroup 4 Internal visual and mechanical	2014	Failure criteria from design & construction requirements of applicable procurement document	1 device (No failures)
Subgroup 5 Bond strength	2011	Condition C or D	15 Bonds (10 units min. No failures)
Subgroup 6 Internal water-vapor content	1018	1000 ppm maximum water content at 100°C (only required on packages which contain a dessicant)	3 devices (No failures) or 5 devices (1 failure)
Subgroup 7 Seal (fine and gross)	1014	As applicable	LTPD = 5
Subgroup 8 Electrical parameters Electrostatic discharge sensitivity Electrical parameters	3015	Group A, subgroup 1 per RETS Condition A or B Group A, subgroup 1 per RETS	LTPD = 15(0) Only required for initial qualification or product redesign

Table III. Group C Inspection

Test	Method	Conditions	Class B LTPD
Subgroup 1 Operating Life Test End point electricals	1005	Test conditions to be specified 1000 hours@+125°C as specified in the applicable detail specification (Subgroups 1, 2, and 3 of Group A)	5
Subgroup 2 Temperature cycling Constant acceleration Seal (fine and gross) Visual examination End point electrical parameters	 1010 2001 1014 1010	 Test condition C Test Condition E, Y1 axis As applicable As specified in applicable device specification (Subgroups 1, 2, and 3 of Group A)	15
Subgroup 10 AC parameters at 125°C		Per applicable RETS	10
Subgroup 11 AC parameters at −55°C		Per applicable RETS	10

Table IV. Group D Inspection

Test	Method	Conditions	Class B LTPD
Subgroup 1			
Physical dimensions	2016		15
Subgroup 2			
Lead integrity	2004	Test conditions B2 (lead fatigue)	15
Seal (fine and gross)	1014	As applicable	
Lid torque	2024	As applicable	
Subgroup 3			
Thermal shock	1011	Test condition B — 15 cycles	15
Temperature cycling	1010	Test condition C — 100 cycles	
Moisture resistance	1004		
Seal (fine and gross)	1014	As applicable	
Visual examination	1004		
End point electrical parameters		As specified in the applicable device specification (Subgroups 1, 2, and 3 of Group A)	
Subgroup 4			
Mechanical shock	2002	Test condition B	15
Vibration variable frequency	2007	Test condition A	
Constant acceleration	2001	Test condition E, Y, Axis	
Seal (fine and gross)	1014	As applicable	
Visual examination	1010 or 1011		
End point electrical parameters		As specified in the applicable device specification (Subgroups 1, 2, and 3 of Group A)	
Subgroup 5			
Salt atmosphere	1009	Test condition A	15
Seal (fine and gross)	1014	As applicable	
Visual examination	1009	Paragraph 3.3.1 of Method 1009	
Subgroup 6			
Internal water vapor content	1018	5000 ppm maximum water content at 100°C	3 devices (No failures) or 5 devices (1 failure)
Subgroup 7			
Adhesion of lead finish	2025		15

6.0 Data

6.1 Certificate of Conformance

All 883B/RETS™ microcircuits shipped shall be accompanied by a Certificate of Conformance as shown on the following page.

6.2 Attributes Data

Attributes data for 100% screening will not normally be provided, but shall be retained on file. Copies are available at nominal cost.

6.3 Quality Conformance Data

Quality conformance data will not normally be provided, but shall be retained on file. Copies are available at nominal cost.

7.0 Packaging

Packing and packaging shall be in accordance with MIL-M-38510.

8.0 Custom Marking

Since 883B/RETS microcircuits are fully compliant with Methods 5004 and 5005 of MIL-STD-883 they are typically fully compliant to Source Control and Specification Control Drawings prepared in accordance with MIL-STD-883 and MIL-STD-100. 883B/RETS devices may be dual-marked with applicable SCD numbers at no extra cost.

9.0 883S/RETS™ Microcircuits

For those semiconductor users requiring space level reliability, National Semiconductor also offers a program for fully compliant Class S devices. This program is described in our Brochure "883S/RETS™ Products from National Semiconductor".

883B/RETS™ PROGRAM CERTIFICATE OF CONFORMANCE

TEST	MIL-STD-883 METHOD**	REQUIREMENT
INTERNAL VISUAL	2010 B	100%
STABILIZATION BAKE	1008 C 24 HRS.@+150°C	100%
TEMPERATURE CYCLING	1010 C 10 CYCLES −65°C/+150°C	100%
CONSTANT ACCELERATION	2001 E 30,000 G's, Y_1 AXIS	100%
FINE LEAK	1014 B 5×10^{-8}	100%
GROSS LEAK	1014 C	100%
BURN-IN	1015 160 HRS.@+125°C	100%
	OR 80 HRS.@+150°C	
FINAL ELECTRICAL	+25°C DC PER NSC RETS*	100%
PDA	10% MAX.	
	+125°C DC PER NSC RETS*	100%
	−55°C DC PER NSC RETS*	100%
	+25°C AC PER NSC RETS*	100%
QA ACCEPTANCE	GROUP A*** (SAMPLE, EACH LOT)	
QUALITY CONFORMANCE	GROUP B*** (SAMPLE, EACH INSPECTION LOT)	
	GROUP C*** (SAMPLE EVERY 90 DAYS PER MICROCIRCUIT GROUP)	
	GROUP D*** (SAMPLE, EVERY 6 MONTHS PER PACKAGE TYPE)	
EXTERNAL VISUAL	2009	100%

*RETS = REL ELECTRICAL TEST SPECIFICATION
**ALL METHODS TO CURRENT REVISION LEVELS
***ALL TESTS, LTPDs AND SAMPLE SIZES ARE AS DEFINED IN METHOD 5005

THIS IS TO CERTIFY THAT ALL 883B/RETS MATERIALS SUPPLIED ON YOUR PURCHASE ORDER COMPLY WITH ALL THE REQUIREMENTS, SPECIFICATIONS, AND DOCUMENTS PERTINENT TO THE NATIONAL 883B/RETS PROGRAM. ALL TEST DATA AND CERTIFICATION IS ON FILE AT OUR FACILITY.

NSC Part Number _____
Cust. Ref. Part Number_____
P.O. Number _____
Date Code(s) _____
Lot Code(s) _____

QUALITY ASSURANCE REPRESENTATIVE

1.0 Scope

1.1 Purpose

This document establishes the requirements for screening and processing of integrated circuits in accordance with MIL-STD-883, Class S where such devices are not available as M38510 Class S devices. These products shall be referred to as 883S/RETS™ microcircuits.

1.2 Intent

This program is intended to provide the user with the ability to procure 883S/RETS microcircuits. These are standardized integrated circuits manufactured and processed by National Semiconductor Corporation in accordance with the requirements of MIL-STD-883, for Class S devices as specified herein.

2.0 Applicable Documents

The following specifications and standards form a part of this specification to the extent specified herein.

2.1 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	General Specification for Microcircuits
MIL-C-45662	Calibration System Requirements
MIL-Q-9858	Quality System Requirements

2.2 Standards

Military

MIL-STD-105	Sampling Procedures and Tables
MIL-STD-883	Test Methods and Procedure for Microelectronics
MIL-STD-976	Certification Requirements for Microcircuits
MIL-STD-1331	Microelectronics Terms and Definitions

2.3 Detail Specification

The detail specification for a particular device is the National Semiconductor RETS (Reliability Electrical Test Specification — see Figure 1) or the MIL-M-38510 detail specification, as applicable. For devices which National Semiconductor has qualified to JM38510 Class S, this specification shall not apply. Those devices shall be furnished only as JAN devices. MIL-M-38510 test tapes will be utilized for those devices for which National Semiconductor intends to pursue qualification (contact factory for specifics).

3.0 Requirements

3.1 General

The individual requirements shall be as specified herein and in accordance with the applicable detail specification. The static and dynamic electrical performance requirements for the integrated circuits and electrical test methods shall be as specified in the detail specification.

3.1.1 Conflicting Requirements

In the event of conflict between the requirements of this specification and other requirements of the applicable device specification, the precedence in which requirements shall govern, in descending order, is as follows:

a) Applicable device specification (detail specification).

b) This specification.

c) Specifications, standards, and other documents referenced in Section 2.1.

3.1.2 Terms, Definitions, and Symbols

For the purpose of this specification, the terms, definitions, and symbols of MIL-STD-883, MIL-STD-1331, and MIL-M-38510 shall apply and shall be used wherever they are pertinent, except as follows:

a) Procuring Activity shall be that organization (either OEM manufacturer or government agency) which generates the actual purchase order or contract used to procure material under this specification. For material purchased through a franchised distributor, the procuring activity shall be that organization which places the purchase order or contract with the distributor.

b. The Qualifying Activity shall be National Semiconductor's Quality Assurance Department.

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RETS111X Revision B

Burn-In-Circuits
H: 8358HR; F: 8359HR; D: 8665HR

Test System: Teradyne J-273

Test Conditions (Unless Otherwise Specified)
V_{CC} = 15V, V_{CM} = 0V, V_{OUT} = 1.4V with respect to V_{CC-}, V_{56} = 0V, R_S = 0V

NOTES	Parameter	Symbol	Test Conditions	Δ Test Number	Test Number	RL-111XRI Subgroup 1 +25°C Min.	RL-111XRI Subgroup 1 +25°C Max.	RL-111XHG Subgroup 2 +125°C Min.	RL-111XHG Subgroup 2 +125°C Max.	RL-111XLG Subgroup 3 −55°C Min.	RL-111XLG Subgroup 3 −55°C Max.	Optional Drift Δ Limits (25°C) (note 3)	Units of Measure
	Input Offset Voltage	V_{IO}	V_{CM} = +13.5V, −14.5V and 0V (note 4)	105, 113	5, 13, 20		3.0		4.0		4.0	±0.5	mV
			R_S = 50KΩ, V_{CM} = +13.5V, −14.5V and 0V	106, 114, 121	6, 14, 21		3.0		4.0		4.0	±0.5	mV
			$V_{85} = V_{86}$ = 0V, V_{CM} = +13.5V, −14.5V, 0V		8, 16, 23		3.0						mV
			$V_{85} = V_{86}$ = 0V, V_{CM} = +13.5V, −14.5V, 0V, R_S = 50KΩ		9, 17, 24		3.0						mV
			V+ = 4.5V, V− = 0V, V_{OUT} = 0.4V, V_{CM} = 3V, 0.5V		27, 29		5.0		6.0		6.0		mV
			V+ = 4.5V, V− = 0V, V_{OUT} = 0.4V, V_{CM} = 3V, 0.5V		28, 30		3.0		4.0		4.0		mV
	Input Offset Current	I_{IO}	R_S = 50KΩ, V_{CM} = +13.5V, −14.5V and 0V		7, 15, 22		10		20		20		nA
			$V_{85} = V_{86}$ = 0V, R_S = 50KΩ, V_{CM} = 13.5V, −14.5V, 0V		10, 18, 25		30						nA
	Input Bias Current	I_{IB}	R_S = 50KΩ, V_{CM} = +13.5V, −14.5V, 0V (note 5)	126	11, 19, 26		100		100		150	±10	nA
	Large Signal Gain	A_{VS}	R_L = 1KΩ, V_{OUT} = −12V to +35.0V		31	40		30		30			V/mV
	Emitter Follower Gain	A_{VEF}	R_L = 600Ω, V_I = −15V to +12V		32	10		8.0		8.0			V/mV
	Common Mode Rejection Ratio	CM_{RR}	+13.5V ≥ V_{CM} ≥ −14.5V		12	80		80		80			dB
6	Negative Supply Current	I_{CC-}		101	1.0		−5.0		−5.0		−15	±0.5	mA
6	Positive Supply Current	I_{CC+}			2.0		6.0		6.0		15		mA
	Input Leakage Current	I_{IL1}	V_{CC} = ±18V, V_{28} = 1V, V_{38} = 30V, V_{OUT} = 50V with respect to V_{CC-}		3.0		10		30				nA
		I_{IL2}	V_{CC} = ±V_{28} = 30V, V_{38} = 1V, V_{OUT} = 50V with respect to V_{CC-}		4		10		30				nA
	Output Leakage Current	I_{LOUT}	V_{CC} = ±18V, 15+15 = 5mA, V_{OUT} = 35V with respect to V_{CC-}		33		10		500				nA
	Ground Leakage Current	I_{LG}	As in I_{LOUT}		34		25		500				nA
	Saturation Voltage	V_{SAT}	I_{OUT} = 50mA, V_{IN} = −5mV		35		1.5						V
			I_{OUT} = 8ma, V_{IN} = −6mV		36		0.4		0.4		0.4		V
2	Strobe ON Current	I_{STR}					4.0						mA

SAMPLE ONLY

The RETS details National's standard electrical testing with the following key information clearly identified:

A. RETS number and revision level.
B. Standard Burn-in circuits.
C. Basic Test system, test tapes and revisions.
D. Test numbers (including Δ tests)
E. Recommended Δ's (which are standard on 883S/RETS™ microcircuits).
F. Special test equipment (where applicable).
G. Clear definition of test conditions.
H. Clear footnotes, where necessary.
I. Part number and function.

Note 4: Δ computed at V_{CM} = +13.5V and −14.5V only
Note 5: Δ computed at V_{CM} = 0V only
Note 6: −55°C tests are for continuity check only

Note 1: Parameter tested go no go only, cannot be data logged.
Note 2: Guaranteed parameter, no testing is available.
Note 3: Drift limits apply to Class S devices only.

Device: LM111 **Function:** Voltage Comparator

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3.1.3 Country of Manufacture

All 883S/RETS™ microcircuits provided under this specification shall be manufactured, assembled and tested within the U.S. and its territories.

3.1.4 Line Certification

883S/RETS microcircuits provided under this specification shall be fabricated and assembled in the United States on lines which have been certified for the fabrication and assembly of JAN microcircuits in accordance with the requirements of MIL-STD-976 and MIL-M-38510. (Note: This is not to be interpreted as implying in any way that parts supplied to this specification are JAN qualified devices.)

3.2 Product Assurance Requirements

883S/RETS microcircuits shall be those which have been subjected to, and passed all applicable requirements, tests, and inspections detailed herein, including wafer lot acceptance screening, qualification, and quality conformance inspection requirements. Where shown, method references are per MIL-STD-883.

3.2.1 Qualification

883S/RETS microcircuits furnished under this specification shall be products which have been produced and tested and have passed the qualification tests specified herein. The required qualification tests shall be Group A, Group B, and Group D testing as specified in Tables I, II, and III of this specification.

3.2.2 Screening

All 883S/RETS microcircuits to be delivered in accordance with this specification shall have been subjected to, and passed, all the screening tests detailed in Method 5004 of MIL-STD-883 for Class S devices (See Figure 2).

3.2.3 Quality Conformance Inspection

Microcircuits shall not be accepted or approved for delivery until the inspection lot has passed quality conformance inspection (see Section 5.1).

3.2.4 Wafer Lot Acceptance

883S/RETS microcircuits furnished under this specification shall be products from wafer lots that have been subjected to and have successfully met the wafer lot acceptance inspections and tests specified in Table IV. For radiation hardened devices only, wafer lot acceptance shall include total dose radiation testing.

3.2.5 Traceability

For 883S/RETS microcircuits, each delivered microcircuit shall be traceable to the inspection lot, inspection sublot, and wafer lot.

3.2.6 In-Process Verification and Die Attach Lead Bonding

Die attach and bonding operations shall be monitored in accordance with MIL-M-38510. Samples will be taken at the beginning of the shift and every two hours thereafter.

3.3 Design Documentation

National Semiconductor shall retain on file the design and construction information required by MIL-M-38510.

3.4 Internal Conductors

Internal thin film conductors on silicon die (metallization stripes, contact areas, bonding interfaces, etc.) shall meet the current density requirements of MIL-M-38510.

3.5 Lead Material and Finish

Lead material and finish shall be as defined in MIL-M-38510.

3.6 Glassivation

All 883S/RETS microcircuits shall be glassivated. The minimum glassivation thickness shall be 6,000 Å for SiO_2 or 2,000 Å for Si_3N_4. The glassivation/nitridation shall cover all electrical conductors except the bonding pads.

3.7 Die Thickness

Unless otherwise specified, the minimum die thickness shall be 0.006 inch (0.15 mm).

3.8 Marking

3.8.1 Marking on Each Device

As a minimum, the following marking shall be placed on each microcircuit:

a) Index point (see 3.8.4).
b) Part number (see 3.8.5).
c) Product assurance level (see 3.8.6).
d) Inspection lot identification code (see 3.8.8).
e) National Semiconductor identification (see 3.8.9).
f) Country of Origin (see 3.8.10).
g) Serial number (see 3.8.11).
h) Total dose radiation identifier (see 3.8.12), where applicable.

3.8.2 Marking on Initial Container

All of the marking specified in Section 3.8.1, except the index point, shall appear on the initial protection or wrapping for delivery. The serial number range shall be shown rather than individual serial numbers.

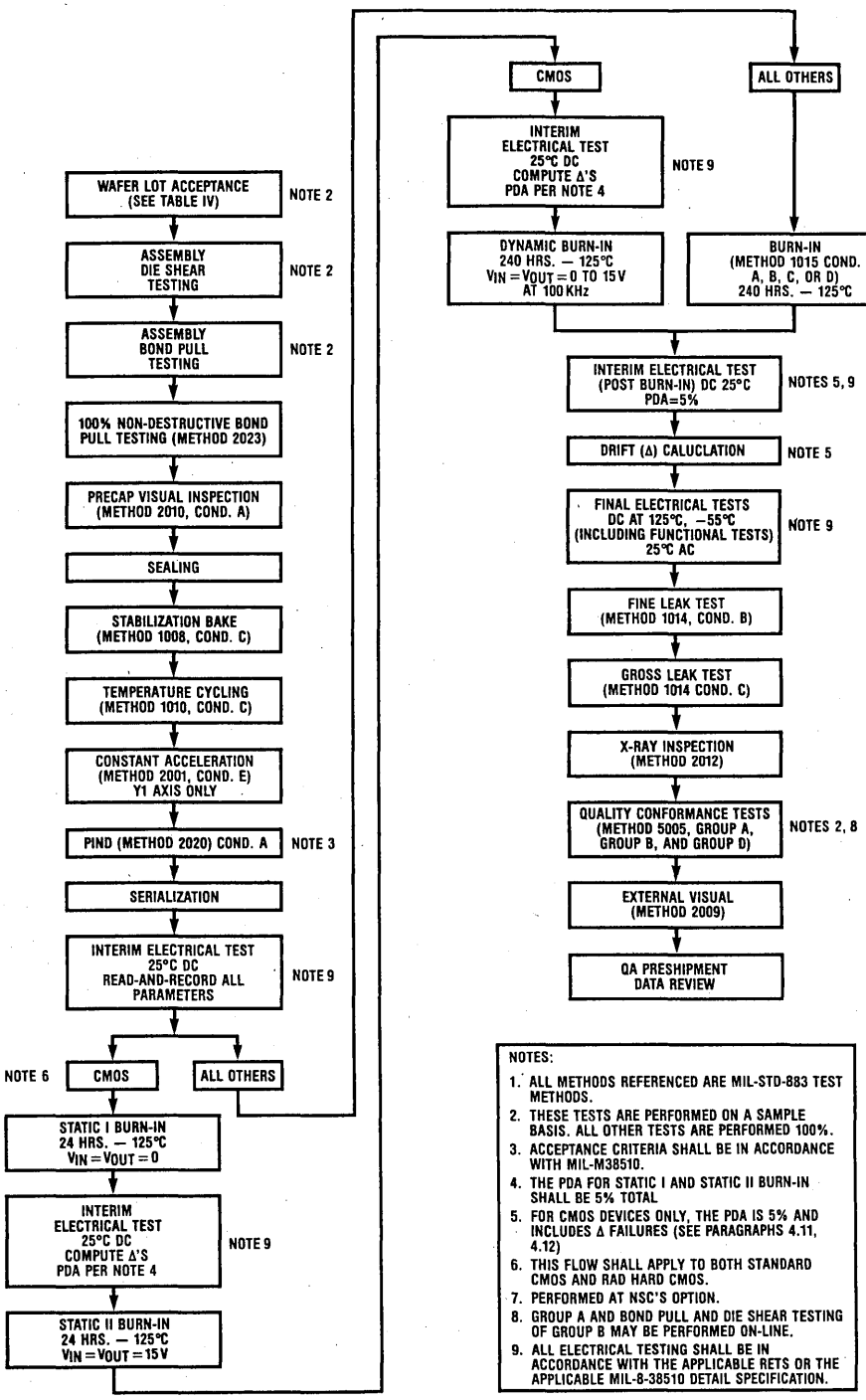


Figure 2. 883S/RETS™ PRODUCT Screening Flow (per MIL-STD-883, method 5004 and MIL-M-38510)

3.8.3 Marking Permanence

Marking shall be permanent in nature and remain legible after testing. Damage to marking caused by mechanical fixturing in Group B and D tests shall not be cause for lot rejection.

3.8.4 Index Point

The index point indicating the starting point for numbering of leads and/or mechanical orientation of the integrated circuit may be a tab, color dot, or other suitable indicator.

3.8.5 Part Number

The part number shall be the National Semiconductor part number.

3.8.6 Product Assurance Level

883S/RETS™ microcircuits shall be marked with a code indicating the product assurance level to which they have been tested and found to conform. The code shall consist of /883 followed by the letter S.

3.8.7 Formation of Lots

883S/RETS microcircuits shall be assembled into inspection lots and sublots as required to meet the product assurance inspection and test requirements of this specification. An inspection lot and sublot shall be as defined in MIL-M-38510. An inspection sublot may not contain dice from more than one wafer lot.

3.8.8 Inspection Lot Identification Code

Integrated circuits shall be marked by a 4-digit date code indicating the date the lot was sealed. The first 2 numbers in the code shall be the last 2 digits of the number of the year. The third and fourth numbers shall be 2 digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. When an inspection lot contains more than one inspection sublot, an alpha character will be suffixed to the date code to maintain wafer lot and inspection sublot traceability (see paragraph 3.2.5). National Semiconductor shall prefix this date code with an alpha character indicating the point of assembly (F for Santa Clara, Y for Tucson).

3.8.9 National Semiconductor Identification

Integrated circuits shall be marked with the National Semiconductor logo (▨).

3.8.10 Country of Origin

The letters "U.S.A." shall be marked below or adjacent to the other specified markings.

3.8.11 Serialization

Prior to the first recorded electrical measurement in screening, each 883S/RETS microcircuit shall be marked with a unique serial number. This serial number allows traceability of test results to the individual microcircuit within that inspection lot. Inspection lot records shall be maintained to provide traceability from the serial number to the specific wafer lot from which the devices originated.

3.8.12 Total Dose Radiation Identifier

Devices which have been subjected to and have passed total dose radiation testing in accordance with Method 1019 of MIL-STD-883 shall be marked with a total dose radiation identifier as specified in the applicable procurement document.

3.8.13 Marking Location and Sequence

Unless otherwise specified, the part number, inspection lot identification code, and serialization (where applicable) shall be located on the top surface of flat packages or dual-in-line configurations and on either the top or the side of cylindrical packages (TO-99 and similar configurations). The index point shall be marked as specified in Appendix C of MIL-M-38510. The balance of the markings may be placed in any suitable location so as to perform their required functions and not interfere with the other markings. Where package size prohibits marking of all information shown in Section 3.8.1, the order of priority for inclusion shall be a, b, d, g, c, h, e, f.

4.0 Conditions and Methods of Test

Conditions and methods of test shall be in accordance with Method 5004 of MIL-STD-883 and as specified herein on a 100% basis. The general requirements of MIL-STD-883 apply as applicable. This section establishes the stress screening tests and test methods for this program. The purpose of these tests is to assure the quality and reliability of the product to a level commensurate with the product's intended application.

4.1 Non-Destructive Bond Pull

Non-destructive bond pull testing shall be performed on 100% of all devices prior to internal visual inspection in accordance with MIL-STD-883 Method 2023.

4.2 Internal Visual Inspection (Precap)

Internal visual inspection shall be performed per MIL-STD-883, Method 2010 Condition A.

4.3 Stabilization Bake

Stabilization bake shall be performed per MIL-STD-883, Method 1008, Condition C. The devices shall be stored for 24 hours minimum at 150°C minimum.

4.4 Temperature Cycling

Temperature cycling shall be performed per MIL-STD-883, Method 1010, Condition C, 10 cycles, from −65°C to +150°C.

4.5 Constant Acceleration

Constant acceleration shall be performed per MIL-STD-883, Method 2001, Condition E, at 30,000 Gs in the Y_1 axis only.

4.6 Particle Impact Noise Detection (PIND)

Particle impact noise detection testing shall be performed in accordance with MIL-STD-883, Method 2020 Condition A and MIL-M-38510.

4.7 Serialization

Each unit shall be serialized (see paragraph 3.8.11).

4.8 Interim Electrical Parameters (Pre Burn-In)

Interim electrical parameters shall be the 25°C DC parameters, specified in the detail specification. All 25°C DC parameters specified on the RETS or the MIL-M-38510 detail specification (as applicable) shall be read and recorded.

4.9 Burn-In

Burn-in shall be performed per MIL-STD-883, Method 1015, Conditions A, B, C or D, at the supplier's discretion. (Burn-in condition varies with product type.) For CMOS devices, the burn-in sequence shall include Static I, Static II, and Dynamic Burn-in (as shown in Figure 1).

The ambient temperature shall be 125°C, and the duration shall be 240 hours minimum, or equivalent in accordance with Method 1015. For CMOS devices, the Static I and Static II burn-in shall each be 24 hours in duration.

4.10 Interim Electrical Parameters (Post Burn-In)

The measurements defined in paragraph 4.8 shall be repeated. The PDA shall be 5.0%. For CMOS, the PDA shall be 5% for the Static I and Static II burn-ins combined and 5% for the Dynamic Burn-in. Drift limits (see 4.11) will be included in the PDA only for CMOS.

4.11 Delta Calculation

Deltas shall be computed for all parameters for which drift limits are established by the RETS or MIL-M-38510 detail specification (as applicable). All units failing the drift limits shall be removed from the lot. Drift limit failures shall not be included in the PDA (see 4.10) only for CMOS devices.

4.12 Final Electrical Parameters

Final electrical parameters shall be as defined in the applicable detail specification. DC testing shall be performed at +25°C, −55°C, and +125°C (except that any 25°C tests performed in 4.10 need not be repeated), and AC tests shall be performed at 25°C unless otherwise specified.

4.13 Hermeticity

Hermeticity test shall be performed per the following to determine the seal integrity of the package.

Fine Leak Testing: Fine leak testing shall be performed per MIL-STD-883, Method 1014, Condition B. The rejection criteria shall be per MIL-STD-883.

Gross Leak Testing: Gross leak testing shall be performed per MIL-STD-883, Method 1014, Condition C. The rejection criteria shall be per MIL-STD-883.

4.14 Radiographic Inspection

Radiographic inspection shall be performed in accordance with MIL-STD-883, Method 2012.

4.15 Quality Conformance Testing

Samples shall be randomly selected from the lot, and quality conformance inspection shall be performed in accordance with 5.0.

4.16 External Visual Inspection

All 883S/RETS™ microcircuits shall receive external visual inspection per MIL-STD-883, Method 2009.

5.0 Quality Assurance Provisions

5.1 Quality Conformance Inspection

Quality conformance inspection shall be in accordance with Tables I, II, and III. Inspection lot sampling shall be in accordance with Method 5005 of MIL-STD-883. Inspection lots failing to meet quality conformance inspection for the Class S product assurance level shall be rejected.

5.1.1 Group A Inspection

Group A inspection shall consist of the electrical parameters in the RETS or MIL-M-38510 detail specification (as applicable). Each inspection lot shall be subjected to Group A (see Table I). Group A testing may be performed on-line.

5.1.2 Group B Inspection

Group B inspection consists of those tests specified in Table II. Group B tests will be performed on every inspection lot, unless specifically waived by the procuring activity.

5.1.3 Group D Inspection

Group D testing consists of those package oriented tests specified in Table III. Group D testing will be performed within National's 883S/RETS™ program once every 6 months per package type, unless specifically waived by the procuring activity.

6.0 Data

6.1 Data Shipped with Parts

One copy of the following data shall be provided with each shipment of 883S/RETS microcircuits:

a. Attributes and variables data for 100% screening.
b. X-ray report.
c. Wafer lot acceptance test results.
d. The applicable RETS.

6.2 Data Retained on File

The following data will be maintained on file at National Semiconductor for 3 years (copies are available upon special request):

a. X-ray film (radiographs).
b. SEM photos.
c. Attributes and variables data for Quality Conformance testing.

7.0 Packaging

Packing and packaging shall be in accordance with MIL-M-38510.

8.0 Hybrid Devices

Hybrid devices are not available through this 883S/RETS product program, but a hybrid Class S flow is defined in our brochure "883S/RETS Hybrids from National Semiconductor."

9.0 Radiation Susceptibility Data

National Semiconductor has a program for providing radiation susceptibility data on selected 883S/RETS device types. Contact the factory for details.

Table I. Group A Electrical Test
(per Method 5005, Table I)

Subgroups	Class S LTPD
Subgroup 1 Static tests at 25°C	5
Subgroup 2 Static tests at 125°C	7
Subgroup 3 Static tests at −55°C	7
Subgroup 4 (Note 1) Dynamic tests at 25°C	5
Subgroup 5 (Note 1) Dynamic tests at 125°C	7
Subgroup 6 (Note 1) Dynamic tests at −55°C	7
Subgroup 7 (Note 1) Functional tests at 25°C	5
Subgroup 8 (Note 1) Functional tests at 125°C and −55°C	10
Subgroup 9 Switching tests at 25°C	7
Subgroup 10 Switching tests at 125°C	10
Subgroup 11 Switching tests at −55°C	10

Notes:

1. National will normally perform these subgroups at the same time as subgroups 1, 2, and 3 respectively.
2. Group A testing may be performed on-line.

Table II. Group B Inspection
(per Method 5005, Table IIA)

TEST	MIL-STD-883 METHOD	CONDITIONS	CLASS S LTPD OR SAMPLE SIZE
Subgroup 1			
a) Physical dimensions	2016		2 devices (0 failures)
b) Internal Water Vapor Content	1018	(Note 4)	3 devices (0 failures) or 5 devices (1 failure)
Subgroup 2 (Note 1)			
a) Resistance to solvents	2015		4 devices (0 failures)
b) Internal visual for DPA	2013 and 2014	Failure criteria from design & construction requirements of applicable procurement document	2 devices (0 failures)
c) Bond strength	2011	Test condition C or D	LTPD = 10 (Note 6)
d) Die shear	2019	Per Method 2019 for applicable die size	3 devices (0 failures)
Subgroup 3			
Solderability (Note 2)	2003	Soldering temperature of 260 ± 10°C	LTPD = 15 (note 5)
Subgroup 4			
a) Lead integrity	2004	Test condition B2	2 devices (0 failures)
b) Seal (fine and gross)	1014	Cond. B or C, as applicable	
c) Lid Torque	2024	As applicable (Note 4)	
Subgroup 5 (Note 3)			LTPD = 5
a) Electrical parameters		Per applicable detail specification (Note 7)	
b) Operating life	1005	Test condition A, B, C or D	
c) Electrical parameters		Per applicable detail specification (Note 7)	
d) Seal (fine and gross)	1014	Cond. B or C, as applicable	
Subgroup 6 (Note 3)			
a) Electrical parameters		Per applicable detail specification (Note 8)	LTPD = 15
b) Temperature cycling	1010	Test condition C, 100 cycles min.	
c) Constant acceleration	2001	Test condition E, Y1 axis only	
d) Seal (fine and gross)	1014	Condition B or C, as applicable	
e) Electrical parameters		Per applicable detail specification (Note 8)	
Subgroup 7 (Note 9)			
a) Electrical parameters		Per applicable detail specification (subgroup 1 of Group A)	LTPD = 15(0)
b) Electrostatic discharge sensitivity	3015		
c) Electrical parameters		Per applicable detail specification (subgroup 1 of Group A)	

Notes:

1. Samples subjected to this subgroup shall have been through the entire sequence of Subgroup 6 testing.
2. All samples shall have seen 240 hours at 125°C (or equivalent).
3. Resubmission of failed lots shall be in accordance with MIL-M-38510.
4. Required only for packages utilizing glass-frit sealing. (National Semiconductor provides only solder- and weld-sealed packages for Class S processed devices.)
5. Sample leads must come from a minimum of three units.
6. Sample bonds must come from a minimum of four units.
7. Read-and-record subgroups 1, 2, and 3 of Group A. Screen subgroups 4-11 of Group A.
8. Read-and-record subgroups 1, 2, and 3 of Group A.
9. Only required for initial qualification and after product redesign.

Table III. Group D Inspection
(per Method 5005, Table IV)

TEST	MIL-STD-883 METHOD	CONDITIONS	CLASS S LTPD
Subgroup 1 Physical dimensions	 2016		LTPD = 15
Subgroup 2 (Note 1) a) Lead integrity b) Seal (fine and gross) c) Lid torque	 2004 1014 2024	 Test conditions B2 (lead fatigue) Cond. B or C, as applicable As applicable (Note 3)	LTPD = 15
Subgroup 3 a) Thermal shock b) Temperature cycling c) Moisture resistance d) End point electrical parameters e) Seal (fine and gross) f) Visual examination	 1011 1010 1004 1014 1004	 Test condition B — 15 cycles Test condition C — 100 cycles Per applicable detail specification (Note 4) Cond. B or C, as applicable	LTPD = 15
Subgroup 4 a) Mechanical shock b) Vibration variable frequency c) Constant acceleration d) Seal (fine and gross) e) Visual examination f) End point electrical parameters	 2002 2007 2001 1014 1010 	 Test condition B Test condition A Test condition E, Y1 axis only Cond. B or C as applicable Per applicable detail specification (Note 4)	LTPD = 15
Subgroup 5 (Note 1) a) Salt atmosphere b) Seal (fine and gross) c) Visual examination	 1009 1014 1009	 Test condition A Condition B or C, as applicable Paragraph 3.3.1 of Method 1009	LTPD = 15
Subgroup 6 (Note 1) Internal water-vapor content	 1018	 5000 ppm maximum water content at 100°C	3 devices (0 failures) or 5 devices (1 failure)
Subgroup 7 (Note 1) Adhesion of lead finish	 2025		LTPD = 15

NOTES:
1. Electrical rejects from the same inspection may be used.
2. Resubmission of failed lots shall be in accordance with MIL-M-38510.
3. Required only for packages utilizing glass-frit sealing. (National Semiconductor provides only solder- and weld-sealed packages for Class S processed devices.)
4. Subgroups 1, 2, and 3 of Group A.

Table IV. Wafer Lot Acceptance

Test	Limit		Sampling Plan	Notes
1. Wafer Thickness	Design Nominal ±2.0 mil. (±0.002 inches) 6.0 mil. (0.006 inches) minimum		Two wafers per wafer lot at incoming inspection.	1
2. Metallization Thickness	a) Conductor metal: 8 kÅ minimum for single level metal and top layer of multi-level metal. 6 kÅ minimum for lower level metal, with a maximum deviation of ±20% from design nominal. b) Barrier metal: ±30% of design nominal		One wafer per metallization run.	
3. Thermal Stability (ΔV_{FB} or ΔV_T)	Process Technology	Limit	One wafer (or monitor) per lot.	2, 3
	Bipolar digital devices operating at greater than 10V and containing no MOS transistors.	⩽0.75V		
	Bipolar linear devices containing no MOS transistors.			
	Bipolar digital devices operating at greater than 10V and containing MOS structures.	⩽1.0V		
	Bipolar linear devices operating at greater than 5.0V and containing MOS transistors.			
	All MOS devices	⩽0.4V		
4. SEM	Per MIL-STD-883, Method 2018		Two wafers per metallization run.	
5. Glassivation Thickness	±20% of design nominal 6 kÅ minimum for SiO_2 2 kÅ minimum for Si_3N_4		Two wafers or test chips per glassivated lot.	
6. Gold Backing Thickness	Per approved design nominal thickness and tolerance.		One wafer per lot.	4
7. Total Dose Radiation	Per MIL-STD-883, Method 1019 Subsequent to radiation, test samples shall pass the post test radiation limits specified by the applicable MIL-M-38510 detail specification or the National Semiconductor radiation specification. In addition, all test samples shall pass subgroup 7 of Group A. Dose rate shall be as specified in the applicable procurement document.		As required by the applicable procurement document.	5

NOTES:

1. This test is not required when the finished wafer design thickness is greater than 10 mils (0.010 inches).
2. Required only for bipolar digital operating at 10V or more, all linear, and all MOS.
3. All readings will be normalized to an oxide thickness of 1000 Å.
4. Required only for gold-backed wafers.
5. Required only for radiation-hardened devices, when specified in the applicable procurement document.

AH0014 DPDT/AH0015 Quad SPST/AH0019 Dual DPST Analog Switches

Absolute Maximum Ratings

V_{CC} Supply Voltage	7.0V
V^- Supply Voltage	−30V
V^+ Supply Voltage	+30V
V^+/V^- Voltage Differential	40V
Logic Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

This series of TTL/DTL compatible MOS analog switches feature high speed with internal level shifting and driving.

The package contains two monolithic integrated circuit chips: the MOS analog chip is similar to the MM450 type which consists of four MOS analog switch transistors. The second chip is a bipolar IC gate and level shifter. The series is available in both hermetic dual-in-line package and flatpack.

These switches are particularly suited for use in both military and industrial applications such as commutators in data acquisition systems, multiplexers, A/D and D/A converters, long time constant integrators, sample and hold circuits, modulators/demodulators, and other analog signal switching applications.

Features

- Large analog voltage switching ± 10V
- Fast switching speed 500ns
- Operation over wide range of power supplies
- Low ON resistance 200Ω
- High OFF resistance $10^{11}\Omega$
- Fully compatible with DTL or TTL logic
- Includes gating and level shifting

RETS0014D, Rev A; RETS0019D, Rev A; RETS0015D, Rev 1A (Teradyne W-301)

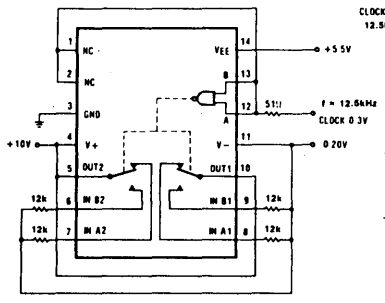
Parameter	Conditions (Note 1)		+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Logical "1" Input Voltage (Note 2) (V_{IH})	V_{CC} = 4.5V		2.0		2.0		2.0			V
Logical "0" Input Voltage (Note 2) (V_{IL})	V_{CC} = 4.5V			.8		.8		.8		V
Logical "1" Input Current (I_{IH})	V_{CC} = 5.5V, V_{IN} = 2.4V			5		5		5		μA
	V_{CC} = 5.5V, V_{IN} = 5.5V			1		1		1		mA
Logical "0" Input Current (I_{IL})	V_{CC} = 5.5V, V_{IN} = 0.4V			−400		−400		−400		μA
Analog Switch ON Resistance (R_{ON})	I_{IN} = −1mA ($V_{IN} \simeq +10V$)			200		200		200		Ω
	I_{IN_X} = 1mA ($V_{IN} \simeq -10V$)			600		600		600		Ω
Logical "0" Supply Current (ICC_L)	V_{CC} = 5.5V, V_{IN} = 0	AH0014		3.0		3.0		3.0		mA
		AH0015		1.64		1.64		1.64		mA
		AH0019		.82		.82		.82		mA
Logical "1" Supply Current (ICC_H)	V_{CC} = 5.5V, V_{IN} = 4.5V	AH0014		1.6		1.6		1.6		mA
		AH0015		6.4		6.4		6.4		mA
		AH0019		3.2		3.2		3.2		mA
Analog Switch Output Leakage (Note 3) (I_{LO})	V_{CC} = 5V, V_{OUT} = −10V			.4		400				nA
Analog Switch Input Leakage (Note 3) (I_{LI})	V_{CC} = 5V, V_{IN} = −10V			.2		200				nA
Analog Input (Drain) Capacitance (Note 4) (C_{IN})	1MHz at Zero Bias			10		10		10		pF
Output (Source) Capacitance (Note 4) (C_{OUT})	1MHz at Zero Bias			13		13		13		pF
Temperature Coefficient of Input/Output Leakage (Note 4)			Doubles every 10 degrees Centigrade							
Analog Turn-OFF Time (t_{OFF})	R_L = 6.8kΩ			500						ns
Analog Turn-ON Time (t_{ON})	R_L = 6.8kΩ	AH0014		425						ns
		AH0015, AH0019		150						ns

Notes:

1. V^+ = 10V, V^- = −20V, V_{CC} = 5V (4.5V for AH0019) except where otherwise specified.
2. Tested go-no-go only.
3. Leakage currents at 25°C and −55°C are guaranteed thru +125°C testing.
4. Guaranteed parameter, no testing available.

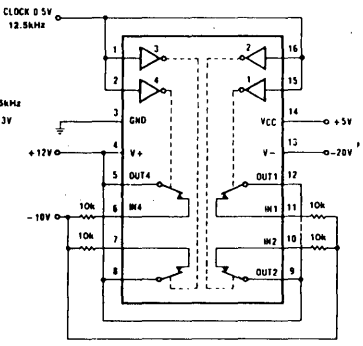
Burn-In Circuits

Dual-In-Line Package (9410HR)



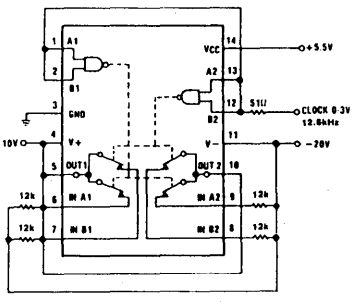
AH0014D
Top View

Dual-In-Line Package (8738HR)



AH0015D
Top View

Dual-In-Line Package (9410HR)



AH0019D
Top View

AH0120/AH0130/AH0140/AH0150/AH0160 Series Analog Switches

Absolute Maximum Ratings

	Levels High	Levels Medium
Total Supply Voltage ($V^+ - V^-$)	36V	34V
Analog Signal Voltage ($V^+ - V_A$ or $V_A - V^-$)	30V	25V
Positive Supply Voltage to Reference ($V^+ - V_R$)	25V	25V
Negative Supply Voltage to Reference ($V_R - V^-$)	22V	22V
Positive Supply Voltage to Input ($V^+ - V_{IN}$)	25V	25V
Input Voltage to Reference ($V_{IN} - V_R$)	±6V	±6V
Differential Input Voltage ($V_{IN} - V_{IN2}$)	±6V	±6V
Input Current, Any Terminal	30mA	30mA
Power Dissipation (Note 1)	500mW	500mW
Operating Temperature Range	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	
Lead Temperature (Soldering, 10 sec)	300°C	

General Description

The AH0100 series represents a complete family of junction FET analog switches. The inherent flexibility of the family allows the designer to tailor the device selection to the particular application. Switch configurations available include dual DPST, dual SPST, DPDT, and SPDT. $r_{DS(ON)}$ ranges from 10 ohms through 100 ohms. Parts are pin compatible with the popular DG100 series.

RETS0126X, Rev A RETS0129X, Rev A RETS0133X, Rev B RETS0134X, Rev B	RETS0139X, Rev - RETS0140X, Rev A RETS0141X, Rev A RETS0142X, Rev -	RETS0143X, Rev A RETS0144X, Rev - RETS0145X, Rev A RETS0146X, Rev -	RETS0151X, Rev - RETS0152X, Rev A RETS0153X, Rev - RETS0154X, Rev A	RETS0160X, Rev - RETS0162X, Rev A RETS0163X, Rev - RETS0164X, Rev -	(Teradyne W-301)

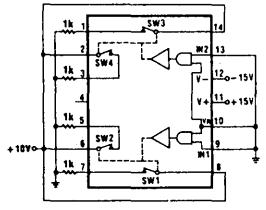
Parameter	Conditions (Note 3)		+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 5) Δ Limit (25°C)	Units
Switch ON Resistance (R_{ON})	I_D = 10mA	AH0140, AH0141, AH0145, AH0146		10		20		20	±5	Ω
		AH0129, AH0133, AH0139, AH0144		30		60		60	±5	Ω
		AH0126, AH0134, AH0142, AH0143		80		150		150	±10	Ω
		AH0153, AH0151, AH0163, AH0161		15		30		30	±5	Ω
		AH0154, AH0152, AH0164, AH0162		50		100		100	±10	Ω
Driver Leakage Current (Note 3) (I_{DL})	$V_D = V_S = -20V$	AH0126-AH0146		1		100		100		nA
		AH0151-AH0164		2		500		500		nA
Switch Leakage Current (Note 3) (I_{SL})	$V_{DS} = \pm 20V$	AH0126-139, AH0142-144		1		100		100		nA
		AH0140, AH0141, AH0145, AH0146		10		1000		1000		nA
		AH0151, AH0153, AH0161, AH0163		10		1000		1000		nA
		AH0152, AH0154, AH0162, AH0164		2		200		200	±10	nA
Logical "1" Input Current (I_{IH})	V_{IN} = 2.5			60		120		120		μA
Logical "0" Input Current (I_{IL})	V_{IN} = .8V			.1		2		2		μA
Positive Supply Current (Switch OFF)	$V_{IN1} = V_{IN2}$ = .8V			10		25		25		μA
(Switch ON)	V_{IN} = 2.5V (one driver)			3.0		3.3		3.3		mA
Negative Supply Current (Switch OFF)	$V_{IN1} = V_{IN2}$ = .8V			−10		−25		−25		μA
(Switch ON)	V_{IN} = 2.5V (one driver)			−1.8		−2.0		−2.0		mA
Reference Input (Enable) Current ON (I_{REFON})	$V_{IN1} = V_{IN2}$ = .8V			−10		−25		−25		μA
OFF (I_{REFOFF})	V_{IN} = 2.5V (one driver)			−1.4		−1.6		−1.6		mA
Switch Turn-On Time (Note 4) (t_{ON})	V_A = ±10V, R_L = 1kΩ	AH0126-139, AH0142-144		0.8						μs
		AH0140, AH0141, AH0145, AH0146		1.0						μs
	V_A = ±7.5V, R_L = 1kΩ	AH0151, AH0153, AH0161, AH0163		1.0						μs
		AH0152, AH0154, AH0162, AH0164		0.8						μs
Switch Turn-Off Time (Note 4) (t_{OFF})	V_A = ±10V, R_L = 1kΩ	AH0126-139, AH0142-144		1.6						μs
		AH0140, AH0141, AH0145, AH0146		2.5						μs
	V_A = ±7.5V, R_L = 1kΩ	AH0151, AH0153, AH0161, AH0163		2.5						μs
		AH0152, AH0154, AH0162, AH0164		1.6						μs

Notes:

1. At operating temperatures above 25°C, derate linearly to a maximum of 200mW at +125°C.
2. $V^+ = +12V$, $V^- = -18V$, $V_R = 0$, unless otherwise specified.
3. 25°C limits are guaranteed through 125°C measurements, but may be bench tested at extra cost.
4. Tested go-no-go only.
5. Class S only.

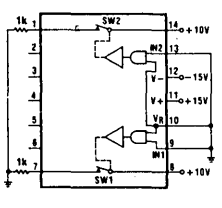
Burn-In Circuits

Dual Dpst (8515HR)



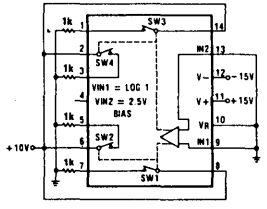
High Level (±10V)	Medium Level (±7.5V)
AH0140 (10Ω)	AH0153 (15Ω)
AH0129 (30Ω)	AH0154 (50Ω)
AH0126 (80Ω)	

Dual Spst (8515HR)



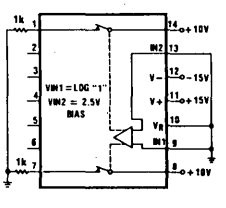
High Level (±10V)	Medium Level (±7.5V)
AH0141 (10Ω)	AH0151 (15Ω)
AH0133 (30Ω)	AH0152 (50Ω)
AH0134 (80Ω)	

DPDT (DIFF) (8515HR)



High Level (±10V)	Medium Level (±7.5V)
AH0145 (10Ω)	AH0163 (15Ω)
AH0139 (30Ω)	AH0164 (50Ω)
AH0142 (80Ω)	

SPDT (DIFF) (8515HR)



High Level (±10V)	Medium Level (±7.5V)
AH0146 (10Ω)	AH0161 (15Ω)
AH0144 (30Ω)	AH0162 (50Ω)
AH0143 (80Ω)	

AH2114 DPST Analog Switch

Absolute Maximum Ratings

V^+ Supply Voltage	+25V
V^- Supply Voltage	−25V
V^+-V^- Differential Voltage	40V
Logic Input Voltage	25V
Power Dissipation (Note 1)	1.36W
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 sec)	+200°C

General Description

The AH2114 is a DPST analog switch circuit comprised of two junction FET switches and their associated driver. The AH2114 is designed to fulfill a wide variety of high level analog switching applications including multiplexers, A to D Converters, integrators, and choppers. Design features include:

Features

- Low ON resistance, typically 75Ω
- High OFF resistance, typically $10^{11}\Omega$
- Large output voltage swing, typically ± 10V
- Powered from standard op-amp supply voltages of ± 15V
- Input signals in excess of 1 MHz
- Turn-ON and turn-OFF times typically 1μs

RETS2114X, Rev Preliminary (Teradyne W-301)

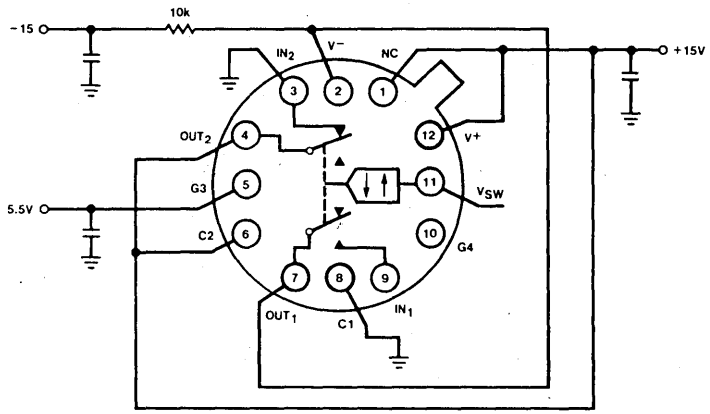
Parameter	Conditions (Note 2)	+25°C Min	+25°C Max	(Note 3) +125°C Min	(Note 3) +125°C Max	(Note 3) −55°C Min	(Note 3) −55°C Max	Δ Limit (25°C)	Units
Static Drain-Source "ON" Resistance (R_{ON})	I_O = 1.0mA, V_{GS} = 0		100		150		150		Ω
Drain-Gate Leakage Current (I_{OG})	V_{OS} = 20V, V_{GS} = −7V		1.0		60		60		nA
FET Gate-Source Breakdown Voltage (V_{GS})	V_{OS} = 0, I_G = 1μA	35		35		35			V
Drain-Gate Capacitance (C_{DG}) (Note 4)	V_{OG} = 20V, I_S = 0, f = 1MHz		5.0						pF
Source-Gate Capacitance (C_{SG}) (Note 4)	V_{OG} = 20 V, I_O, f = 1MHz		5.0						pF
DC Voltage range (V_{IN}) (Note 5)		±9							V
AC Voltage range (V_{IN}) (Note 4)		±9							V
Input 1 Turn-on time (t_{ON1}) (Note 4)	V_{IN1} = 10V		60						ns
Input 2 Turn-on time (t_{ON2}) (Note 4)	V_{IN2} = 10V		1.5						μs
Input 1 Turn-off time (t_{OFF1}) (Note 4)	V_{IN1} = 10V		.75						μs
Input 2 Turn-off time (t_{OFF2}) (Note 4)	V_{IN2} = 10V		80						ns

Notes:

1. Derate linearly at 100°C/W above 25°C.
2. V^+ = +15V, V^- = −15V, unless otherwise specified.
3. Temperature limits are guaranteed.
4. Guaranteed parameter.
5. Tested go-no-go only.

Burn-In Circuit

Metal Can Package
(9779HR)



Top View

Switch is shown in Logical "1" position

Note: All capacitors are .1μF every five sockets.

DH0006/DH0008 Current Drivers

Absolute Maximum Ratings

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0mA
Peak Output Current	DH0006H 1.5 Amp
(50ms On/1 sec Off)	DH0008H 3.0 Amp
Continuous Output Current	
(See continuous operating curves.)	
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C

General Description

The DH0006 and DH0008 are integrated high voltage, high current drivers designed to accept standard DTL or TTL logic levels and drive a load of up to 400mA at 28 volts for DH0006 and 3A at 45 volts for DH0008H. AND inputs are provided along with an Expander connection, should additional gating be required. The addition of an external capacitor provides control of the rise and fall times of the output in order to decrease cold lamp surges or to minimize electromagnetic interference if long lines are driven.

Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

Features

- Operation from a single +10V to +45V power supply
- Low standby power dissipation of only 35mW for 28V power supply
- 1.5A, 50ms pulse current capability (DH0006)
- 3.0A, 50ms pulse current capability (DH0008)

RETS0006H, Rev 1A; RETS0008H, Rev 1A (Teradyne W-301)

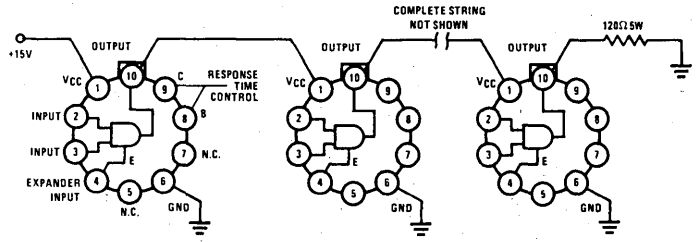
Parameter	Conditions		+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 3) Δ Limit (25°C)	Units
Logical "1" Output Voltage (V_{OH})	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 1.6A	DH0008	42		43		43			V
	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 800mA	DH0008	26.5		26.5		26.5		±.2	V
	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 400mA	DH0006	26.5		26.5		26.5		±.2	V
	V_{CC} = 10V, V_{IN} = 2.0V, I_{OUT} = 150µA	DH0006	8.8		8.8		8.8			V
Logical "0" Output Voltage (V_{OL})	V_{CC} = 45V, V_{IN} = .8V, R_L = 1kΩ	DH0006		10		10		10		mV
		DH0008		100		100		100		mV
Logical "1" Input Current (I_{IH})	V_{CC} = 45V, V_{IN} = 2.4V			5.0		5.0		5.0	±1.0	µA
	V_{CC} = 45V, V_{IN} = 5.5V			100		100		100		µA
Logical "0" Input Current (I_{IH})	V_{CC} = 45V, V_{IN} = .45V			−1.0		−1.0		−1.0		µA
"OFF" Power Supply Current (ICC_{OFF})	V_{CC} = 45V			2.0		2.0		2.0		mA
"ON" Power Supply Current (ICC_{ON})	V_{CC} = 45V, V_{IN} = 2V			8.0		8.0		8.0		mA
Logical "1" Input Voltage (Note 1) (V_{IH})			2.0		2.0		2.0			V
Logical "0" Input Voltage (Note 1) (V_{IN})				0.8		0.8		0.8		V
Input Breakdown Voltage (Note 1) (B_{VIN})			5.5		5.5		5.5			V
Rise Time (Note 2) (t_r)	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5V	DH0008		500						ns
Fall Time (Note 2) (t_f)	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5V	DH0008		4.0						µs
Turn On Time (Note 2) (t_{ON})	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5V	DH0008		1.0						µs
Turn Off Time (Note 2) (t_{OFF})	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5V	DH0008		10						µs
Rise Time (Note 2) (t_r)	V_{CC} = 28V, R_L = 82Ω	DH0006		300						ns
Fall Time (Note 2) (t_f)	V_{CC} = 28V, R_L = 82Ω	DH0006		1.5						µs
Turn On Time (Note 2) (t_{ON})	V_{CC} = 28V, R_L = 82Ω	DH0006		600						ns
Turn Off Time (Note 2) (t_{OFF})	V_{CC} = 28V, R_L = 82Ω	DH0006		5.2						µs
NAND output leakage (I_L)	V_{IN} = 0			40		40		40		mV

Notes:

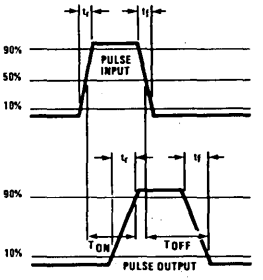
1. Tested go-no-go only.
2. Guaranteed parameter.
3. Class S only.

Burn-In Circuits

Metal Can Package (8248HR)



Switching Time Waveforms



DH0011 (SH2001) High Voltage, High Current Driver

Absolute Maximum Ratings

V_{CC}	8V
Collector Voltage (Output)	40V
Input Reverse Current	1.0mA
Power Dissipation	800mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to 150°C

General Description

The DH0011 high voltage, high current driver family consists of hybrid integrated circuits which provide a wide range of variations in temperature range, package, and output current drive capability. A summary of the variations is listed below.

Applications include driving lamps, relays, cores, and other devices requiring several hundred milliamp currents at voltages up to 40V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects the base of the output transistor.

RETS0011X, Rev 0A (Teradyne W-301, HDN-30-301-076)

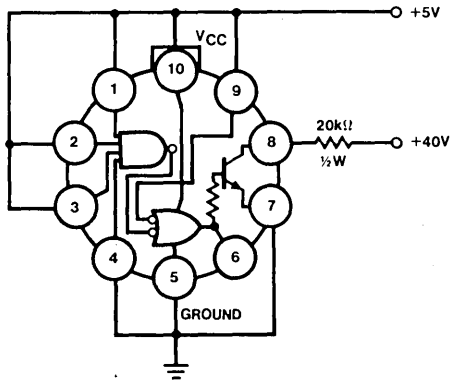
Parameter	Conditions	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 4) Δ Limit (25°C)	Units
Logical "0" Output Voltage at Output 1 (V_{OL})	V_{CC} = 4.5V, V_{IN} = Ⓐ (all inputs), I_{OUT} = 250mA		.4		.45		.45		V
	V_{CC} = 4.5V, V_{IN}(nand) = Ⓐ V_{IN}(nor) = Ⓑ, I_{OUT} = 250mA		.4		.45		.45		V
Logical "0" Output Voltage at Output 2 (V_{OL})	V_{CC} = 4.5V, V_{IN} = Ⓑ other inputs at Ⓐ, I_{OUT} = Ⓒ		.4		.45		.45		V
	V_{CC} = 4.5V, V_{IN} = Ⓐ, I_{OUT} = Ⓒ		.4		.45		.45		V
Logical "1" Input Current at NAND Inputs (I_{IH})	V_{CC} = 5.5V, V_{IN} = 4.0V, other inputs at 0, output open		2.0		5.0				μA
Logical "1" Input Current at NOR Input (I_{IH})	V_{CC} = 5.5V, V_{IN} = 4.0V, other inputs at Ⓐ, output open		2.0		5.0				μA
Logical "0" Input Current at NAND Inputs (I_{IL})	V_{CC} = 5.5V, V_{IN} = 0, other inputs at 4.0V, output open		−1.6		−1.5		−1.6		mA
Logical "0" Input Current at NOR Input (I_{IL})	V_{CC} = 5.5V, V_{IN} = 0, other inputs at Ⓐ, output open		−1.6		−1.5		−1.6		mA
Logical "1" Output Voltage at Output 2 (V_{OH})	V_{CC} = 4.5V, V_{IN} = Ⓐ, I_{OUT} = 0	2.0		1.8		2.2		±.2	V
Output Leakage Current (I_{LOUT})	V_{CC} = 4.5V, V_{IN} = Ⓐ, V_{OUT} = 40V		5.0		200				μA
Supply Current (I_{CC})	V_{CC} = 5.0V, V_{IN} = Ⓐ		30.6						mA
Breakdown Current (iBV_{CC})	V_{CC} = 8.0V, V_{IN} = Ⓐ		29.6						mA
Output Breakdown Voltage (Note 2) (BV_{CC})	V_{CC} = 4.5V, I_{OUT} = 5μA	40							V
	V_{CC} = 4.5V, I_{OUT} = 200μA			40					V
Logical "1" Input Voltage (Note 2) (V_{iH})		1.9		1.7		2.1			V
Logical "0" Input Voltage (Note 2) (V_{IL})			1.1		0.8		1.4		V
Turn-On Time (Note 3) (t_{ON})	V_{CC} = 5.0V		160						ns
Turn-Off Time (Note 3) (t_{OFF})	V_{CC} = 5.0V		220						ns

Notes:

1. See table below for Ⓐ, Ⓑ and Ⓒ forcing functions.
2. Tested go-no-go only.
3. Guaranteed parameter.
4. Class S only.

Burn-In Circuit

Metal Can Package (8432HR)



Top View

Forcing Functions

	25°C	125°C	−55°C	
Ⓐ	1.9	1.7	2.1	V
Ⓑ	1.1	0.8	1.4	V
Ⓒ	8	7.5	8	mA

DH0034 High Speed Dual Level Transistor

Absolute Maximum Ratings

V_{CC} Supply Voltage	7.0V
Negative Supply Voltage	−30V
Positive Supply Voltage	+25V
Differential Supply Voltage	25V
Maximum Output Current	100mA
Input Voltage	+5.5V
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The DH0034 is a high speed level translator suitable for interfacing to MOS or junction FET analog switches. It may also be used as a universal logic level shifter capable of accepting TTL/DTL input levels and shifting to CML, MOS, or SLT levels.

Features

- Fast switching. t_{pd0}: typically 15ns; t_{pd1}: typically 35ns.
- Large output voltage range: 25V
- Input is TTL/DTL compatible
- Low output leakage: typically 0.1μA
- High output currents: up to ±100mA

RETS0034D, Rev 3B; RETS0034H, Rev 3A (Teradyne W-301)

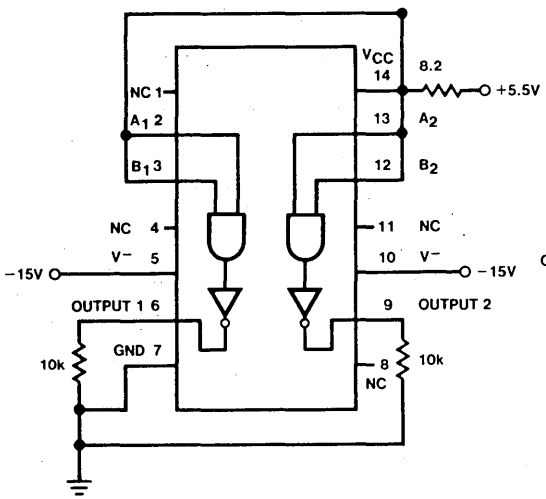
Parameter	Conditions (Note 2)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 1) Δ Limit (25°C)	Units
Logical "1" Input Current (I_{IH})	V_{IN} = 2.4V		40		40		40	±4	μA
	V_{IN} = 5.5V		1.0		1.0		1.0		mA
Logical "0" Input Current (I_{IL})	V_{IN} = .4V	−0.1	−1.6	−0.1	−1.6	−0.1	−1.6		mA
Power Supply Current (I_{CC})	V_{IN} = 4.5V		38		38		38		mA
	V_{IN} = 0		48		48		48		mA
Logical "0" Output Voltage (V_{OL})	V_{CC} = 14.5V, V^- = −15V, V_{IN} = 12V, I_{OUT} = 50mA, V_{GND} = 10V	−14.5		−14.5		−14.5			V
Output Leakage Current (I_L)	V_{IN} = .8V, V_{OUT} = 10V, V_{CC} = 15.5V, V^- = −15V, V_{GND} = 10V		5.0		5.0		5.0	±1.0	μA
Logical "1" Input Voltage (Note 3) (V_{IH})	V_{CC} = 4.5V	2.0		2.0		2.0			V
Logical "0" Input Voltage (Note 3) (V_{IL})	V_{CC} = 4.5V		0.8		0.8		0.8		V
Logical "0" Output Voltage (Note 3) (V_{OL})	V_{CC} = 4.5V, I_{OUT} = 50 mA	V^- + .5		V^- + .5		V^- + .5			V
Transition Time (Note 4) (t_t)	V_{CC} = 5V, V_{OUT} = 0V, R_L = 510Ω		25						ns
	V_{CC} = 5V, R_L = 510Ω		60						ns

Notes:

1. Class S only.
2. V_{CC} = 5.5V, V^- = −25V, except as otherwise specified.
3. Tested go-no-go only.
4. Guaranteed parameter, no testing available.

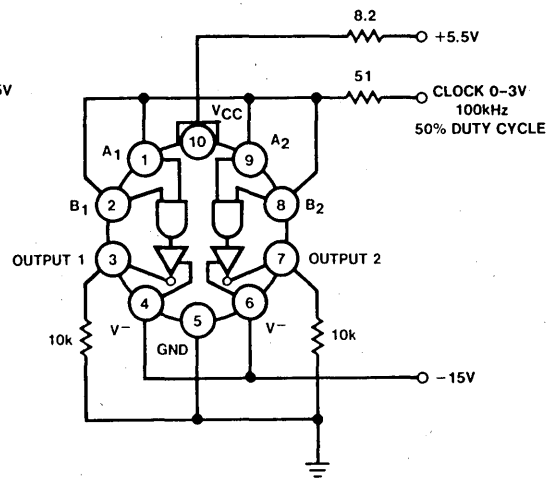
Burn-In Circuits

Dual-In-Line Package (9860HR)



Top View

Metal Can Package (8550HR)



Top View

DH0035 PIN Diode Switch Driver

Absolute Maximum Ratings

V^- Supply Voltage Differential (Pin 5 to Pin 1 or 2)	40V
V^+ Supply Voltage Differential (Pin 1 or 2 to Pin 8 or 9)	30V
Input Current (Pin 3 or 7)	±75mA
Peak Output Current	±1.0 Amps
Power Dissipation (Note 1)	1.5W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The DH0035 is a high speed digital driver designed to drive PIN diodes in RF modulators and switches. The device is used in conjunction with an input buffer such as the DM7830 or DM5440.

The DH0035 is capable of driving a variety of PIN diode types including parallel, serial, anode grounded and cathode grounded. For additional information, see AN-49 PIN Diode Drivers.

Features

- Large output voltage swing 30V
- Peak output current in excess of 1 Amp
- Inputs TTL/DTL compatible
- Short propagation delay 10ns
- High repetition rate 5MHz

RETS0035G, Rev 1B (Teradyne W-301)

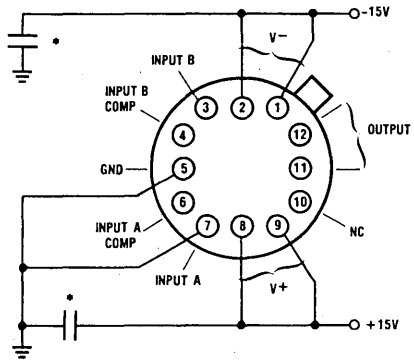
Parameter	Conditions (Note 2)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Logical "1" Input Voltage (Note 3) (V_{IH})	V_{OUT} = −8V, R_L = 100Ω	2.0		2.0		2.0			V
Logical "0" Input Voltage (Note 3) (V_{IL})	V_{OUT} = +8V, R_L = 100Ω		0.4		0.4		0.4		V
Logical "1" Output Voltage (V_{OH})	I_{OUT} = −100mA	7.0		7.0		7.0			V
Logical "0" Output Voltage (V_{OL})	I_{OUT} = 100mA		−7.0		−7.0		−7.0		V
Positive Short Circuit Current (Note 4) (I_{OS+})	V_{IN} = 0, R_L = 0, duty cycle ≤ 3%	400		400		400			mA
Negative Short Circuit Current (Note 4) (I_{OS-})	V_{IN} = 1.5V, I_{IN} = 50mA, R_L = 0, duty cycle ≤ 3%	−800		−800		−800			mA
Turn-On Delay (Note 4) (t_{ON})	V_{IN} = 1.5V, V_{OUT} = −3V		15		15		15		ns
Turn-Off Delay (Note 4) (t_{OFF})	V_{IN} = 1.5V, V_{OUT} = +3V		30		30		30		ns
ON Supply Current ($I_{CC}ON$) (Note 5)	V_{IN} = 1.5V, V_3 = .4V, I_{OUT} = 0	−60		−60		−60			mA

Notes:

1. Derate linearly at 10mW/°C for ambient temperatures above 25°C.
2. V^+ = 10V, V^- = −10V, Pin 5 grounded unless otherwise specified.
3. Tested go-no-go only.
4. Guaranteed parameter, no testing available.
5. Tested on negative supply to guarantee 60μA maximum limit.

Burn-In Circuit

Metal Can (TO-8) Package
(8659HR)



Top View

Note: * All capacitors are .1μF every five sockets.

LH0002 Current Amplifier

Absolute Maximum Ratings

Supply Voltage	±22V
Power Dissipation Ambient	600mW
Input Voltage (Equal to Power Supply Voltage)	
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Steady State Output Current	±100mA
Pulsed Output Current (50ms On/1 sec Off)	±400mA

General Description

The LH0002 is a general purpose thick film hybrid current amplifier that is built on a single substrate.

Features

- High input impedance 180kΩ
- Low output impedance 10Ω
- High power efficiency
- Low harmonic distortion
- DC to 30MHz bandwidth
- Output voltage swing that approaches supply voltage
- 400mA pulsed output current
- Slew rate is typically 200V/μs
- Operation from ±5V to ±20V

These features make it ideal to integrate with an operational amplifier inside a closed loop configuration to increase current output. The symmetrical output portion of the circuit also provides a low output impedance for both the positive and negative slopes of output pulses.

The LH0002 is available in an 8-lead low-profile TO-5 header.

Applications

- Line drive
- 30MHz buffer
- High speed D/A conversion
- Instrumentation buffer
- Precision current source

RETS0002X, Rev 2B (Teradyne J-273)

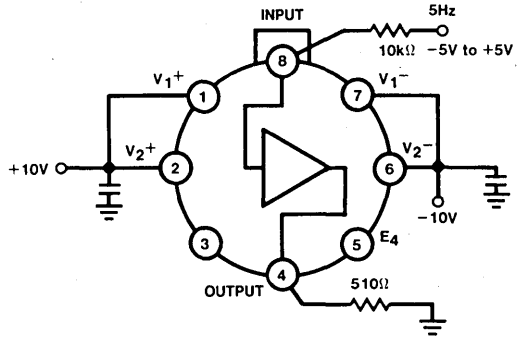
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Voltage Gain (A_V)	V_{IN} = ±10V	0.95		0.95		0.95			
Input Resistance (R_{IN})	R_S = 200kΩ, V_{IN} = ±1V	180		180		180			kΩ
Output Resistance (R_{OUT})	R_L = 50Ω, V_{IN} = 1V		10		10		10		Ω
Output Voltage Swing (V_{OUT})	V_{IN} = ±12V	±10		±10		±10			V
	V_{CC} = ±15V, V_{IN} = ±10V, R_L = 100Ω, R_S = 50Ω	±9.5							V
DC Output Offset Voltage (V_{OO})	R_S = 300Ω		±30		±30		±30		mV
DC Input Offset Voltage (Note 2) (V_{IO})			±100		±100		±100		mV
DC Input Offset Current (I_{IO})			±10		±10		±10		μA
Positive Supply Current (I_{CC}+)			10		10		10		mA
Negative Supply Current (I_{CC}−)			−10		−10		−10		mA
Output Leakage Current (Note 2) (I_L)			±10		±10		±10		μA
Harmonic Distortion (Note 2)	V_{IN} = 5.0V_{RMS}, f = 1kHz		0.5						%
Bandwidth (Note 2) (B_W)	V_{IN} = 1.0V_{RMS}, R_L = 50Ω, f = 1MHz	30							MHz
Rise time (Note 2) (t_r)	R_L = 50Ω, ΔV_{IN} = 100mV, R_S = 50Ω		12						ns
AC Voltage Gain (A_V) (Note 2)	V_{IN} = 3$V_{p\text{-}p}$, f = 1kHz	0.95		0.95		0.95			
AC Input Resistance (R_{IN}) (Note 2)	R_S = 200kΩ, V_{IN} = 1V_{RMS}, f = 1kHz	180		180		180			kΩ
AC Output Resistance (R_{OUT}) (Note 2)	R_L = 50Ω, V_{IN} = 1V_{RMS}, f = 1kHz		10		10		10		Ω
AC Output Voltage Swing (V_{OUT}) (Note 2)	R_S = 50Ω, f = 1kHz	±10		±10		±10			V

Notes:

1. $V_1^+ = V_2^+ = 12V$, $V_1^- = V_2^- = -12V$, R_S = 10kΩ, R_L = 1kΩ, unless otherwise specified.
2. Guaranteed parameter, no testing available.

Burn-In Circuit

Metal Can Package



Top View

LH0003 Wide Bandwidth Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation	See curve
Differential Input Voltage	±7V
Input Voltage	Equal to supply
Load Curent	120mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0003 is a general purpose operational amplifier which features: slewing rate up to 70 volts/μsec, a gain bandwidth of up to 30MHz, and high output currents.

Features

- Very low offset voltage — typically 0.4mV
- Large output swing — > ±10V into 100Ω load
- High CMRR — typically > 90dB
- Good large signal frequency response: 50kHz to 400kHz depending on compensation

Typical Compensation

Circuit Gain	C_1 pF	C_2 pF	Slew Rate $R_L > 200\Omega$ V/μs	Full Output Frequency $R_L > 200\Omega$ V_{OUT}, ±10V
≥40	0	0	70	400
≥10	5	30	30	350
≥5	15	30	15	250kHz
≥2	50	50	5	100
≥1	90	90	2	50

RETS0003X, Rev 3A (Teradyne W-301)

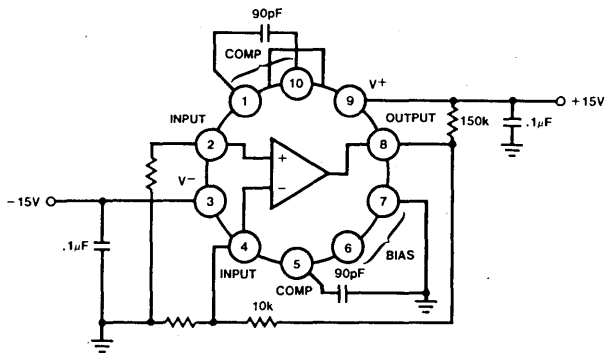
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 3) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 100Ω		3.0		3.0		3.0	±1.0	mV
Input Offset Current (I_{IO})			200		200		200	±20	nA
Input Bias Current (I_{IB})			2.0		2.0		2.0	±0.4	μA
Supply Current (I_{CC})	V_{CC} = ±20V		3.0		3.0		3.0		mA
Voltage Gain (A_V)	R_L = 100kΩ, V_{OUT} = ±10V	20		20		20			V/mV
	R_L = 2kΩ, V_{OUT} = ±10V	15		15		15			V/mV
Output Voltage Swing (V_{OUT})	R_L = 100Ω	±10		±10		±10			V
Common Mode Rejection Ratio (CM_{RR})	−10V ≤ V_{CM} ≤ +10V	70		70		70			dB
Power Supply Rejection Ratio (SV_{RR})	±10V ≤ V_{CC} ≤ ±20V	70		70		70			dB
Input Resistance (Note 2) (R_{IN})		60		75		45			kΩ

Notes:

1. V_{CC} = ±15V unless otherwise specified.
2. Tested go-no-go only.
3. Class S only.

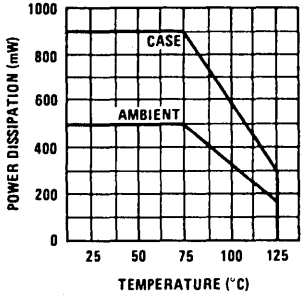
Burn-In Circuit

Metal Can Package
(9694HR)



Top View

Maximum Power Dissipation



LH0004 High Voltage Operational Amplifier

Absolute Maximum Ratings

Supply Voltage, Continuous	±45V
Power Dissipation (See Curve)	400mW
Differential Input Voltage	±7V
Input Voltage	Equal to supply
Short Circuit Duration	3 sec
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0004 is a general purpose operational amplifier designed to operate from supply voltages up to ±40V. The device dissipates extremely low quiescent power, typically 8mW at 25°C and V_{CC} = ±40V.

Features

- Capable of operation over the range of ±5V to ±40V
- Large output voltage typically ±35V
- Low input offset current typically 20nA
- Low input offset voltage typically 0.3mV
- Frequency compensation with 2 small capacitors
- Low power consumption 8mW at ±40V

The LH0004's high gain and wide range of operating voltages make it ideal for applications requiring large output swing and low power dissipation.

The LH0004 is specified for operation over the −55°C to +125°C military temperature range.

Applications

- Precision high voltage power supply
- Resolver excitation
- Wideband high voltage amplifier
- Transducer power supply

RETS0004X, Rev 1B (Teradyne W-301)

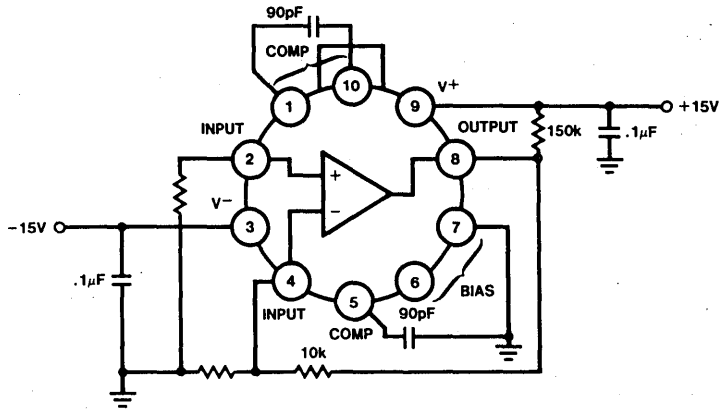
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 4) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 5kΩ		1.0		2.0		2.0	±0.5	mV
Input Offset Current (I_{IO})			20		100		100	±5	nA
Input Bias Current (I_{IB})			100		300		300	±20	nA
Large Signal Gain (A_V)	V_{OUT} = ±30V, R_L = 100kΩ	30		10		10			V/mV
Positive Supply Current (I_{CC}+)			150		175		175		μA
Supply Voltage Rejection Ratio (SV_{RR})	R_S = 5kΩ, ±20V ≤ V_{CC} ≤ ±40V	70		70		70			dB
Common Mode Rejection Ratio (CM_{RR})	R_S = 5kΩ, −33V ≤ V_{CM} ≤ 33V	70		70		70			dB
Negative Supply Current (I_{CC}−)			100		135		135		μA
Output Voltage Swing (V_{OUT})	R_L = 10kΩ	±30		±30		±30			V
Input Resistance (Note 3) (R_{IN})		0.5							MΩ
Input Voltage Range (Note 2) (V_{IN})		±10		±10		±10			V
Temperature Coefficient of Input Offset Voltage (Note 3) ($\Delta V_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C		10						μV/°C
Temperature Coefficient of Input Bias Current (Note 3) ($\Delta_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C		2						nA/°C
Input Noise Voltage (Note 3) (V_N)	R_S = 1kΩ, 5Hz ≤ f ≤ 1000Hz		10						μV_{RMS}
Short Circuit Current (Note 3) (I_{OS})		−50	+50						mA
Output Voltage Swing (Note 3) (V_{OUT})	R_L = 4kΩ	±34		±34					V

Notes:

1. V_{CC} = ±40V unless otherwise noted.
2. Tested go-no-go only.
3. Guaranteed parameter.
4. Class S only.

Burn-In Circuit

Metal Can Package
(9694HR)

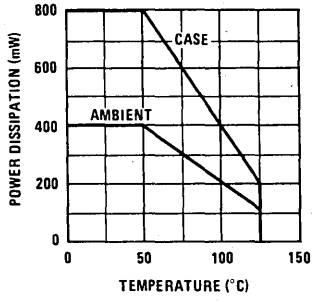


Top View

Note:

Pin 7 must be grounded or connected to a voltage at least 5 volts more negative than the positive supply (Pin 9). Pin 7 may be connected to the negative supply; however, the standby current will be increased. A resistor may be inserted in series with Pin 7 to Pin 9. The value of the resistor should be a maximum of 100kΩ per volt of potential between Pin 3 and Pin 9.

Package Power Dissipation



LH0005A Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (See curve)	400mW
Differential Input Voltage	±15V
Input Voltage	Equal to supply voltages
Peak Load Current	±100mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0005A is a hybrid integrated circuit operational amplifier employing thick film resistors and discrete silicon semiconductors in its design. The select matching of the input pairs of transistors results in low input bias currents and a very low input offset current, both of which exhibit excellent temperature tracking.

Features

- Very high output current capability: ±50mA into a 100 ohm load
- Low standby power dissipation: typically 60mW at ±12V
- High input resistance: typically 2M at 25°C
- Full operating range: −55°C to +125°C
- Good high frequency response: unity gain at 30MHz

With no external roll-off network, the amplifier is stable with a feedback ratio of 10 or greater. By adding a 200pF capacitor between pins 9 and 10, and a 200 ohm resistor in series with a 75pF capacitor from pin 4 to ground, the amplifier is stable to unity gain. The unity gain loop phase margin with the above compensation is typically 70 degrees. With a gain of 10 and no compensation the loop phase margin is typically 50 degrees.

RETS0005AX, Rev A (Teradyne W-301)

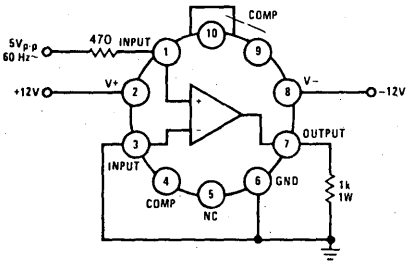
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 0		3.0		4.0		4.0	±1.0	mV
Input Offset Current (I_{IO})	R_S = 50kΩ		5.0		5.0		25		nA
Input Bias Current (I_{IB})	R_S = 10kΩ		25		25		125	±5.0	nA
Positive Supply Current (Note 2) (I_{CC}+)	R_S = 0	2.0	5.0		5.0		5.0		mA
Negative Supply Current (Note 2) (I_{CC}−)	R_S = 0	−1.0	−4.0		−4.0		−4.0		mA
Supply Voltage Rejection Ratio (Note 2) (SV_{RR})	R_S = 0, ±8V ≤ V_{CC} ≤ ±12V	60							dB
Common Mode Rejection Ratio (CM_{RR})	R_S = 0, ±7V ≤ V_{CC} ≤ ±17V, −4V ≤ V_{CM} ≤ 4V	60							dB
Large Signal Gain (A_V)	R_L = 100kΩ, 0 ≤ V_{CM} ≤ ±5V	4		3		3			V/mV
Output Voltage Swing (V_{OUT})	R_L = 100Ω, V_{CM} = ±11.5V	±5		±5		±4			V
	R_L = 10kΩ, V_{CM} = ±11.5V	−10	+6	−10	+6	−10	+6		V
Input Resistance (Note 3) (R_{IN})		1.0							MΩ
Common Mode Rejection Ratio (Note 4) (CM_{RR})				60		60			dB
Supply Voltage Rejection Ratio (Note 4) (SV_{RR})				60		60			dB

Notes:

1. V_{CC} = ±12V unless otherwise specified.
2. These tests guarantee the supply current curve shown below.
3. Tested go-no-go only.
4. Guaranteed parameter, no testing available.

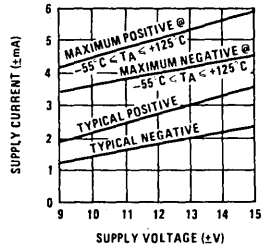
Burn-In Circuit

Metal Can Package
(8447HR)

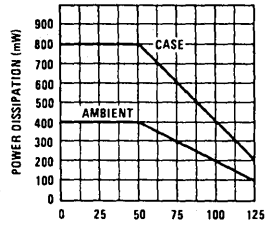


Top View

Supply Current



Maximum Power Dissipation



LH0020 High Gain Instrumentation Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	±22V
Power Dissipation	1.5W
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Output Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0020 is a general purpose operational amplifier designed to source and sink 50mA output currents. In addition to its high output capability, the LH0020 exhibits excellent open loop gain, typically in excess of 100dB. The parameters of the LH0020 are guaranteed over the temperature range of −55°C to +125°C and ± 15V ≤ V_{CC} ≤ ± 22V.

Features

- Low offset voltage typically 1.0mV at 25°C over the entire common mode voltage range
- Low offset current typically 10nA at 25°C
- Offset voltage is adjustable to zero with a single potentiometer
- ± 14V, 50mA output capability

Output current capability, excellent input characteristics, and large open loop gain make the LH0020 suitable for application in a wide variety of applications from precision dc power supplies to precision medium power comparator.

RETS0020G, Rev 0A (Teradyne W-301)

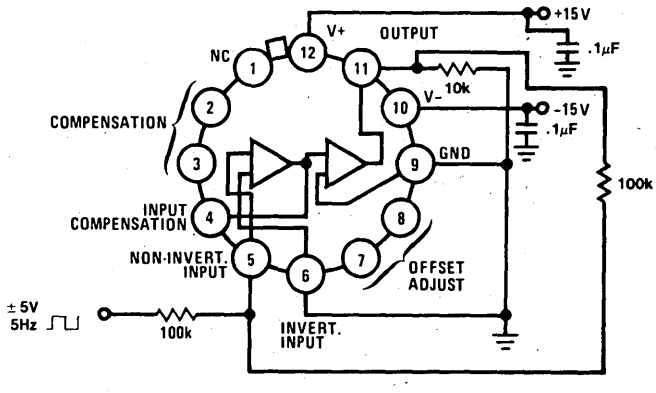
Parameter	Conditions (Note 2)	+25°C Min	+25°C Max	(Note 3) +125°C Min	(Note 3) +125°C Max	(Note 3) −55°C Min	(Note 3) −55°C Max	(Note 6) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 10kΩ		2.5		4.0		4.0	±1.0	mV
Input Offset Current (I_{IO})			50		100		100	±10	nA
Input Bias Current (I_{IB})			250		500		500	±50	nA
Large Signal Voltage Gain (A_V)	R_L = 1kΩ, V_{OUT} = ±10V	100		50		50			V/mV
Power Supply Rejection Ratio (SV_{RR})	±5V ≤ V_{CC} ≤ ±15V	90		90		90			dB
Common Mode Rejection Ratio (CM_{RR})	−5 ≤ V_{CM} ≤ +5V	90		90		90			dB
Short Circuit Current (I_{OS})	R_L = 0		±130						mA
Output Voltage Swing (V_{OUT})	R_L = 300Ω	14.2		14.0		14.0			V
Supply Current (I_{CC})			5.0						mA
Input Resistance (Note 4) (R_{IN})		0.6							MΩ
Input Voltage Range (Note 5) (V_{IN})		±12		±12		±12			V

Notes:

1. For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
2. V_{CC} = ± 15V unless otherwise specified.
3. Temperature limits are guaranteed through 25°C testing.
4. Tested go-no-go only.
5. Guaranteed parameter, no testing available.
6. Class S only.

Burn-In Circuit

Metal Can Package
(8529HR)



Top View

LH0021 1.0 Amp Power Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation	See curves
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Peak Output Current (Note 2)	2.0 Amps
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0021 is a general purpose operational amplifier capable of delivering large output currents not usually associated with conventional IC Op Amps. The LH0021 will provide output currents in excess of one ampere at voltage levels of ±12V. In addition, both the inputs and outputs are protected against overload. The devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

Features

- Output current 1.0 Amp
- Output voltage swing ±12V into 10Ω
- Wide full power bandwidth 15kHz
- Low standby power 100mW at ±15V
- Low input offset voltage and current 3mV and 100nA
- High slew rate 1.5V/μs
- High open loop gain 100V/mV

The excellent input characteristics and high output capability of the LH0021 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies

The LH0021 is supplied in a 8-pin TO-3 package rated at 20 watts with suitable heat sink.

RETS0021K, Rev 0D (Teradyne J-273A)

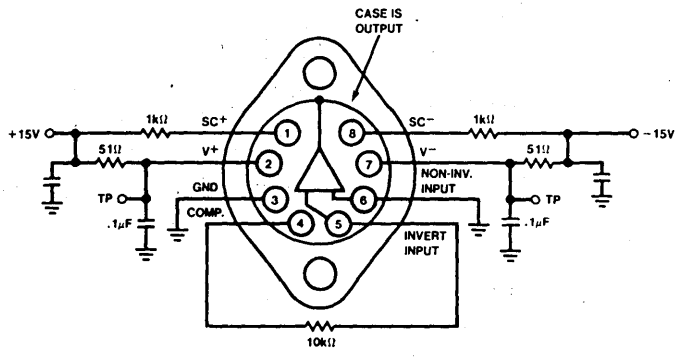
Parameter	Conditions (Note 4)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 7) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})			3.0		5.0		5.0	±1.0	mV
Input Offset Current (I_{IO})			100		300		300	±20	nA
Input Bias Current (I_{IB})			300		1000		1000	±50	nA
Voltage Gain (A_V)	R_L = 1kΩ, V_{OUT} = ±10V	100							V/mV
	R_L = 100Ω, V_{OUT} = ±10V	25		25		25			V/mV
Supply Current (I_{CC})	V_{OUT} = 0		3.5		3.5		3.5		mA
Power Supply Rejection Ratio (SV_{RR})	±5V ≤ V_{CC} ≤ ±15V	80		80		80			dB
Short Circuit Current (I_{OS})	R_{SC} = 0.5Ω	±800	±1600						mA
Output Voltage Swing (V_{OUT})	R_L = 100Ω	±13.5		±13.5		±13.5			V
Input Resistance (Note 6) (R_{IN})		0.3							MΩ
Power Consumption (Note 6) (P_D)			105		105		105		mW
Input Voltage Range (Note 5) (V_{IN})		±12		±12		±12			V
Slew Rate (Note 6) (s_r)	A_V = +1, R_L = 100Ω, C_C = 3000pF	1.5							V/μs
Common Mode Rejection Ratio (CM_{RR})	−10V ≤ V_{CM} ≤ +10V	70		70		70			dB
Temperature Coefficient of Input Offset Voltage (Note 6) ($\Delta V_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C		25						μV/°C
Change of Input Offset Voltage with Change in Output Power (Note 6) ($\Delta V_{IO}/\Delta V_{OUT}$)			15						μV/W
Temperature Coefficient of Input Offset Current (Note 6) ($\Delta I_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C		1.0						nA/°C
Output Voltage Swing (V_{OUT})	R_L = 10Ω	±11							V
Small Signal Transient Response (Note 6) (t_{resp})	C_C = 3000pF		1.0						μs
Small Signal Overshoot (Note 6) (os)	C_C = 3000pF		20						%

Notes:

1. Rating applies for supply voltages above ±15V. For supplies less than ±15V, rating is equal to supply voltage.
2. Rating applies for LH0041G and LH0021K with R_{SC} = 0.
3. Rating applies as long as package power rating is not exceeded.
4. V_{CC} = ±15V, R_S = 100Ω, C_C = 3000pF, R_{SC} = 0Ω, unless otherwise specified.
5. Tested go-no-go only.
6. Guaranteed parameter.
7. Class S only.

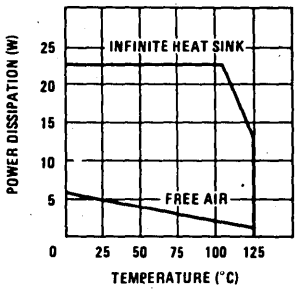
Burn-In Circuit

Metal Can (TO-3) Package (9312HR)



Top View

Power Dissipation



LH0022 High Performance FET Op Amp

Absolute Maximum Ratings

Supply Voltage	±22V
Power Dissipation	See graph
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V^-	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0022 is an FET input operational amplifier with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. This device is internally compensated and is free of latch-up and unusual oscillation problems. The device may be offset nulled with a single 10k trimpot with negligible effect in CMRR.

Features

- Low input offset voltage — 100 microvolts typ.
- High open loop gain — 100dB typ.
- Excellent slew rate — 3.0V/μs typ.
- Internal 6dB/octave frequency compensation
- Pin compatible with standard IC Op Amps (TO-5 package)

The LH0022 is intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets.

The LH0022 provides low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high output impedance buffers.

RETS0022X, Rev E (Teradyne W-301)

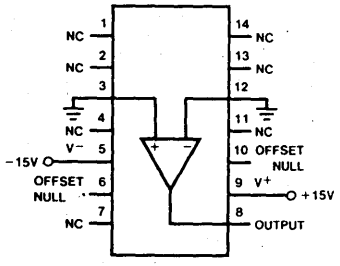
Parameter	Conditions (Note 3)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 100kΩ		4.0		5.0		5.0		mV
Input Offset Current (I_{IO}) (Note 8)			2.0		2000		2000		pA
Input Bias Current (I_{IB}) (Note 8)			0.05		10		10		nA
Supply Current (I_{CC})			2.5		2.5		2.5		mA
Power Supply Rejection Ratio (SV_{RR})	R_S = 10kΩ, ±5V ≤ V_{CC} ≤ ±15V	80		80		80			dB
Common Mode Rejection Ratio (CM_{RR})	R_S = 10kΩ, V_{IN} = ±10V	80		80		80			dB
Large Signal Voltage Gain (A_V)	R_L = 2kΩ, 0 ≤ V_{OUT} ≤ ±10V	100		50		50			V/mV
Output Voltage Swing (Note 4) (V_{OUT})		±10		±10		±10			V
Output Short Circuit Current (I_{OS})			±50		±50		±50		mA
Input Voltage Range (Note 6) (V_{IN})		±12		±12		±12			V
Output Current Swing (Note 6) (I_{OUT})	V_{OUT} = ±10V	±10		±5		±5			mA
Power Dissipation (Note 6) (P_D)			75		75		75		mW
Input Resistance (Note 6) (R_{IN})		10^{10}							Ω
Slew Rate (Note 7) (s_r)		1.5							V/μs
Rise Time (Note 7) (t_r)			1.5						μs
Overshoot (Note 7) (os)			30						%
Temperature Coefficient of Input Offset Voltage (Note 7) ($\Delta V_{IO}/\Delta T$)			10						μV/°C
Temperature Coefficient of Input Offset Current (Note 7) ($\Delta I_{IO}/\Delta T$)		Doubles every 10 degrees Centigrade							
Temperature Coefficient of Input Bias Current (Note 7) ($\Delta I_{IB}/\Delta T$)		Doubles every 10 degrees Centigrade							

Notes:

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies for minimum source resistance of 10kΩ; for source resistances less than 10kΩ, maximum differential input voltage is ±5V.
3. V_{CC} = ±15V unless otherwise specified.
4. R_L = 1kΩ at 25°C; R_L = 2kΩ at 125°C and −55°C.
5. The temperature coefficient of these parameters makes testing of them at −55°C both impractical and irrelevant.
6. Tested go-no-go only.
7. Guaranteed parameter.
8. Tested only functionally at 25°C, guarantee by testing at 125°C.

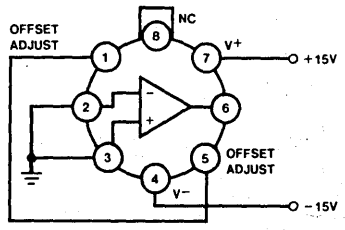
Burn-In Circuits

Dual-In-Line Package (8713HR)



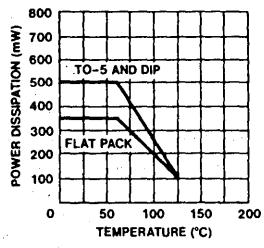
Top View

Metal Can Package (8336HR)



Top View

Maximum Power Dissipation



LH0023G Sample and Hold Circuit

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	±20V
Logic Supply Voltage (V_{CC})	+7.0V
Logic Input Voltage (V_6)	+5.5V
Analog Input Voltage (V_5)	±15V
Power Dissipation	See graph
Output Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0023 is a complete sample and hold circuit including input buffer amplifier, FET output amplifier, analog signal sampling gate, TTL compatible logic circuitry and level shifting. It is designed to operate from standard ±15V DC supplies, but provision is made on the LH0023/LH0023C for connection of a separate +5V logic supply in minimum noise applications. The principal difference between the LH0023 and the LH0043 is a 10:1 trade-off in performance on sample accuracy vs sample acquisition time. Devices are pin compatible except that TTL logic is inverted between the two types.

The LH0023 is ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup. It offers significant cost and size reduction over equivalent module or discrete designs.

Features

- Sample accuracy 0.1% max
- Hold drift rate 0.5mV/sec typ
- Sample acquisition time 100μs max for 20V
- Aperture time 150ns typ
- Wide analog range ±10V min
- Logic input TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

RETS0023G, Rev 0A (Teradyne W-301)

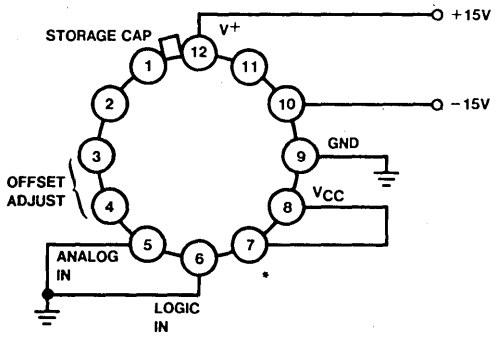
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 4) Δ Limit (25°C)	Units
Sample (Logic "1") Input Current (I_{IH})	V_{IN} = 2.4V, V_{CC} = 5.5V		5.0		5.0		5.0	±1.0	μA
Hold (Logic "0") Input Current (I_{IL})	V_{IN} = 0.4V, V_{CC} = 5.5V		500		500		500	±50	μA
Negative Supply Current (I^-)	V_5 = 0, V_6 = 2.0V, V_{11} = 0		6.0		6.0		6.0		mA
Positive Supply Current (I^+)	V_5 = 0, V_6 = 0.4V, V_{11} = 0		6.0		6.0		6.0		mA
V_{CC} Supply Current (I_{CC})	V_5 = 0, V_6 = 5.0V		1.6		1.6		1.6		mA
Output Offset Voltage (V_{OO})	R_S = 10kΩ, V_5 = 0, V_6 = 0 (without null)		±20		±20		±20	±4	mV
Sample Accuracy	V_{OUT} = ±10V		.10		.10		.10		mV/V
Hold (Logic "0") DC Input Resistance (R_{INL})		20							kΩ
Sample (Logic "1") Analog Input Current (I_{IH})			1.0		1.0		1.0		μA
Pin 1 Leakage Current (I_{L1})	V_5 = ±10V, V_{11} = ±10V		0.2		1.0		1.0		nA
Sample Acquisition Time (t_{acq}) (Note 2)	V_{IN} = ±10V, C_S = 0.01μF, ΔV_{OUT} = 20V		100		100		100		μs
Sample (Logic "1") Input Voltage (Note 2) (V_{IH})	V_{CC} = 4.5V	2.0		2.0		2.0			V
Hold (Logic "0") Input Voltage (Note 2) (V_{IL})	V_{CC} = 4.5V		0.8		0.8		0.8		V
Analog Input Voltage Range (Note 2) (V_{IN})		±10		±10		±10			V
Analog Output Voltage Range (Note 2) (V_{OUT})	R_L ≥ 1kΩ	±10		±10		±10			V
Sample (Logic "1") DC Input Resistance (Note 2) (R_{INH})		500		500		500			kΩ
Slew Rate (Output Amp) (Note 3) (s_r)		1.5							V/μs
Drift Rate (Note 3) (d_r)	V_{OUT} = ±5V, C_S = 0.01μF		20		250		250		mV/s
Aperture Time (Note 3) (t_{ap})			300		300		300		ns

Notes:

1. V^+ = +15V, V^- = −15V, V_{CC} = 5V unless otherwise specified.
2. Tested go-no-go only.
3. Guaranteed parameter.
4. Class S only.

Burn-In Circuit

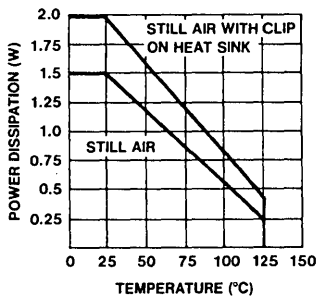
Metal Can Package
(9549HR)



Top View

Note: *Tie for operation with V^+ = 15V only.

Power Dissipation



LH0024 High Slew Rate Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	±18V
Input Voltage	Equal to supply
Differential Input Voltage	±5V
Power Dissipation	600mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0024 is a very wide bandwidth, high slew rate operational amplifier intended to fulfill a wide variety of high speed applications such as buffers to A to D and D to A converters and high speed comparators. The device exhibits useful gain in excess of 50MHz making it possible to use in video applications requiring higher gain accuracy than is usually associated with such amplifiers.

Features

- Very high slew rate — 400V/μs at Av = +1
- Wide small signal bandwidth — 70MHz typ
- Wide large signal bandwidth — 15MHz typ
- High output swing — ±12V into 1K
- Offset null with single pot
- Low input offset — 6mV
- Pin compatible with standard IC op amps

The LH0024 combination of wide bandwidth and high slew rate make it an ideal choice for a variety of high speed applications including active filters, oscillators, and comparators as well as many high speed general purpose applications.

RETS0024H, Rev 0A (Teradyne W-301)

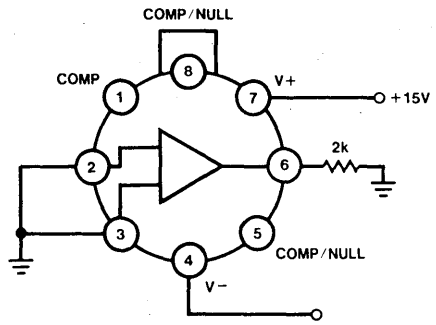
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 4) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 50Ω		4.0		6.0		6.0	±1.0	mV
Input Offset Current (I_{IO})			5.0		10.0		10.0		μA
Input Bias Current (I_{IB})			30		40		40		μA
Power Supply Current (I_{CC})			15		15		15		mA
Large Signal Voltage Gain (A_V)	R_L = 1kΩ	4.0		3.0		3.0			V/mV
Input Voltage Range (Note 2) (V_{IN})		±12		±12		±12			V
Output Voltage (Note 2) (V_{OUT})	R_L = 1kΩ	±12		±10		±10			V
Slew Rate (Note 3) (s_r)	V_{CC} = ±15V, R_L = 1kΩ, C_1 = C_2 = 30pF, Av = +1	400							V/μs
Common Mode Rejection Ratio (Note 3) (CMR_R)	V_S = ±15V, ΔV_{IN} = ±10V, R_S = 50Ω	55		55		55			dB
Power Supply Rejection Ratio (Note 3) (SVR_R)	±5V ≤ V_{CC} ≤ ±18V, R_S = 50Ω	55		55		55			dB

Notes:

1. V_{CC} = ±15V unless otherwise specified.
2. Tested go-no-go only.
3. Guaranteed parameter.
4. Class S only.

Burn-In Circuit

Metal Can Package
(9533HR)



Top View

LH0032 Ultra Fast FET Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	±18V
Input Voltage	$\pm V_S$
Differential Input Voltage	±30V
Power Dissipation	See Curve
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0032 is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers, allowing the use of operational gain setting and frequency response shaping into the megahertz region.

Features

- High slew rate — 350V/μs
- High bandwidth — 70 MHz
- High input impedance — $10^9\Omega$ min
- Low input bias current — 100pA max
- Offset null with single pot
- Low input offset voltage — 5mV max
- No compensation for gains above 50

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D-to-As, buffers in data acquisition systems, and sample and hold circuits. Additional applications include high speed integrators and video amplifiers.

RETS0032G, Rev 2A (Teradyne J-273)

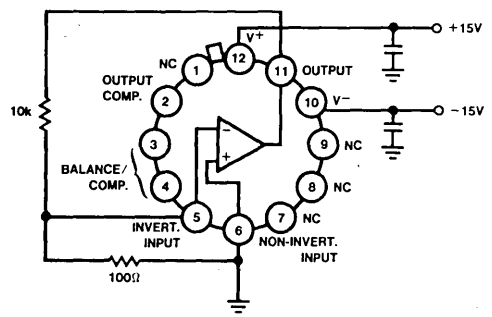
Parameter	Conditions (Note 2)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 6) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 100kΩ		5.0		10.0		10.0	±1.0	mV
Input Offset Current (I_{IO}) (Note 4)	Pulse correlated		.025		25		25		nA
	Measured in still air after 7 minutes (Note 3)		.25						nA
Input Bias Current (I_{IB}) (Note 4)	Pulse correlated		0.1		50		50		nA
	Measured in still air after 7 minutes (Note 3)		1.0						nA
Power Supply Current (I_{CC})	Pulse correlated		23.0						mA
	Measured in still air after 7 minutes (Note 3)		20.0						mA
Large Signal Gain (A_V) (Note 5)	R_L = 1kΩ, V_{OUT} = ±10V	48		45		45			dB
Common Mode Rejection Ratio (CM_{RR})	ΔV_{IN} = ±10V	50		50		50			dB
Supply Voltage Rejection Ratio (SV_{RR})	±5V ≤ V_{CC} ≤ ±20V	50		50		50			dB
Output Voltage Swing (V_{OUT})	R_L = 1kΩ	±10		±10		±10			V
Input Voltage Range (Note 2) (V_{IN})		±10		±10		±10			V
Input Resistance (Note 2) (R_{IN})		10^6							MΩ
Voltage Gain (Note 3) (A_V)	R_L = 1kΩ, V_{OUT} = ±10V, f = 1kHz	60		57		57			dB
Slew Rate (Note 3) (s_r)	A_V = 1, ΔV_{IN} = 20V, R_L = 1kΩ	350							V/μs
Small Signal Rise Time (Note 3) (t_r)	A_V = 1, ΔV_{IN} = 1V, R_L = 1kΩ		20						ns
Small Signal Delay Time (Note 3) (t_d)	A_V = 1, ΔV_{IN} = 1V, R_L = 1kΩ		25						ns
Temperature Coefficient of Input Offset Voltage (Note 3) ($\Delta V_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C		150						μV/°C
Setting Time to 1% of Final Value (Note 3) (t_{set})	A_V = −1, ΔV_{IN} = 20V, R_L = 1kΩ		0.5						μs

Notes:

1. V_{CC} = ±15V unless otherwise specified.
2. Tested go-on-go only.
3. Guaranteed parameter;
4. 25°C Limit guaranteed by 125°C testing.
5. The DC limit as tested correlates to the limit shown for f = 1kHz.
6. Class S only.

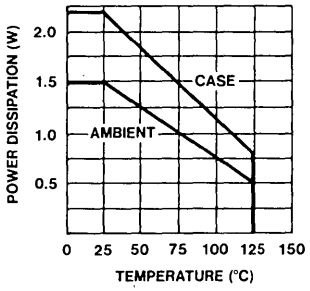
Burn-In Circuit

Metal Can Package



Top View

Maximum Power Dissipation



LH0033 Fast Buffer Amplifier

Absolute Maximum Ratings

Supply Voltage ($V^+ - V^-$)	40V
Maximum Power Dissipation (see Curve)	1.5W
Maximum Junction Temperature	175°C
Input Voltage	Equal to Supplies
Continuous Output Current	±100mA
Peak Output Current	±250mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0033 is a high speed, FET input, voltage follower/buffer designed to provide high current drive at frequencies from DC to over 100MHz.

The LH0033 will provide ±10mA into 1kΩ loads (±100mA peak) at slew rates of 1500V/μs and exhibits excellent phase linearity up to 20MHz.

It is intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffers for driving reactive loads and high impedance input buffers for high speed A-to-Ds and comparators.

Features

- Wide range single or dual supply operation
- Wide power bandwidth — DC to 100MHz
- High output drive — ±10V with 50Ω load
- Low phase non-linearity — 2 degrees
- Fast rise times — 2ns
- High current gain — 120dB
- High input resistance — $10^{10}\Omega$

Advantages

- Only +10V supply needed for $5V_{p-p}$ video out
- Speed does not degrade system performance
- Wide data rate range for phase ecoded systems
- Output drive adequate for most loads
- Single pre-calibrated package

RETS0033G, Rev 2A (Teradyne J-273)

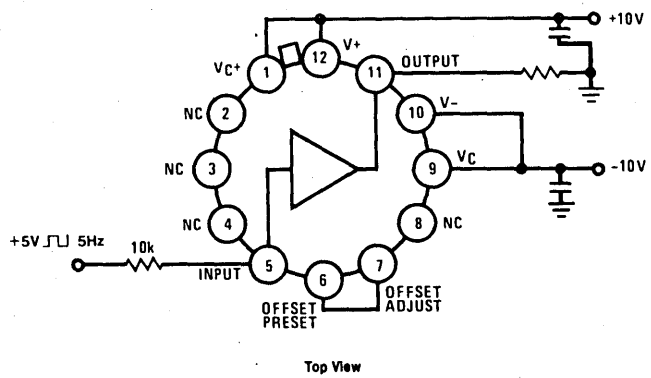
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 5) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 100kΩ		±10		±15		±15	±3.0	mV
Input Bias Current (Note 2) (I_{IB})	R_S = 0		0.25		10		10		nA
	R_S = 0, measured in still air after 7 minutes (note 4) pulse correlated		2.5						nA
Voltage Gain (A_V)	V_{IN} = ±10V, R_L = 1kΩ	0.97		0.97		0.97			V/V
Output Impedance (R_{OUT})	V_{IN} = $1V_{RMS}$, R_L = 1kΩ, ±10μA ≤ I_{OUT} ≤ ±10mA		10		10		10		Ω
Output Voltage Swing (V_{OUT})	R_L = 1kΩ, V_{IN} = ±14V	±12		±12		±12			V
Supply Current (I_{CC})			22.0		22.0		22.0		mA
Input Impedance (Note 3) (R_{IN})		10^{10}		10^{10}		10^{10}			Ω
Slew Rate (Note 4) (S_r)	V_{IN} = ±10V, R_S = 50Ω, R_L = 1kΩ	1000							V/μs
Power Consumption (Note 3) (P_D)	V_{IN} = 0		660		660		660		mW
Temperature Coefficient of Input Offset Voltage (Note 4) ($\Delta V_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C		250						μV/°C
Output Voltage Swing (Note 4) (V_{OUT})	R_L = 100Ω, V_{IN} = ±10V	±9		±9		±9			V
I_{CC} Second Stage Mismatch (ΔI_{CC})	$I_{CC1} - I_{CC2}$		10		10		10		mA

Notes:

1. $V_C^+ = V^+ = +15V$, $V_C^- = V^- = -15V$, R_S = 100kΩ, V_{IN} = 0 unless otherwise noted.
2. 25°C limit is guaranteed by testing at 125°C.
3. Tested go-no-go only.
4. Guaranteed parameter.
5. Class S only.

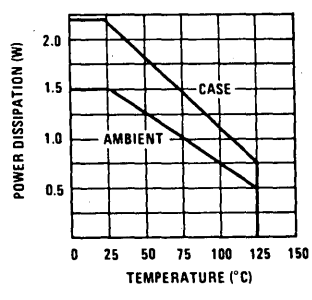
Burn-In Circuit

Metal Can Package,
(8520HR)



Top View

Power Dissipation



Note: Case is electrically isolated.

LH0036 Instrumentation Amplifier

Absolute Maximum Ratings

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range	±VCC
Shield Drive Voltage	±VCC
CMRR Preset Voltage	±VCC
CMRR Trim Voltage	±VCC
Power Dissipation (Note 1)	1.5W
Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0036 is a true micro power instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300MΩ input impedance and excellent 100dB common mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable with one external resistor from 1 to 1000. Power supply operating range is between ±1V and ±18V. Input bias current and output bandwidth are both externally adjustable or can be set by internally set values.

Features

- High input impedance 300MΩ
- High CMRR 100dB
- Single resistor gain adjust 1 to 1000
- Low power 90μW
- Wide supply range ±1V to ±18V
- Adjustable input bias current
- Adjustable output bandwidth
- Guard drive output

RETS0036G, Rev 0B (Teradyne W-301)

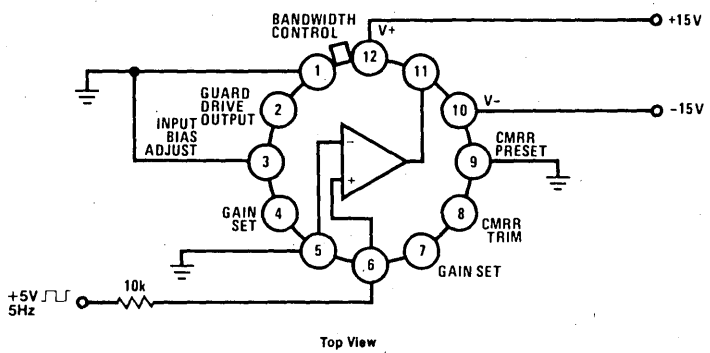
Parameter	Conditions (Note 2)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 5) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 1kΩ, V_{CM} = 0		±1.0		±2.0		±2.0	±0.5	mV
Output Offset Voltage (V_{OO})	R_S = 1kΩ, V_{CM} = 0		±5.0		±6.0		±6.0		mV
Input Offset Current (I_{IO})	V_{CM} = 0		±40		±80		±80	±10	nA
Input Bias Current (I_{IB})	V_{CM} = 0		±100		±150		±150	±20	nA
Voltage Gain Deviation	ΔV_{IN} = 10V		±1.0		±1.0		±1.0		%
	ΔV_{IN} = 0.1V		±1.0		±1.0		±1.0		%
	ΔV_{IN} = 10mV		±1.0		±1.0		±1.0		%
Power Supply Current (I_{CC})			400		400		400		μA
Common Mode Rejection Ratio (CM_{RR})	A_V = 1, −10V ≤ V_{IN} ≤ +10V		±2.5		±2.5		±2.5		mV/V
	A_V = 100, −10V ≤ V_{IN} ≤ +10V		±250		±250		±250		μV/V
Power Supply Rejection Ratio (SV_{RR})	A_V = 1, ±5V ≤ V_{CC} ≤ ±15V		±2.5		±2.5		±2.5		mV/V
	A_V = 100, ±5V ≤ V_{CC} ≤ ±5V		±0.25		±0.25		±0.25		mV/V
Output Voltage Swing (Note 3) (V_{OUT})	R_L = 10kΩ	±10		±10		±10			V
	V_{CC} = ±1.5V, R_L = 100kΩ	±0.6		±0.6		±0.6			V
Input Voltage Range (Note 3) (V_{IN})		±10		±10		±10			V
Common Mode Rejection Ratio (Note 4) (CM_{RR})	A_V = 10, ΔR_S = 1kΩ		0.25		0.25		0.25		mV/V
Guard Drive Output		4.5	5.5	4.5	5.5	4.5	5.5		V
CM_{RR} Trim		4.5	5.5	4.5	5.5	4.5	5.5		V
Supply Voltage Range (V_{CC}) (Note 3)			±18		±18		±18		V

Notes:

1. The maximum junction temperature is 150°C. For operation at elevated temperatures derate the G package on a thermal resistance of 90°C/W above 25°C.
2. V_{CC} = ±15V unless otherwise specified. Temperature limits guaranteed through 25°C testing.
3. Tested go-no-go only.
4. Guaranteed parameter.
5. Class S only.

Burn-In Circuit

Metal Can (TO-8) Package
(9316HR)



Top View

LH0037 Low Cost Instrumentation Amplifier

Absolute Maximum Ratings

Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage Range, Shield Drive Voltage	±V_{CC}
CMRR Preset Voltage, CMRR Trim Voltage	±V_{CC}
Power Dissipation (Note 1)	1.5W
Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0037 is a true instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300MΩ input impedance and excellent 100dB common-mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable with one external resistor from 1 to 1000. Power supply operating range is between ±5V and ±22V.

Features

- High input impedance — 300MΩ
- High CMRR — 100dB
- Single resistor gain adjust — 1 to 1000
- Low power — 250mW
- Wide supply range — ±5V to ±22V
- Guard drive output

RETS0037G, Rev OB (Teradyne W-301)

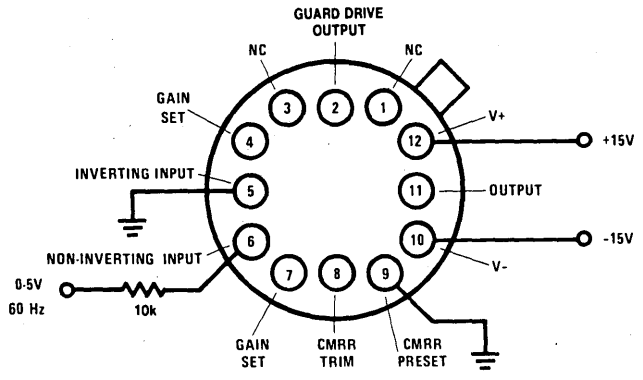
Parameter	Conditions (Note 2)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 4) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 1kΩ		±1.0		±2.0		±2.0	±.5	mW
Input Bias Current (I_{IB})			±0.5		±1.5		±1.5	±.2	μA
Input Offsent Current (I_{IO})			±100		±200		±200		nA
Output Offset Voltage (V_{OO})	R_S = 1kΩ		±5.0		±6.0		±6.0		mV
Supply Current (I_{CC})			8.4		8.4		8.4		mA
Input Voltage Range (Note 3)(V_{IN})	Differential or Common Mode	±12		±12		±12			V
Power Supply Rejection Ratio (SV_{RR})	A_V = 1		±2.5		±2.5		±2.5		mV/V
	A_V = 100, ±5V ≤ V_{CC} ≤ ±15V		±.25		±.25		±.25		mV/V
Common Mode Rejection Ratio (CM_{RR})	ΔR_S = 1k, A_V = 1		±2.5		±2.5		±2.5		mV/V
	ΔR_S = 1k, A_V = 10 (Note 5)		±0.25		±0.25		±0.25		mV/V
	ΔR_S = 1k, A_V = 100		±.10		±.10		±.10		mV/V
Output Voltage (V_{OUT})	R_L = 2kΩ	±10		±10		±10			V
Gain error (E_{AV})	A_{VCL} = 1, A_{VCL} = 100		±1		±1		±1		%
Guard Drive Output		±4.5	±5.5	±4.5	±5.5	±4.5	±5.5		V
CMRR Trim		±4.5	±5.5	±4.5	±5.5	±4.5	±5.5		V
Supply Voltage range (V_{CC}) (Note 3)			±22		±22		±22		V

Notes:

1. The maximum junction temperature is 150°C. For operation at elevated temperatures, derate at 90°C/W.
2. V_{CC} = ±15V, V_g = 0, unless otherwise noted.
3. Tested go-no-go only.
4. Class S only.
5. Guaranteed parameter.

Burn-In Circuit

Metal Can Package



Top View

LH0038 True Instrumentation Amplifier

Absolute Maximum Ratings

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±1V
Input Voltage	±V_{CC}
Power Dissipation (See Curve)	500mW
Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 20 sec)	300°C

General Description

The LH0038 is a precision true instrumentation amplifier (TIA) capable of amplifying very low level signals, such as thermocouple and low impedance strain gauge outputs. Precision thin film gain setting resistors are included in the package to allow the user to set the closed-loop gain from 100 to 2000. Since the resistors are of a homogenous single chip construction, they track almost perfectly so that temperature variations of closed loop gain are virtually eliminated.

LH0038 exhibits excellent CMRR, PSRR, gain linearity, as well as extremely low input offset voltage, offset voltage drift and input noise voltage.

The devices are provided in a hermetically sealed 16-lead DIP.

Features

- Ultralow offset voltage — 25μV typ., 100μV max
- Ultralow offset drift — 0.25 μV/°C max
- Ultralow input noise — 0.2μV p-p
- Pin strap gain options — 100, 200, 400, 500, 1k, 2k
- Excellent PSRR and CMRR — 120 dB

RETS0038D, Rev 1B (Teradyne W-301)

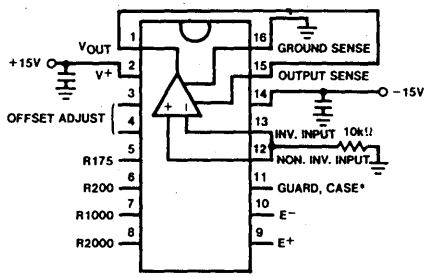
Parameter	Conditions (Note 3)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 2) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 50Ω, V_{CM} = 0		±100		±125		±125		μV
Output Offset Voltage (V_{OO})	R_S = 50Ω, V_{CM} = 0		±10		±15		±15		mV
Input Bias Current (I_{IB})	V_{CM} = 0		±100		±200		±200		nA
Input Offset Current (I_{IO})	V_{CM} = 0		±5		±8		±8		nA
Gain Error (E_{AV})	A_{VCL} = 100		±0.3		±0.3		±0.3		%
	A_{VCL} = 175		±0.3		±0.3		±0.3		%
	A_{VCL} = 200		±0.3		±0.3		±0.3		%
	A_{VCL} = 1000		±0.5		±0.5		±0.5		%
	A_{VCL} = 2000		±2.0		±2.0		±2.0		%
Output Voltage (V_{OUT})	R_L = 10kΩ	10		10		10			V
	R_L = 10kΩ		−10		−10		−10		V
Output Short Circuit Current (I_{OS})		2.0	10.0						mA
		−10	−2						mA
Power Supply Rejection Ratio (SV_{RR})	±5V < V_{CC} < ±15V, A_{CVL} = 100		±20		±20		±20		μV/V
		94		94		94			db
	±5V < V_{CC} < ±15V, A_{VCL} = 1000		±3.2		±3.2		±3.2		μV/V
		114		114		114			db
Common Mode Rejection Ratio (CM_{RR})	−10V < V_{CM} < 10V, A_{VCL} = 100		±20		±20		±20		μV/V
		94		94		94			db
	−10V < V_{CM} < 10V, A_{VCL} = 1000		±2.0		±2.0		±2.0		μV/V
		114		114		114			db
Supply Current (I_{CC})			2.0						mA
Guard Voltage Error (E_{GV})	V_{CM} = 0V, V^+ = +5V, V^- = −25V	−100	100	−100	100	−100	100		mV
	V_{CM} = 0V, V^+ = +25V, V^- = −5V	−100	100	−100	100	−100	100		mV
Guard Offset (V_{GO})	V_{CM} = 0		±0.1		±0.1		±0.1		V
Supply Voltage Range (V_{CC}) (Note 2)		±5	±18	±5	±18	±5	±18		V
Temperature Coefficient of Input Offset Voltage ($\Delta V_{IO}/\Delta T$) (Note 5)	A_{VCL} = 2000, −55°C ≤ T_A ≤ 125°C		±0.25						μV/°C
Common Mode Input Voltage Range (V_{CM}) (Note 4)		±10		±10		±10			V

Notes:

1. The inputs have diode over-voltage protection. Excessive currents will flow for differential voltages in excess of ±1V. Input current should be limited to 10mA.
2. Class S only.
3. V_C = ±15V, unless otherwise specified.
4. Tested go-no-go only.
5. Guaranteed parameter.

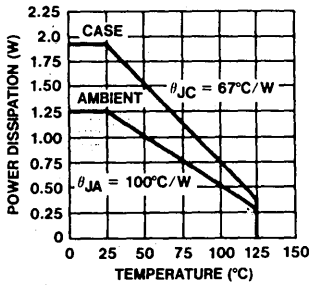
Burn-In Circuit

Dual-In-Line Package (9897HR)



Top View

Power Dissipation



Note: *Guard output is connected to the case.

LH0041 0.2 Amp Power Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	± 18V
Power Dissipation	See Curves
Differential Input Voltage	± 30V
Input Voltage (Note 1)	± 15V
Peak Output Current (Note 2)	0.5A
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0041 is a general purpose operational amplifier capable of delivering large output currents not usually associated with conventional IC Op Amps. The LH0041 delivers currents of 200mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload. The devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

Features

- Output current 0.2A
- Output voltage swing ± 13V into 100Ω
- Wide full power bandwidth 15kHz
- Low standby power 100mW at ± 15V
- Low input offset voltage and current 3mV, 100nA
- High slew rate 1.5V/μs
- High open loop gain 100V/mV

The LH0041 is particularly suited for applications such as torque driver for internal guidance systems, diddle yoke driver for alpha-numeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

RETS0041X, Rev 2A (Teradyne J-273A)

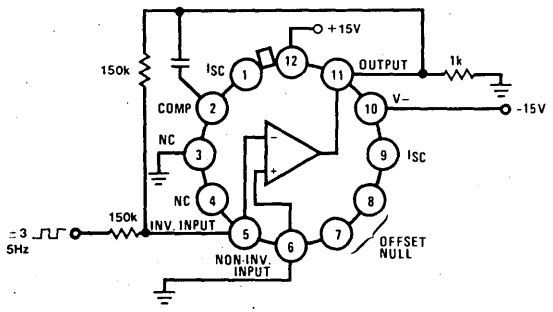
Parameter	Conditions (Note 4)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 7) J Limit (25°C)	Units
Input Offset Voltage (V_{IO})			3.0		5.0		5.0	± 1.0	mV
Input Offset Current (I_{IO})			100		300		300	± 20	nA
Input Bias Current (I_{IB})			300		1000		1000	± 50	nA
Voltage Gain (A_V)	R_L = 1kΩ, R_S = 0Ω, V_{OUT} = ± 10V	100							V/mV
	R_L = 100Ω, R_S = 0Ω, V_{OUT} = ± 10V	25		25		25			V/mV
Supply Current (I_{CC})	R_S = 0Ω, V_{OUT} = 0V		3.5		3.5		3.5		mA
Power Supply Rejection Ratio (SV_{RR})	± 5 ≤ V_{CC} ≤ ± 15V	80		80		80			dB
Common Mode Rejection Ratio (CM_{RR})	−10V ≤ V_{CM} ≤ +10V	70		70		70			dB
Output Voltage Swing (V_{OUT})	R_L = 100Ω	± 13.0		± 13.0		± 13.0			V
Short Circuit Current (I_{OS})	R_{SC} = 3.3Ω		± 300						mA
Input Resistance (Note 6) (R_{IN})		0.3							MΩ
Input Voltage Range (Note 6) (V_{IN})		± 12		± 12		± 12			V
Power Consumption (Note 6) (P_D)			105		105		105		mW
Slew Rate (Note 6) (s_r)	A_V = +1, R_L = 100Ω, C_C = 3000pF	1.5							V/μs
Temperature Coefficient of Input Offset Current (Note 6) ($\Delta I_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C		1.0						nA/°C
Small Signal Transient Response (Note 6) (t_{resp})	C_C = 3000pF		1.0						μs
Small Signal Overshoot (Note 6) (os)	C_C = 3000pF		20						%

Notes:

1. Rating applies for supply voltages above ± 15V. For supplies less than ± 15V, rating is equal to supply voltage.
2. Rating applies with R_{SC} = 0.
3. Rating applies as long as package power rating is not exceeded.
4. V_{CC} = ± 15V, R_S = 100Ω, C_C = 100pF unless otherwise specified.
5. Tested go-no-go only.
6. Guaranteed parameter.
7. Class S only.

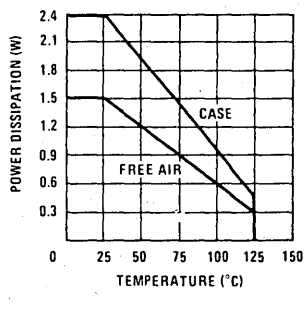
Burn-In Circuit

Metal Can Package (8666HR)



Top View

Power Dissipation



LH0042 Low Cost FET Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	±22V
Power Dissipation (see Curve)	500mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V^-	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0042 is a FET input operational amplifier with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate.

Features

- Low input offset current
- Low input offset drift
- Low input offset voltage 100μV typ.
- High open loop gain 100dB typ.
- Excellent slew rate 3.0V/μs typ.
- Internal 6dB/octave frequency compensation
- Pin compatible with standard IC op amps

The LH0042 is intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0042 provides low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

Special electrical parameter selection and custom built circuits are available on special request.

RETS0042X, Rev A (Teradyne W-301)

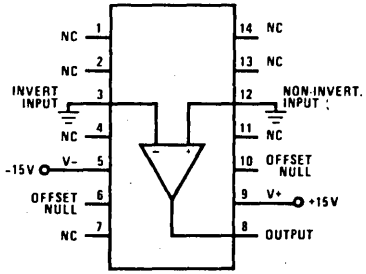
Parameter	Conditions (Note 3)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 100kΩ		20		20		20		mV
Input Offset Current (Note 6) (I_{IO})			5.0		5000		5000		pA
Input Bias Current (Note 6) (I_{IB})			.025		50		50		nA
Supply Current (I_{CC})			3.5		3.5		3.5		mA
Power Supply Rejection Ratio (SV_{RR})	R_S = 10kΩ, ±5V ≤ V_{CC} ≤ ±15V	70		70		70			dB
Common Mode Rejection Ratio (CM_{RR})	R_S = 10kΩ, V_{IN} = ±10V	70		70		70			dB
Large Signal Voltage Gain (A_V)	R_L = 1kΩ, V_{OUT} = ±10V	50		50		50			V/mV
Output Voltage Swing (V_{OUT})	R_L = 1kΩ, T_A = 25°C (R_L = 2k, −55°C ≤ T_A ≤ 125°C	±10		±10		±10			V
Output Short Circuit Current (I_{OS})			±50		±50		±50		mA
Input Voltage Range (Note 5) (V_{IN})		±12		±12		±12			V
Output Current Swing (Note 5) (I_{OUT})	V_{OUT} = ±10V	±10		±5		±5			mA
Power Dissipation (Note 5) (P_D)			105		105		105		mW
Slew Rate (Note 4) (s_r)		1.5							V/μs
Rise Time (Note 4) (t_r)			1.5						μs
Overshoot (Note 4) (os)			30						%
Temperature Coefficient of Input Offset Voltage (Note 4) ($\Delta V_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C		30						μV/°C
Temperature Coefficient of Input Offset Current (Note 4) ($\Delta I_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C	Doubles every 10 degrees Centigrade							
Temperature Coefficient of Input Bias Current (Note 4) ($\Delta I_{IB}/\Delta T$)	−55°C ≤ T_A ≤ +125°C	Doubles every 10 degrees Centigrade							

Notes:

1. For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies for minimum source resistance of 10kΩ. For source resistances less than 10kΩ maximum differential input voltage is ±5V.
3. V_{CC} = ±15V unless otherwise specified.
4. Guaranteed parameter.
5. Tested go-no-go only.
6. Guaranteed at 25°C through 125°C testing.

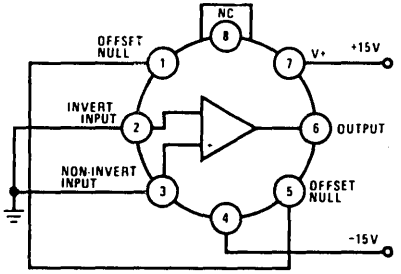
Burn-In Circuits

Dual-In-Line Package (8713HR)



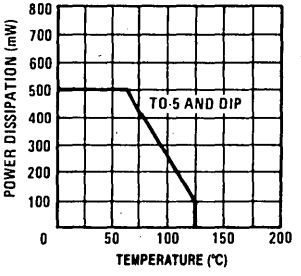
Top View

Header Package (9336HR)



Top View

Maximum Power Dissipation



LH0043 Sample and Hold Circuit

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	±20V
Logic Input Voltage (V_6)	±5.5V
Analog Input Voltage (V_5)	±15V
Power Dissipation	See Graph
Output Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0043 is a complete sample and hold circuit including input buffer amplifier, FET output amplifier, analog signal sampling gate, TTL compatible logic circuitry and level shifting. It is designed to operate from standard ±15VDC supplies. The principal difference between the LH0023 and the LH0043 is a 10:1 trade-off in performance on sample accuracy vs. sample acquisition time. Devices are pin compatible except that TTL logic is inverted between the two types.

The LH0043 is ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup. It offers significant cost and size reduction over equivalent module or discrete designs. Each device is available in a hermetic TO-8 package and is completely specified over both full military and instrument temperature ranges.

Features

- Sample acquisition time — 15μs max for 20V, 4μs typ for 5V
- Aperture time — 20ns typ
- Hold drift rate — 1mV/s typ
- Sample accuracy — 0.1% max
- Wide analog range — ±10V min
- Logic input — TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

RETS0043G, Rev 4B (Teradyne W-301)

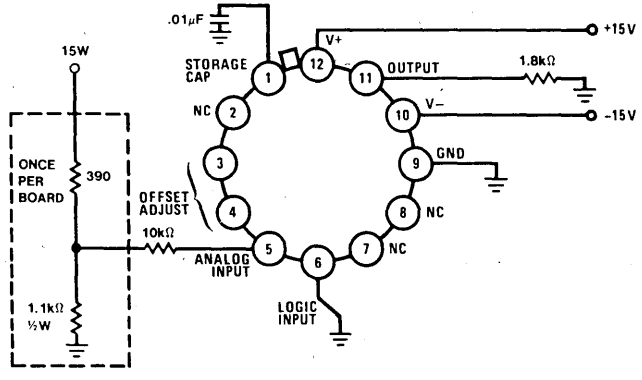
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 4) Δ Limit (25°C)	Units
Sample (Logical "0") Input Current (I_{IL})	V_6 = 0.4V		−1.5		−1.5		−1.5		mA
Hold (Logical "1") Input Current (I_{IH})	V_6 = 2.4V		5.0		5.0		5.0	±1.0	μA
Negative Supply Current (I_{CC}^-)	V_5 = 10V, V_6 = 2V, V_{11} = 0		−22		−22		−22		mA
Positive Supply Current (I_{CC}^+)	V_5 = 10V, V_6 = 0.4V, V_{11} = 0		18		18		18		mA
Output Offset Voltage (V_{OO})	V_5 = V_6 = Ground, R_S = 10kΩ		±40		±40		±40	±8	mV
Sample Accuracy	V_{OUT} = ±10V, R_L = 1kΩ		0.1		0.1		0.1		%
Analog Input Current (I_{IN})	V_6 = 0.8V		5.0		5.0		5.0		nA
Drift Rate (d_r) (Note 3)	V_5 = ±10V, V_6 = 2.4V, C_S = 0.01μF		2.5		2500		2500		mV/s
Output Amplifier Slew Rate (s_r) (Note 3)	V_{OUT} = S_V, C_S = .001μF	1.5		1.5		1.5			V/μs
Hold (Logical "1") Input Voltage (Note 2) (V_{IH})		2.0		2.0		2.0			V
Sample (Logical "0") Input Voltage (Note 2) (V_{IL})			0.8		0.8		0.8		V
Analog Input Voltage Range (Note 2) (V_{IN})		±10		±10		±10			V
DC Input Resistance (Note 2) (R_{IN})		10^{10}							Ω
Analog Voltage Output Range (Note 2) (V_{OUT})	R_L = 1kΩ	±10							V
Pin 1 Leakage Current (Note 3) (I_{L1})	V_{CC} = ±10V, V_{11} = ±10V		.025		25		25		nA
Drift Rate (Note 3) (d_r)	V_{OUT} = ±10V, C_S = 0.001μF		.025		25		25		mV/ms
Aperture Time (Note 3) (t_{ap})			60		60		60		ns
Sample Acquisition Time (Note 3) (t_{acq})	ΔVOUT = 20V, C_S = 0.001μF		15		15		15		μs
	ΔVOUT = 20V, C_S = 0.01μF		50		50		50		μs
Analog Voltage Output Range (Note 3) (V_{OUT})	R_L = 2kΩ			±10		±10			V

Notes:

1. V^+ = +15V, V^- = −15V Unless otherwise specified. Temporary limits are guaranteed through 25°C testing.
2. Tested go-no-go only.
3. Guaranteed parameter.
4. Class S only.

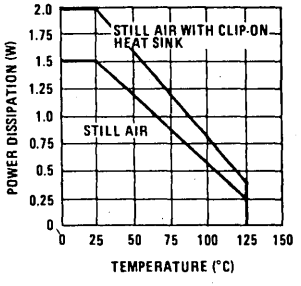
Burn-In Circuit

Metal Can (TO-8) Package
(9806HR)



Top View

Power Dissipation



LH0044/LH0044A Precision Low Noise Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (See Curve)	600mW
Differential Input Voltage (Note 1)	±15V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 10 sec)	300°C

General Description

The LH0044 is a low noise, ultra-stable, high gain, precision operational amplifier family intended to replace either chopper-stabilized monolithic or modular amplifiers. The devices are particularly suited for differential mode, inverting, and non-inverting mode applications requiring very low initial offset, low offset drift, very high gain, high CMR_R, and high PSRR. In addition, the LH0044 Series' low initial offset and offset drift eliminate costly and time consuming null adjustments at the systems level. The superior performance afforded by the LH0044 Series is made possible by advanced processing and testing techniques, as well as active laser trim of critical metal film resistors to minimize offset voltage and drift. Unique construction eliminates thermal feedback effects.

The LH0044 Series is an excellent choice for a wide range of precision applications including strain gauge bridges, thermocouple amplifiers, and ultrastable reference amplifiers.

The device is available in standard TO-5 op amp pinout and is compatible with LM108A, LM725, and LM741 type amplifiers.

RETS0044X, Rev −; RETS0044AX, Rev − (Teradyne W-301)

Parameter	Conditions (Note 3)		+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	V_{CM} = 0V, R_S = 50Ω	0044		50		150		150		µV
		0044A		25		75		75		µV
Input Offset Current (I_{IO})		0044		5		5		10		nA
		0044A		2.5		2.5		5.0		nA
Input Bias Current (I_{IB})		0044		30		30		100	±6	nA
		0044A		15		15		50	±5	nA
Power Supply Rejection Ratio (SV_{RR})	±5 ≤ V_{CC} ≤ ±15V		114		114		114			dB
Common Mode Rejection Ratio (CM_{RR})	−10V ≤ V_{CM} ≤ +10V		114		114		114			dB
Open Loop Voltage Gain (A_V)	R_L = 10kΩ, V_{OUT} = ±10V		114		114		114			dB
Output Voltage Swing (V_{OUT})	R_L = 10kΩ	0044	±12		±12		±12			V
		0044A	±13		±13		±13			V
Power Supply Current (I_{CC})	I_L = 0A	0044		4.0		4.0		4.0	±1.0	mA
		0044A		3.0		3.0		3.0	±1.0	mA
Power Dissipation (Note 4) (P_d)		0044		120		120		120		mW
		0044A		90		90		90		mW
Differential Input Impedance (Note 4) (R_{IN})		0044	2.5		2.5		2.5			MΩ
		0044A	5.0		5.0		5.0			MΩ
Temperature Coefficient of Input Offset Voltage (Note 5) ($\Delta V_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C	0044		1.0						µV/°C
		0044A		0.5						µV/°C
Temperature Coefficient of Input Offset Current (Note 5) ($\Delta I_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C	0044		80						pA/°C
		0044A		40						pA/°C
Temperature Coefficient of Input Bias Current (Note 5) ($\Delta I_{IB}/\Delta T$)	−55°C ≤ T_A ≤ +125°C	0044		600						pA/°C
		0044A		300						pA/°C
Long Term Stability (Note 5)	t = 1 month	0044		2.0						µV/t
		0044A		1.0						µV/t
Thermal Feedback Coefficient (Note 5)				0.02						µV/mV
Input Voltage Range (Note 6) (V_{IN})		0044	±12		±12		±12			V
		0044A	±13		±13		±13			V
Input Noise Voltage (Note 6) (V_N)	BW = 0.01Hz to 10Hz, R_S = 50Ω	0044		0.8						µVp-p
		0044A		0.7						µVp-p
	BW = 0.01Hz to 10Hz, R_S = 10kΩ imbalance	0044		1.0						µVp-p
		0044A		0.9						µVp-p

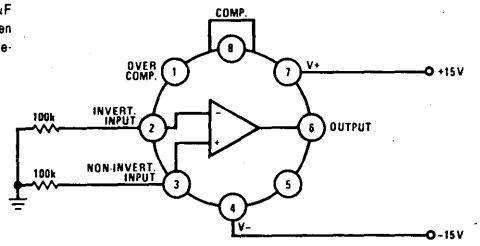
Notes:

1. The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow for differential input voltages in excess of 1V. Input current should be limited to less than 1mA.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. V_{CC} = ±15V unless otherwise specified. Temperature limits are guaranteed by 25°C testing.
4. Tested go-no-go only.
5. Guaranteed parameter, no testing available.
6. Guaranteed parameter, may be tested at extra cost.

Burn-In Circuit

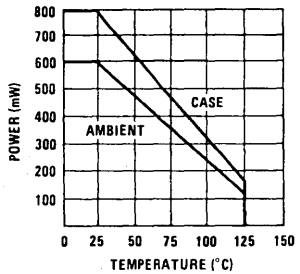
Note:
Case is electrically isolated. Compensation is not normally required however. For maximum stability 0.01µF capacitor should be placed between Pins 7 and 8 when device is used below closed loop gains of 10.

Metal Can Package (9181HR)



Top View

Maximum Power Dissipation



LH0045 Two Wire Transmitter

Absolute Maximum Ratings

Supply Voltage (L_1 to common)	+50V
Input Current	±20mA
Input Voltage (Either Input to Common)	0V to V_{REF}
Differential Input Voltage	±20V
Output Current (Either L_1 or L_2)	50mA
Reference Output Current	5.0mA
Power Dissipation	
LH0045G (Note 1)	1.5W
LH0045K (Note 1)	3.0W
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0045 Two Wire Transmitter is a linear integrated circuit designed to convert the voltage from a sensor to a current, and send it through to a receiver, utilizing the same simple twisted pair as the supply voltage.

The LH0045 contains an internal reference designed to power the sensor bridge, a sensitive input amplifier, and an output current source. The output current scale can be adjusted to match the industry standards of 4.0mA to 20mA or 10mA to 50mA.

Designed for use with various sensors, the LH0045 will interface with thermocouples, strain gauges, or thermistors. The use of the power supply leads as the signal output eliminates two or three extra wires in remote signal applications. Also, current output minimizes susceptibility to voltage noise spikes and eliminates line drop problems.

Features

- High sensitivity > 10μA/μV
- Low input offset voltage 2.0mV
- Low input bias current 2.0nA
- Single supply operation 10V to 50V
- Programmable bridge reference (LH0045G) 5.0V to 30V
- Non-interactive span and null adjust
- Over compensation capability
- Supply reversal protection

RETS0045G, Rev A; RETS0045K, Rev A (Teradyne W-301)

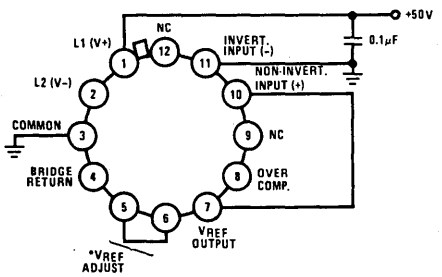
Parameter	Conditions (Note 2)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 6) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	I_{CC} = 4mA		2.0		3.0		3.0	±1.0	mV
Input Offset Current (I_{IO})			0.2		0.4		0.4		nA
Input Bias Current (I_{IB})			2.0		3.0		3.0	±1.0	nA
Open Loop Supply Current (I_{CC})	V_{CC} = 50V		3.0		3.0		3.0		mA
Reference Voltage (V_{REF})	I_{REF} = 2mA	4.3	5.9						V
	I_{REF} = 2mA, Pins 5 & 6 open (Note 3)	8.6	12						V
Supply Voltage Range (V_{CC}) (Note 4)		9.0	50.0	9.0	50.0	9.0	50.0		V
Reference Voltage Load Regulation (V_{RLOAD})	0 ≤ I_{REF} ≤ 2mA		0.2						%
Reference Voltage Line Regulation (V_{RLINE})	ΔVCC = 10V to 45V		0.5						mV/V
Power Supply Rejection Ratio (SV_{RR})	ΔVCC = 10V to 45V, I_{CC} = 12 mA		0.1		0.1		0.1		mV/V
Common Mode Rejection Ratio (CM_{RR})	ΔVIN = 10V to 3.3V, I_S = 4.0mA		0.1		0.1		0.1		mV/V
Open Loop Transconductance	ΔICC = 4mA to 20mA	10^6							μ℧
	ΔICC = 10mA to 50mA	2×10^6							μ℧
Resistor R_5	I_{CC} = 1.0mA	950	1050						Ω
Resistor R_9	I_{CC} = 12mA	95	105						Ω
Input Voltage Range (Note 4) (V_{IN})		1.0	3.3	1.0	3.3	1.0	3.3		V
Input Resistance (Note 4) (R_{IN})		30							MΩ
Temperature Coefficient of R_5 (Note 5) ($\Delta R_5/\Delta T$)	I_{CC} = 1.0mA, −55°C ≤ T_A ≤ +125°C		300						ppm/°C
Temperature Coefficient of R_9 (Note 5) ($\Delta R_9/\Delta T$)	I_{CC} = 12mA, −55°C ≤ T_A ≤ +125°C		300						ppm/°C
Input Voltage Range (Note 5) (V_{IN})		1.0	7.6	1.0	7.6	1.0	7.6		V
Supply Voltage Range (Note 5) (V_{CC})	Pins 5 & 6 open (Note 3)	15.0	50.0	15.0	50.0	15.0	50.0		V

Notes:

1. For operating at elevated temperatures, the TO-8 package must be derated at 30°C/W (junction to case) or 83°C/W (junction to ambient) and the TO-3 package must be derated at 25°C/W (junction to case) or 40°C/W (junction to ambient).
2. +10V ≤ V_{CC} ≤ +50V, pin 5 shorted to pin 6 (TO-8 package only) unless otherwise specified. Temperature limits guaranteed by 25°C testing.
3. TO-8 package only.
4. Tested go-no-go only.
5. Guaranteed parameter, no testing available.
6. Class S only.

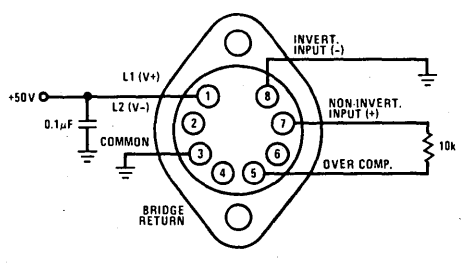
Burn-In Circuits

Metal Can (TO-8) Package (9265HR)



Top View

Metal Can (TO-3) Package



Top View

Note: * Pin 5 is shorted to pin 6 to obtain a nominal +5.1V, V_{REF}. Left open V_{REF} = +10V. The case is isolated from the circuit for both TO-3 and TO-8.

LH0052 Precision FET Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	±22 V
Power Dissipation (See Graph)	500mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V^-	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0052 is a FET input operational amplifier with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 200μV maximum offset and 5μV/°C offset drift. Input offset current is less than 100 femtoamps at room temperature and 100pA maximum at +125°C.

Features

- Low input offset current — 500 femtoamps max
- Low input offset drift — 10μV/°C max
- Low input offset voltage — 100μV typ
- High open loop gain — 100dB typ
- Excellent slew rate — 3.0V/μs typ
- Internal 6dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

The LH0052 is intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers.

RETS0052H, Rev 0A; RETS0052D, Rev 0A (Teradyne W-301)

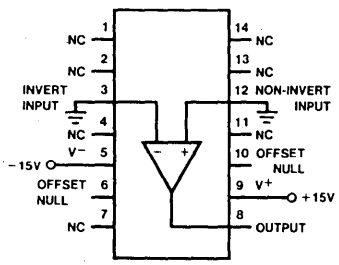
Parameter	Conditions	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 8) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 100kΩ		0.5		1.0		1.0	±0.25	mV
Input Offset Current (Note 5) (I_{IO})			0.5		500		Note 4		pA
Input Bias Current (Note 5) (I_{IB})			2.5		2500		Note 4		pA
Supply Current (I_{CC})			3.5		3.5		3.5		mA
Power Supply Rejection Ratio (SV_{RR})	R_S = 10kΩ, ±5V ≤ V_{CC} ≤ ±15V	74		74		74			dB
Common Mode Rejection Ratio (CM_{RR})	R_S = 10kΩ, V_{IN} = ±10V	74		74		74			dB
Large Signal Voltage Gain (A_V)	R_L = 2kΩ, V_{OUT} = ±10V	100		50		50			V/mV
Output Voltage Swing (V_{OUT})	R_L = 1kΩ at 25°C (R_L = 2kΩ at −55°C & +125°C)	±10		±10		±10			V
Output Short Circuit Current (I_{OS})			±50						mA
Input Voltage Range (Note 6) (V_{IN})		±12		±12		±12			V
Ouptut Current Swing (Note 6) (I_{OUT})	V_{OUT} = ±10V	±10		±5		±5			mA
Power Dissipation (Note 6) (P_D)			105		105		105		mW
Input Resistance (Note 6) (R_{IN})		10^{11}							Ω
Slew Rate (Note 7) (s_r)		1.5							V/μs
Rise Time (Note 7) (t_r)			1.5						μs
Overshoot (Note 7) (os)			30						%
Temperature Coefficient of Input Offset Voltage (Note 7) ($\Delta V_{IO}/\Delta T$)	+25°C ≤ T_A ≤ +125°C		5						μV/°C
	−55°C ≤ T_A ≤ +25°C		5						μV/°C
Temperature Coefficient of Input Offset Current (Note 7) ($\Delta I_{IO}/\Delta T$)	−55°C ≤ T_A ≤ +125°C	Doubles every 10 degrees Centigrade							
Temperature Coefficient of Input Bias Current (Note 7) ($\Delta I_B/\Delta T$)	−55°C ≤ T_A ≤ +125°C	Doubles every 10 degrees Centigrade							

Notes:

1. For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies for minimum source resistance of 10kΩ; for source resistances less than 10kΩ maximum differential input voltage is ±5V.
3. V_{CC} = ±15V unless otherwise specified.
4. The temperature coefficient of these parameters makes establishment of −55°C limit impossible.
5. These parameters are guaranteed at 25°C by testing at 125°C.
6. Tested go-no-go only.
7. Guaranteed parameter.
8. Class S only.

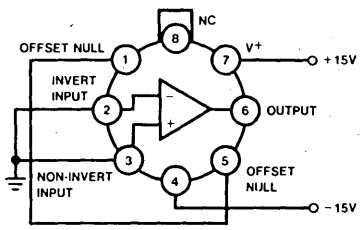
Burn-In Circuits

Dual-In-Line Package (8713HR)



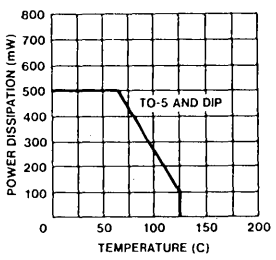
Top View

Metal Can (TO-5) Package (8336HR)



Top View

Maximum Power Dissipation



LH0053 High Speed Sample and Hold Amplifier

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	±18V
Gate Input Voltage (V_6 and V_7)	±20V
Analog Input Voltage (V_4)	±15V
Input Current (I_8 and I_5)	±10mA
Power Dissipation (See curve)	1.5W
Output Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0053 is a high speed sample and hold circuit capable of acquiring a 20V step signal in under 10μs.

The device is ideally suited for a variety of high speed data acquisition applications including analog buffer memories for A to D conversion and synchronous demodulation.

An auxiliary switch within the device extends its usefulness in applications such as preset integrators.

Features

- Sample acquisition time 10μs max for 20V signal
- FET switch for preset or reset function
- Sample accuracy null
- Offset adjust to 0V
- DTL/TTL compatible FET gate
- Single storage capacitor

RETS0053G, Rev 0A (Teradyne W-301)

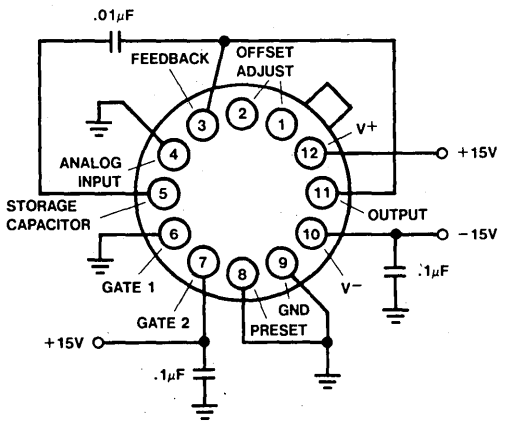
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 5) Drift Δ Limits (25°C) Only	Units
Supply Current (I_{CC})	V_4 = 0, V_8 = 0.5V		18.0		18.0		18.0		mA
Analog Output Voltage Range (V_{OUT})	R_L = 2kΩ	±10		±10		±10			V
Output Offset Voltage (V_{OO})	V_4 = 0, V_8 = 0.5V		7.0		10		10	±2	mV
Sample Accuracy	V_4 = ±10V, V_8 = 0.5V		0.2						%
Leakage Current, Pin 5 (Note 2) (I_{L5})	V_4 = ±10V		.03		30		Note 3		nA
Drift Rate	V_4 = ±10V, C_F = 1000pF		.03		3.0		Note 3		V/s
Analog Input Voltage Range (Note 2) (V_{IN})		±10		±10		±10			V
Aperture Time (Note 4) (t_{ap})	ΔV_8 = 4.5V		25						ns
Sample Acquisition Time (t_{acq}) (Note 4)	V_4 = ±10V, C_F = 1000pF		10						μs
	V_4 = ±10V, C_F = 100pF		9						μs
Q2 Switch ON Resistance (R_{ON})	V_7 = 0.5V, I_8 = 1.0mA		300						Ω
Input Bias Current (Note 4) (I_{IB})	V_4 = 0		250						nA
Input Resistance (Note 4) (R_{IN})		9.0	11.0						kΩ
Sample ("0") Input Voltage (Note 4) (V_{IL})			0.5		0.5		0.5		V
Hold ("1") Input Voltage (Note 4) (V_{IH})		4.5		4.5		4.5			V
Sample ("0") Input Current (Note 4) (I_{IL})	V_8 = .5V		−5.0		−100		−100		μA
Hold ("1") Input Current (Note 4) (I_{IH})	V_8 = 4.5V		.001		1.0		Note 3		μA

Notes:

1. V_{CC} = ±15V, V_{311} = 0, V_9 = 0, C_{511} = 1000pF.
2. Measured go-no-go only.
3. This parameter is unmeasurable at −55°C, the room temperature limit is guaranteed at −55°C.
4. Guaranteed parameter.
5. Class S only.

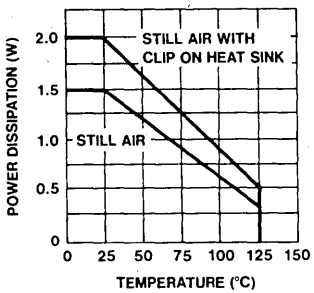
Burn-In Circuit

Metal Can Package (9293HR)



Top View

Power Dissipation



LH0061 0.5 Amp Wide Band Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	± 18V
Power Dissipation	See Curve
Differential Input Current (Note 1)	± 10mA
Input Voltage (Note 2)	± 15V
Peak Output Current	2A
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0061 is a wide band, high speed, operational amplifier capable of supplying currents in excess of 0.5A at voltage levels of ± 12V. Output short circuit protection is set by external resistors, and compensation is accomplished with a single external capacitor. With a suitable heat sink the device is rated at 20W.

The wide bandwidth and high output power capabilities of the LH0061 make it ideal for such applications as AC servos, deflection yoke drivers, capstan drivers, and audio amplifiers.

Features

- Output current 0.5A
- Wide large signal bandwidth 1MHz
- High slew rate 50V/μs
- Low standby power 240mW
- Low input current 300nA max

RETS0061X, Rev 0B (Teradyne W-301)

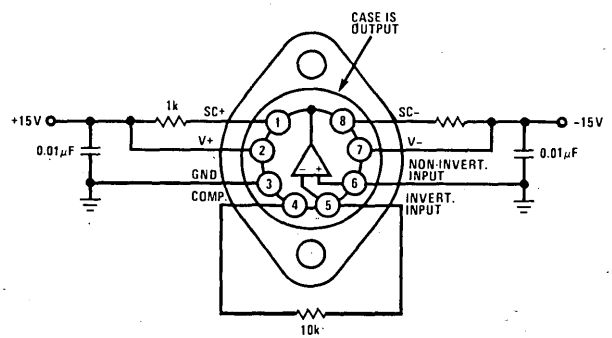
Parameter	Conditions (Note 4)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 7) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 0		4.0		6.0		6.0	± 1.0	mV
Input Offset Current (I_{IO})			100		300		300	± 20	nA
Input Bias Current (I_{IB})			300		1000		1000	± 50	nA
Voltage Gain (A_V)	V_{OUT} = ± 10V, R_L = 1kΩ	50							V/mV
Power Supply Current (I_{CC})	R_S = 0, V_{OUT} = 0	3.5	10		10		10		mA
Power Supply Rejection Ratio (SV_{RR})	± 5V ≤ V_{CC} ≤ ± 15V, R_S = 10kΩ	70		70		70			dB
Common Mode Rejection Ratio (CM_{RR})	ΔV_{CM} = ± 10V, R_S = 10kΩ	70		70		70			dB
Short Circuit Current (I_{OS})	V_{OUT} = 0, R_{SC} = 1Ω	± 400	± 800						mA
Output Voltage Swing (V_{OUT})	R_L = 20Ω	± 10		± 10		± 10			V
Input Resistance (Note 5) (R_{IN})		0.3							MΩ
Power Consumption (Note 5) (P_D)			300		300		300		mW
Input Voltage Range (Note 5) (V_{IN})		± 11		± 11		± 11			V
Slew Rate (Note 6) (s_r)	A_V = +1, R_L = 100Ω, C_C = 3000pF	50							V/μs
Voltage Gain (Note 6) (A_V)	V_O = ± 10V, R_L = 20Ω	5		5		5			V/mV
Small Signal Overshoot (Note 6) (os)	C_C = 3000pF		20						%

Notes:

1. The inputs are shunted with back-to-back diodes for overvoltage protection. Excessive current will flow if a differential voltage in excess of 1V is applied between the inputs without limiting resistors.
2. For supply voltages less than ± 15V the absolute maximum input voltage is equal to the supply voltage.
3. Rating applies as long as package power rating is not exceeded.
4. V_{CC} = ± 15V unless otherwise specified. Temperature limits are guaranteed by testing at 25°C.
5. Tested go-no-go only.
6. Guaranteed parameter.
7. Class S only.

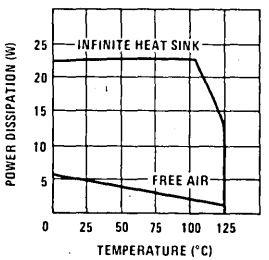
Burn-In Circuit

Metal Can (TO-3) Package

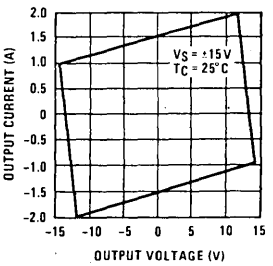


Top View

Power Dissipation



Safe Operating Area



LH0062 High Speed FET Op Amp

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (See graph)	500mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0062 is a precision, high speed FET input operational amplifier with more than an order of magnitude improvement in slew rate and bandwidth over conventional FET IC op amps. In addition it features very closely matched input characteristics, very high input impedance, and ultra low input currents with no compromise in noise, common mode rejection ratio or open loop gain. The device has internal unity gain frequency compensation, thus assuring stability in all normal applications. This considerably simplifies its application, since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation will boost the slew rate to over 120V/μs and almost double the bandwidth. (See LB-2, LB-14, and LB-17 for discussions of the application of feed-forward techniques.) Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1μs. In addition, it is free of latch-up and may be simply offset nulled with negligible effect on offset drift or CMRR.

The LH0062 is designed for applications requiring wide bandwidth, high slew rate and fast settling time while at the same time demanding the high input impedance and low input currents characteristic of FET inputs. Thus it is particularly suited for such applications as video amplifiers, sample/hold circuits, high speed integrators, and buffers for A/D conversion and multiplex system.

RETS0062X, Rev 3A (Teradyne W-301)

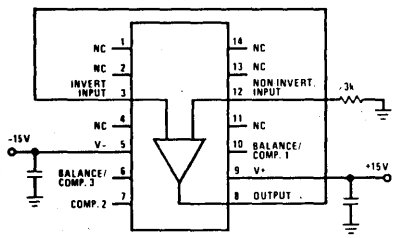
Parameter	Conditions (Note 3)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 8) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 100kΩ		5.0		7.0		7.0	±1.0	mV
Input Offset Current (Note 4) (I_{IO})			0.1		2		Note 5		nA
Input Bias Current (Note 4) (I_{IB})			0.1		10		Note 5		nA
Open Loop Voltage Gain (A_V)	R_L = 2kΩ, V_{OUT} = ±10V	50		25		25			V/mV
Power Supply Rejection Ratio (SV_{RR})	±5V ≤ V_{CC} ≤ ±15V	80		80		80			dB
Common Mode Rejection Ratio (CM_{RR})	−10V ≤ V_{CM} ≤ +10V	80		80		80			dB
Output Voltage Swing (V_{OUT})	R_L = 2kΩ	±12		±10		±10			V
Output Short Circuit Current (I_{OS})			±50						mA
Power Supply Current (I_{CC})		3.5	8.0		8.0		8.0		mA
Input Voltage Range (Note 6) (V_{IN})		±10		±10		±10			V
Power Consumption (Note 6) (P_D)			240		240		240		mW
Input Offset Current (Note 7) (I_{OS})			2						pA
Input Bias Current (Note 7) (I_{IB})			10						pA
Slew Rate (Note 7) (s_r)	(Voltage follower)	50							V/μs
Output Current Swing (Note 7) (I_{OUT})	V_{OUT} = ±10V	±10							mA
Temperature Coefficient of Input Offset Voltage (Note 7) ($\Delta V_{IO}/\Delta T$)	R_S = 100kΩ, −55°C ≤ T_A ≤ +125°C		25						μV/°C
Temperature Coefficient of Input Offset Current (Note 7) ($\Delta I_{IO}/\Delta T$)		Doubles every 10 degrees Centigrade							
Temperature Coefficient of Input Bias Current (Note 7) ($\Delta I_{IB}/\Delta T$)		Doubles every 10 degrees Centigrade							

Notes:

1. For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies for minimum source resistance of 10kΩ; for source resistances less than 10kΩ maximum differential input voltage is ±5V.
3. V_{CC} = ±15V unless otherwise specified.
4. Because of the current measuring limitations of automated test equipment, these tests are gross functional tests to guarantee parametric values. (See Note 7.)
5. Because of the temperature coefficient, no meaningful limits can be established for these parameters at −55°C.
6. Tested go-no-go only.
7. Guaranteed parameter.
8. Class S only.

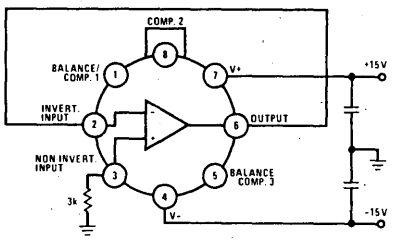
Burn-In Circuits

Dual-In-Line Package



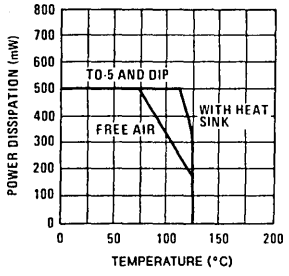
Top View

Metal Can (TO-5) Package



Top View

Maximum Power Dissipation



Note: All capacitors are .1μF every five sockets.

LH0063 Damn Fast Buffer

Absolute Maximum Ratings

Supply Voltage ($V^+ - V^-$)	40V
Maximum Power Dissipation (See Curve)	5W
Maximum Junction Temperature	175°C
Input Voltage	Equal to Supplies
Continuous Output Current	±250mA
Peak Output Current	±500mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0063 is a high speed, FET input, voltage follower/buffer designed to provide high current drive at frequencies from DC to over 100MHz. The LH0063 will provide ±250mA into 50Ω loads (±500mA peak) at slew rates of up to 6000V/μs. In addition, it exhibits excellent phase linearity up to 20MHz.

Features

- Damn fast — 2000V/μs
- Wide range single or dual supply operation
- Wide power bandwidth — DC to 100MHz
- High output drive — ±10V with 50Ω load
- Low phase non-linearity — 2 degrees
- Fast rise times — 3ns
- High current gain — 120dB
- High input resistance — $10^{10}\Omega$

It is intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffers for driving reactive loads and high impedance input buffers for high speed A-to-Ds and comparators. In addition, the LH0063/LH0063C can continuously drive 50Ω coaxial cables or be used as a diddle yoke driver for high resolution CRT displays. For additional applications information see AN-48.

Advantages

- Only +10V supply needed for $5V_{p\text{-}p}$ video out
- Speed does not degrade system performance
- Wide data rate range for phase encoded systems
- Output drive adequate for most loads
- Single pre-calibrated package

RETS0063K, Rev 1A (Teradyne W-301)

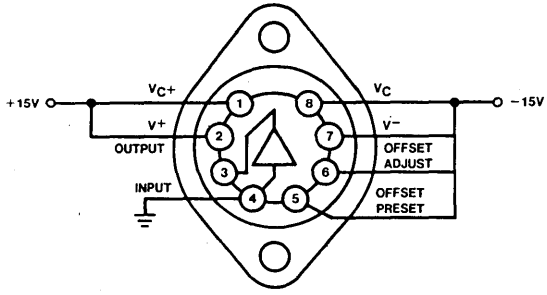
Parameter	Conditions	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Power Supply Current (I_{CC})	V_{CC} = ±15V, R_L = ∞		±65						mA
Output Offset Voltage (V_{OO})	V_{CC} = ±15V		±25		±100		±100		mV
Input Bias Current (I_{IB}) (Note 3)	V_{CC} = ±15V		.2		100		100		nA
Voltage Gain (A_V)	V_{IN} = ±10V, R_S = 100kΩ, R_L = 1kΩ (Note 1)	0.94	1	0.94	1	0.94	1		V/V
	V_{IN} = ±10V, R_S = 100kΩ, R_L = 50Ω (Note 1)	0.92	1.0	0.92	1.0	0.92	1.0		V/V
Output Voltage Swing (V_{OUT})	V_{CC} = ±5V, R_L = 50Ω	.5							$V_{p\text{-}p}$
Input Resistance (Note 2) (R_{IN})		10^{10}							Ω
Output Impedance (Note 2) (R_{OUT})	V_{OUT} = ±10V, R_S = 100kΩ		4		4		4		Ω
Slew Rate (Note 3) (s_r)	V_{CC} = ±15V, R_S = 50Ω, R_L = 50Ω, V_{IN} = ±10V	2000							V/μs
	V_{CC} = ±15V, R_S = 50Ω, R_L = 1kΩ, V_{IN} = +10V	4000							V/μs
Output Voltage Swing (V_{OUT})	R_L = 50Ω, V_{CC} = ±15V	±10		±10		±10			V
Bandwidth (Note 3) (G_{BW})	V_{IN} = $1V_{RMS}$, V_{CC} = ±15V, R_L = 50Ω	100							MHz
Rise Time (Note 3) (t_r)	V_{CC} = ±15V, R_S = 50Ω, R_L = 50Ω, ΔV_{IN} = 0.5V		3						ns
Propagation Delay (Note 3) (t_{pd})	V_{CC} = ±15V, R_S = 50Ω, R_L = 50Ω, ΔV_{IN} = 0.5V		3						ns
Harmonic Distortion (Note 3)			0.5						%

Notes:

1. For AV^+, V^+ = +25V, V^- = −5V; for AV^-, V^+ = +5V, V^- = −25V.
2. Tested go-no-go only.
3. Guaranteed parameter.

Burn-In Circuit

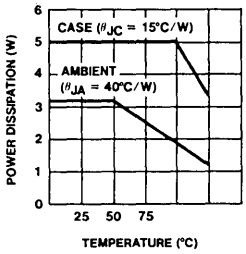
Metal Can (TO-3) Package



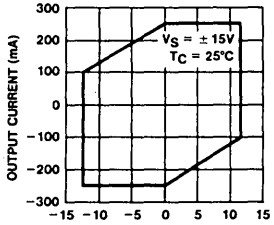
Top View

Note: Case is electrically isolated.

Power Dissipation



DC Safe Operating Area



LH0070 Series Precision BCD Buffered Reference
LH0071 Series Precision Binary Buffered Reference

Absolute Maximum Ratings

Supply Voltage	40V
Power Dissipation (See Curve)	600mW
Short Circuit Duration	Continuous
Output Current	±20mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0070 and LH0071 are precision, three terminal, voltage references consisting of a temperature compensated zener diode driven by a current regulator and a buffer amplifier. The devices provide an accurate reference that is virtually independent of input voltage, load current, temperature and time. The LH0070 has a 10.000V nominal output to provide equal step sizes in BCD applications. The LH0071 has a 10.240V nominal output to provide equal step sizes in binary applications.

The output voltage is established by trimming ultra-stable, low temperature drift, thin film resistors under actual operating circuit conditions. The devices are short-circuit proof in both the current sourcing and sinking directions.

The LH0070 and LH0071 series combine excellent long term stability, ease of application, and low cost, making them ideal choices as reference voltages in precision D to A and A to D systems.

Features

- Accurate output voltage
  - LH0070 10V ± 0.01%
  - LH0071 10.24V ± 0.01%
- Single supply operation 12.5V to 40V
- Low output impedance 0.1Ω
- Excellent line regulation 0.1mV/V
- Low zener noise 20μVp-p
- 3-lead TO-5 (pin compatible with the LM109)
- Short circuit proof
- Low standby current 3mA

RETS0070H-0, Rev 00 | RETS0070H-2, Rev 00 | RETS0071H-1, Rev 00
RETS0070H-1, Rev 00 | RETS0071H-0, Rev 00 | RETS0071H-2, Rev 00

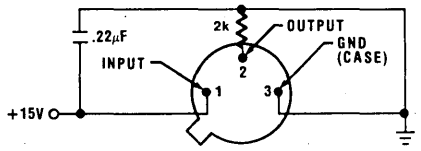
Parameter	Conditions (Note 1)		+25°C Min	+25°C Max	(Note 2) +125°C Min	(Note 2) +125°C Max	(Note 2) −55°C Min	(Note 2) −55°C Max	Δ Limit (25°C)	Units
Output Voltage (V_{OUT})		LH0070	9.5	10.5	9.5	10.5	9.5	10.5		V
		LH0071	9.75	10.75	9.75	10.75	9.75	10.75		V
Output Accuracy (Note 3)		-0, -1		±.1		±.3		±.3		%
		-2		±.05		±.2		±.2		%
Output Voltage Change with Temperature (Note 5) ($\Delta V_{OUT}/\Delta T$)	$-25°C \le T_A \le 25°C$, $25°C \le T_A \le 85°C$	-0		±.2						%
		-1		±.1						%
		-2		±.04						%
Line Regulation (V_{RLINE})	$13V \le V_{IN} \le 33V$	-0, -1		±.1						%
		-2		±.03						%
Load Regulation (V_{RLOAD})	$0mA \le I_{OUT} \le 5mA$			±.03						%
Input Voltage Range (Note 3) (V_{IN})			12.5	40	12.5	40	12.5	40		V
Quiescent Current (I_Q)	$13V \le V_{IN} \le 33V$, $I_{OUT} = 0$		1	5	1	5	1	5		mA
Change in Quiescent Current (ΔI_Q)	$13V \le V_{IN} \le 33V$, $I_{OUT} = 0$			1.5		1.5		1.5		mA
Output Resistance (Note 4) (R_{OUT})				1		1		1		Ω
Long Term Stability (Note 4)		-0, -1		±.2						%/yr
		-2		±.05						%/yr

Notes:

1. $V_{IN} = +15V$, $R_L = 10k\Omega$ unless otherwise specified.
2. Temperature characteristics are guaranteed, not measured.
3. Tested go-no-go only.
4. Guaranteed parameter, no testing available.
5. Tested 100% $25°C \le T_A \le 85°C$ guaranteed, not tested $-25°C \le T_A \le 25°C$.

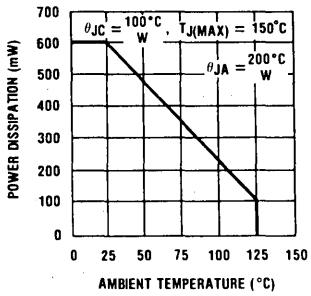
Burn-In Circuit

Metal Can (TO-5) Package



Bottom View

Power Dissipation



LH0075 Positive Precision Programmable Regulator

Absolute Maximum Ratings

Input Voltage	32V
Output Voltage	27V
Output Current	200mA
Power Dissipation	See Curve
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0075 is a precision programmable regulator for negative voltages. Regulated output voltages from 0 to +27V may be obtained by using 1 external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (5V, 6V, 10V, 12V, and 15V). The output current limit is adjustable from 0 to 200mA using 2 external resistors. These features provide an inventory of precision regulated values in 1 package.

Features

- Line regulation typically 0.008%/V
- Load regulation typically 0.075%
- Remote voltage sensing
- Ripple rejection — 80dB
- Output adjustable to 0V
- Adjustable precision current limit
- Output current to 200mA

RETS0075G, Rev 0A (Teradyne W-301)

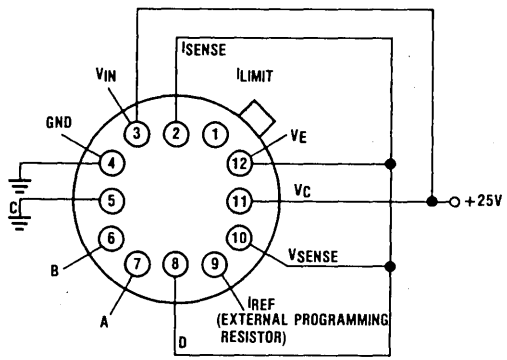
Parameter	Conditions	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Line Regulation (V_{RLINE})			.02						%/V
Load Regulation (V_{RLOAD})	$V_{OUT} \geq 5V$		3.2						%
	$V_{OUT} \leq 5V$		.3						%
Reference Current (I_{REF})	V_{IN} = 15V	.998	1.002						mA
Minimum Load Current (I_L)		98	102	98	102	98	102		μA
Output Voltage Range (Note 2) (V_{OUT})		0	27	0	27	0	27		V
Minimum Input Voltage (V_{IN})		±10		±10		±10			V
Input Output Differential Voltage (V_{DIFF})	$1mA \leq I_L \leq 200mA$		3.2						V
Quiescent Supply Current (I_{CC})			6.5		6.5		6.5		mA
Initial Output Voltage Tolerance	V_{OUT} = 2V, 5V, 6V, 10V (Note 3)		±.5		±.5		±.5		%
Functional Voltage Change with Temperature	$-55°C \leq T_A \leq 125°C$		.003						%/°C
Current Limit Function (I_{CL})	I_L = 0	0	10	0	10	0	10		mA
	I_L = 50mA	45	55	45	55	45	55		mA
	I_L = 200mA	195	205	195	205	195	205		mA

Notes:

1. Guaranteed parameter.
2. Tested go-no-go only.
3. V_{IN} = −15V, V_{OUT} obtained by using R4, R5, R6, and R8 individually.

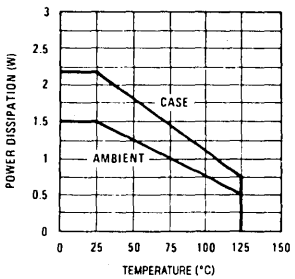
Burn-In Circuit

Metal Can Package (LH0075)



Top View

Maximum Power Dissipation



Note: Case is electrically isolated.

LH0076 Negative Precision Programmable Regulator

Absolute Maximum Ratings

Input Voltage	−32V
Output Voltage	−27V
Output Current	200mA
Power Dissipation	See Curve
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0076 is a precision programmable regulator for negative voltages. Regulated output voltages from 0 to −27V may be obtained by using 1 external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (−3V, −5V, −6V, −8V, −9V, −12V, −15V and −18V). The output current limit is adjustable from 0 to 200mA using 2 external resistors. These features provide an inventory of precision regulated values in 1 package.

Features

- Line regulation typically 0.005%/V
- Load regulation typically 0.02%
- Remote voltage sensing
- Ripple rejection — 70dB
- Output adjustable to 0V
- Adjustable precision current limit
- Output current to 200mA

RETS0076G, Rev 0A (Teradyne W-301)

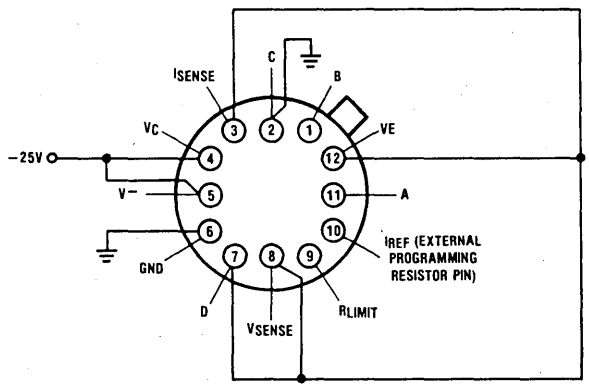
Parameter	Conditions	+25°C Min	+25°C Max	(Note 1) +125°C Min	(Note 1) +125°C Max	(Note 1) −55°C Min	(Note 1) −55°C Max	Δ Limit (25°C)	Units
Line Regulation (V_{RLINE})	$-12V \le V_{IN} \le -32V$		.02						%/V
Load Regulation (V_{RLOAD})	$V_{OUT} \ge -5V$, $1mA \le I_L \le 200mA$		7.5						mV
	$V_{OUT} \le -5V$, $1mA \le I_L \le 200mA$ (Note 1)		.15						%
Reference Current (I_{REF})	$V_{IN} = -15V$	.998	1.002						mA
Minimum Load Current (I_{LIM})		98	102	98	102	98	102		μA
Output Voltage Range (Note 2) (V_{OUT})		0	−27	0	−27	0	−27		V
Minimum Input Voltage (Note 2) (V_{IN})		−10		−10		−10			V
Input-Output Differential Voltage (V_{DIFF})	$1mA \le I_L \le 200mA$		3.2						V
Quiescent Supply Current (I_{CC})		−10	+15	−10	+15	−10	+15		mA
Initial Output Voltage Tolerance	V_{OUT} =3V, 5V, 6V, 9V (Note 3)		±.5		±.5		±.5		%
Functional Output Voltage (V_{OUT})		−15	−5	−15	−5	−15	−5		V
Functional Power Supply Current (I_{CC})		−12	−5	−12	−5	−12	−5		mA
Functional Current Limit Voltage (V_{CL})	V_{IN} − 32V	4.5	5.5						V

Notes:

1. Guaranteed parameter.
2. Tested go-no-go only.
3. $V_{IN} = -15V$, V_{OUT} obtained by using R4, R5, R6, and R8 individually.

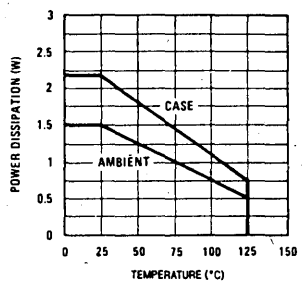
Burn-In Circuit

Metal Can Package (LH0076)



Top View

Maximum Power Dissipation



Note: Case is electrically isolated.

LH0082 Optical Communication Receiver

Absolute Maximum Ratings

Supply Voltage	12V
Power Dissipation (25°C)	.5W
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Lead Temperature (Soldering, 20 sec)	300°C
Input Current	± 10mA

General Description

The LH0082 is a general purpose, low-noise, fiber optic receiver, which may also be used as a fast current to voltage converter, or as a high speed voltage amplifier. The circuit includes a 2GHz gain-bandwidth FET-input amplifier, a 2.4 volt reference, a comparator with hysteresis, and all the necessary resistors and capacitors for feedback and coupling, all integrated in a hermetic dual-in-line package. The large gain-bandwidth of the preamp enables fast response even with high capacitance photodiodes. A separate analog output permits the reception of analog signals to 20MHz via a fiber optic link. The internal comparator converts a low level analog signal to a CMOS/TTL/DTL compatible logic signal at data rates up to 15Mbits/s NRZ. The LH0082 can be used with an external comparator at data rates to 50Mbits/s.

Features

- Single 4.5 to 12 volt supply
- DC to 50Mbits/s NRZ data bandwidth
- Low noise
- $< 10^{-9}$ bit error rate
- Pin selectable sensitivity: −45dBm/−35dBm*
- CMOS/TTL/DTL compatibility
- Can be used with photodiodes, PIN photodiodes, phototransistors, avalanche photodiodes, and photomultipliers
- > 80dB dynamic range

* Assumes 0.5 A/W PIN diode input

RETS0082D, Rev 0A (Teradyne J-273A)

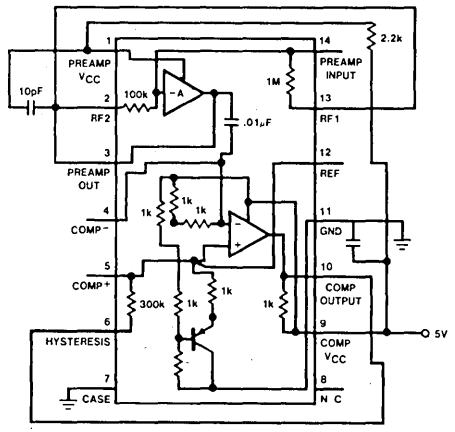
Parameter	Conditions (Note 3)	+25°C Min	+25°C Max	(Note 2) +125°C Min	(Note 2) +125°C Max	(Note 2) −55°C Min	(Note 2) −55°C Max	Δ Limit (25°C)	Units
Preamplifier:									
Input Bias Current (I_{IB}) (Note 2)			.2						nA
Input Capacitance (C_{IN}) (Note 2)			5						pF
Voltage Gain (A_V)		70							V/V
Output Quiescent Voltage (V_{OQ})		1.9	2.6	1.2	2.2	2.2	3.2		V
Output Voltage Swing (V_{OUT})	No Load	3.5							V
Transimpedance	Low Sensitivity	90	110						kΩ
	High Sensitivity	0.9	1.1						MΩ
Power Supply Current ($I_{CC}1$)		10	30						mA
Comparator/Reference:									
Comparator Input Resistance (R_{IN}) (Note 2)		.95	1.05						kΩ
Hysteresis Voltage (V_H) (Note 2)		7	11						mV
Reference Voltage (V_{REF})		2.2	2.6						V
Low Level Output Voltage (V_{OL})	I_{OL} = 3.2mA		0.5						V
High Level Output Voltage (V_{OH})	I_{OH} = −1mA	3.8							V
Power Supply Current ($I_{CC}9H$)	$V_{OUT} \geq 3.8V$	4.5	17						mA
($I_{CC}9L$)	$V_{OUT} \leq .5V$	9.5	22						mA
Total Supply Current (I_{CC}) (Note 3)	High or Low Sensitivity	14.5	52						mA

Notes:

1. $V_{CC}1$ = 5V, $V_{CC}9$ = 5V, unless otherwise specified.
2. Guaranteed parameter.
3. Tested go-no-go only.

Burn-In Circuit

Dual-In-Line-Package (9981HR)



Top View

Note: One supply ground for every 10 devices.

LH0084 Digitally Programmable Gain Instrumentation Amplifier

Absolute Maximum Ratings

Supply Voltage (Note 1)	± 18V
Analog Input Voltage (Note 2)	± 15V
Differential Input Voltage (Note 2)	± 30V
Digital Input Voltage	−4V, +18V
Power Dissipation (See Curve)	2.5W
Output Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 20 sec)	+300°C

General Description

The LH0084 is a self-contained, high speed, high accuracy, digitally-programmable-gain instrumentation amplifier. It consists of paired FET-input variable-gain voltage-follower input stages followed by a differential-to-single-ended output stage. The input stage is programmable in accurate gain steps of 1, 2, 5, or 10 controlled by the logic levels of a 2-bit TTL-compatible digital input word. For additional flexibility, the output stage is pin-strappable to fixed gains of 1, 4, or 10 for an overall gain range of 1 to 100.

Applications include increased dynamic range A-to-D converters, test systems, and post multiplexer amplifier for data acquisition systems.

The device exhibits high input impedance, low offset voltage, high CMRR and PSRR, high speed, and excellent gain accuracy and gain non-linearity.

Features

- Excellent gain accuracy — 0.1% max
  and gain non-linearity — 0.002% typ
- Extremely low gain drift — 1ppm/°C typ, 10ppm/°C max
- High input impedance — $10^{11}\Omega$ typ
- High CMRR and PSRR — 70dB min
- TTL compatible digital inputs
- High speed, settling to 0.1% — 4µs max

RETS0084D, Rev Preliminary (Teradyne W-301)

Parameter	Conditions (Note 4)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 100Ω, VCM = 0		10		15		15		mV
Output Offset Voltage (V_{OO})	R_S = 100Ω, VCM = 0		10		15		15		mV
Input Bias Current (I_{IB}) (Note 3)	R_S = 100Ω, VCM = 0		.5		500		500		nA
Input Offset Current (I_{IO}) (Note 3)	R_S = 100Ω, VCM = 0		.2		800		200		nA
Input Voltage Range (V_{IN}) (Note 5)		± 10		± 10		± 10			V
Gain Error (E_{AV})	A_V = 1 to 10		0.1		0.2		0.2		%
	A_V = 10 to 100		0.2		0.3		0.3		%
Gain Temperature Coefficient ($\Delta A_V/\Delta T$) (Note 6)	−55°C ≤ T_A ≤ +125°C		20						ppm/°C
Common Mode Rejection Ratio (CMR_R)	V_{IN} = ± 10V, A_V = 1	70		70		70			dB
	A_V = 10	76		76		76			dB
	A_V = 100	80		80		80			dB
Power Supply Rejection Ratio (SV_{RR})	±8V ≤ V_{CC} ≤ ± 18V, A_V = 1	70		70		70			dB
	A_V = 10	76		76		76			dB
	A_V = 100	80		80		80			dB
Output Voltage Swing (V_{OUT})		± 10		± 10		± 10			V
Output Short Circuit Current (I_{OS})		±5	± 30	±2	± 30	±2	± 30		mA
Logical "0" Input Voltage (V_{IL}) (Note 5)			0.7		0.7		0.7		V
Logical "1" Input Voltage (V_{IH}) (Note 5)		2.0		2.0		2.0			V
Logical "0" Input Current (I_{IL})	V_{IN} = .4V		40		40		40		µA
Logical "1" Input Current (I_{IH})	V_{IN} = 2.4V		10		10		10		µA
Power Supply Voltage Range (V_{CC}) (Note 5)		±8	± 18	±8	± 18	±8	± 18		V
Power Supply Current (I_{CC+})	V_{CC} = ± 18V		26		26		26		mA
(I_{CC-})	V_{CC} = ± 18V		14		14		14		mA
Power Dissipation (P_d) (Note 5)	V_{CC} = ± 18V		720		720		720		mW
	V_{CC} = ± 15V (Note 6)		600		600		600		mW
Slew Rate (s_r) (Note 6)	V_{OUT} = ± 10V	10							V/µs
Settling Time (t_{set}) (Note 6)	ΔV_{OUT} = ± 20V, A_V = 1		3.0						µs
	A_V = 10		3.5						µs
	A_V = 100		4.0						µs

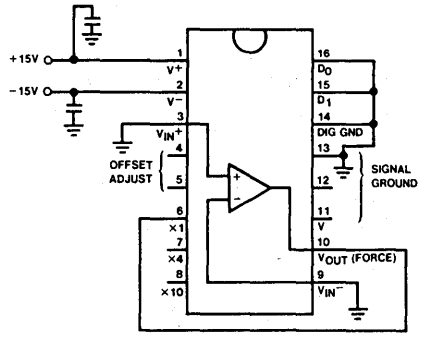
Notes:

1. Improper supply power-on sequence may damage the device.
2. For supply voltages less than ± 15V the maximum input voltage is equal to the supply voltage.
3. 25°C limit is guaranteed through 125°C testing.
4. V_{CC} = ± 15V, R_L = 10kΩ, unless otherwise specified.
5. Tested go-no-go only.
6. Guaranteed parameter.

Burn-In Circuit

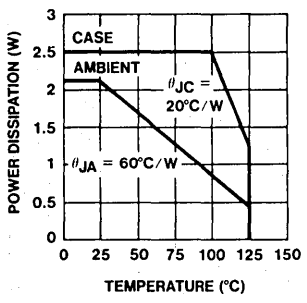
Dual-In-Line Package (9968HR)

Note: Case is electrically isolated. Capacitors are .1µF every five sockets.



Top View

Power Dissipation



LH0086 Digitally Programmable Gain Amplifier

Absolute Maximum Ratings

Supply Voltage (Note 1)	±18V
Analog Input Voltage (Note 2)	±15V
Digital Input Voltage	−4V, +18V
Power Dissipation (See Curve)	
Output Short Circuit Duration	continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0086 is a self-contained high speed, high accuracy, digitally-programmable gain amplifier. It consists of a FET input operational amplifier, a precision resistor ladder and a digitally programmable switch network. A three bit TTL compatible digital input word selects accurate gain steps of 1, 2, 5, 10, 20, 50, 100, or 200.

The LH0086 exhibits low offset voltage, high input impedance, PSRR, high speed, and excellent gain accuracy and gain linearity.

Features

- Excellent gain accuracy and gain non-linearity. .05% Typ.
- Extremely low gain drift. 1ppm/°C Typ.
- High input impedance. 10^{11} Typ.
- High SV_{RR} 80dB min.
- TTL compatible digital inputs.
- High speed, settling to .1% 5μs Typ.

RETS0086X, Rev Preliminary

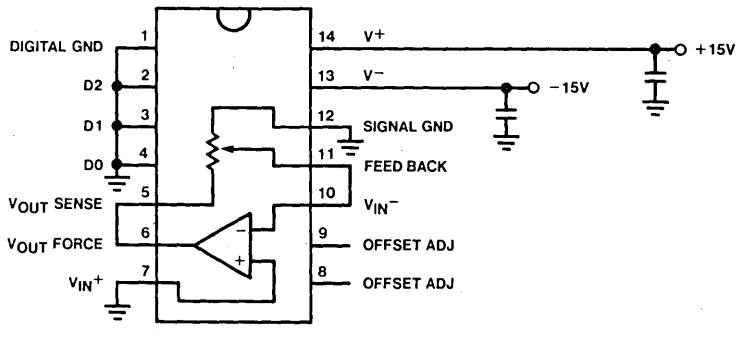
Parameter	Conditions (Note 3)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})			5.0		7.0		7.0		mV
Input Bias Current (I_{IB}) (Note 6)			0.5		500		500		nA
Input Offset Current (I_{IO})			0.2		200		200		nA
Input Voltage Range (V_{IN}) (Note 5)		±10		±10		±10			V
Output Voltage Swing (V_{OUT})	R_L = 10kΩ	±10		±10		±10			V
Power Supply Rejection Ratio (SV_{RR})	±8V ≤ V_{CC} ≤ ±18V	80		80		80			dB
Output Short Circuit Current (I_{OS}) (Note 4)		±5	±30	±2	±30	±2	±30		mA
Logical "0" Input Voltage (V_{IL}) (Note 5)			.7		.7		.7		V
Logical "1" Input Voltage (V_{IH}) (Note 5)		2.0		2.0		2.0			V
Logical "0" Input Current (I_{IL})	V_{IL} = .4V		4.0		4.0		4.0		μA
Logical "1" Input Current (I_{IH})	V_{IH} = 2.4V								μA
Supply Voltage Range (V_{CC}) (Note 5)		±8	±18	±8	±18	±8	±18		V
Power Supply Current (I_{CC}+)			15.5		15.5		15.5		mA
(I_{CC}−)			8.5		8.5		8.5		mA
Power Dissipation (P_d) (Note 5)			370		370		370		mW
Voltage Gain (A_V)	A_V = 1								V/V
	A_V = 2								V/V
	A_V = 5								V/V
	A_V = 10								V/V
	A_V = 20								V/V
	A_V = 50								V/V
	A_V = 100								V/V
	A_V = 200								V/V
Gain Error (A_{VE}) (Note 4)	A_V = 1		.01		.02		.02		%
	A_V = 2, 5, 10		.05		.10		.10		%
	A_V = 20, 50, 100, 200		.20		.30		.30		%

Notes:

1. Improper supply power on sequence may damage the device.
2. For supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.
3. V_{CC} = ±15V, R_L = 10kΩ, pin 10 connected to pin 11, pin 5 connected to pin 6 unless otherwise specified.
4. Guaranteed parameter.
5. Tested go-no-go only.
6. 25°C limits guaranteed through 125°C testing.

Burn-In Circuit

Dual-In-Line Package
(9967HR)



Top View

Note: Capacitors are .1μF every fifth socket.

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LH0091 True RMS to DC Converter

Absolute Maximum Ratings

Supply Voltage	±22V
Input Voltage	±15V Peak
Output Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0091, rms to dc converter, generates a dc output equal to the rms value of any input per the transfer function:

$$E_{OUT\ (DC)} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2\,(t)\,dt}$$

The device provides rms conversion to an accuracy of 0.1% of reading using the external trim procedure. It is possible to trim for maximum accuracy (0.5 mV ± 0.05% typ) for decade ranges, i.e., 10 mV—100 mV, 0.7V—7V, etc.

Features

- Low cost
- True RMS conversion
- 0.5% of reading accuracy untrimmed
- 0.5% of reading accuracy with external trim
- Minimum component count
- Input voltage to ±15V peak for V_S = ±15V
- Uncommitted amplifier for filtering, gain, or high crest factor configuration
- Military or commercial temperature range

RETS0091X, Rev − (Teradyne W-301)

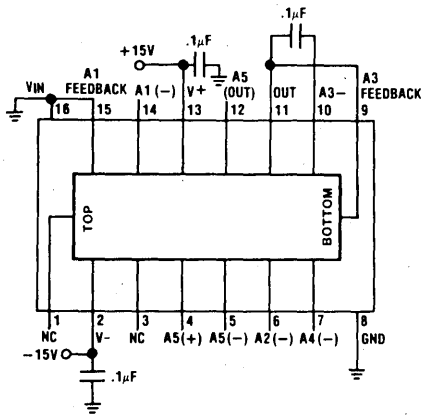
Parameter	Conditions (Note 2)	+25°C Min	+25°C Max	(Note 1) +125°C Min	(Note 1) +125°C Max	(Note 1) −55°C Min	(Note 1) −55°C Max	(Note 5) Δ Limit (25°C)	Units
Converter Characteristics									
Total Unadjusted Error (Note 3, Figure 1)	$50mV_{rms} \le V_{IN} \le 7V_{RMS}$		40, ±1		65, ±3		65, ±3		mV, %
Total Adjusted Error (Note 3, Figure 2)	$50mV_{RMS} \le V_{IN} \le 7V_{RMS}$		1, ±.2		1, ±.2		1, ±.2		mV, %
Frequency for Specified Adjusted Error (Note 3)	$V_{IN} \le 7V_{RMS}$ (sine wave)	30		30		30			kHz
Frequency for 1% Additional Error (Note 3)	$V_{IN} \le 7V_{RMS}$ (sine wave)	100		100		100			kHz
Crest Factor (Note 3)	(Crest Factor = $V_{peak} + V_{RMS}$ of a wave form)	5		5		5			
Input Voltage Range (Note 4) (V_{IN})		±.05	±11	±.05	±11	±.05	±11		V_{peak}
Input Impedance (Note 4) (R_{IN})		4.5							kΩ
Output Voltage Swing (V_{OUT})	R_L = 2.5kΩ	±10		±10		±10			V
Op amp characteristics									
Output Voltage Swing (V_{OUT})	R_L = 2.5kΩ	±10		±10		±10			V
Quiescent Current (I_Q)	V_{CC} = ±15V		18		18		25		mA
Input Offset Voltage (V_{IO})	R_S = 10kΩ		10		20		20	±2	mV
Input Offset Current (I_{IO})			200		500		500		nA
Input Bias Current (I_{IB})			500		1500		1500		nA
Large Signal Voltage Gain (A_V)	V_{OUT} = ±10V, R_L = 2kΩ	15		10		10			V/mV

Notes:

1. Temperature characteristics are guaranteed, not tested.
2. V_{CC} = ±15V, unless otherwise specified.
3. Guaranteed parameter, no testing available.
4. Tested go-no-go only.
5. Class S only.

Burn-In Circuit

Dual-In-Line Package



Top View

Figure 2 LH0091 DC Trim Connection

R1 = dc symmetry balance
R2 = Input offset
R3 = Output offset
R4 = Gain output

Note: This procedure will give accuracies of 0.5mV offset ± 0.05% reading for inputs from 0.05V peak to 10V peak.

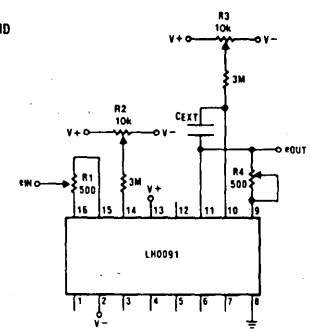
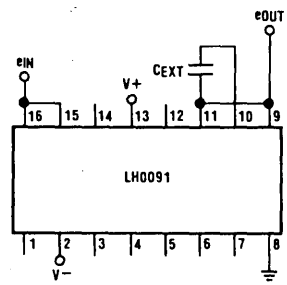


Figure 1 LH0091 Basic Connection (No Trim)



Note: $C_{EXT} \ge 1\mu F$; frequency ≥ 1kHz

Procedure:

1. Apply $50mV_{DC}$ to the input. Read and record the output.
2. Apply $-50mV_{DC}$ to the input. Use R2 to adjust for an output of the same magnitude as in step 1.
3. Apply 50mV to the input. Use R3 to adjust the output for 50mV.
4. Apply −50mV to the input. Use R2 to adjust the output for 50mV.
5. Apply ± 10V alternately to the input. Adjust R1 until the output readings for both polarities are equal (not necessary that they be exactly 10V).
6. Apply 10V to the input. Use R4 to adjust for 10V at the output.
7. Repeat this procedure to obtain the desired accuracy.

LH0094 Multifunction Converter

Absolute Maximum Ratings

Supply Voltage	±22V
Input Voltage	±22V
Output Short Circuit Duration	continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH0094 multifunction converter generates an output voltage per the transfer function:

$E_O = V_Y (V_Z/V_X)^m$, $0.1 \leq m \leq 10$

m is continually adjustable, and is set by two resistors.

RETS0094D, Rev 1A (Teradyne W-301)

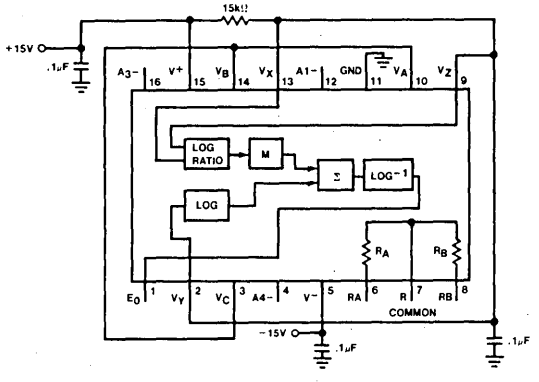
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Output Voltage Swing, (V_{OUT})									
Multiplication Mode	R_L = 10kΩ	10		10		10			V
Division Mode	R_L = 10kΩ	10		10		10			V
Square Mode	R_L = 10kΩ	10		10		10			V
Square Root Mode	R_L = 10kΩ	10		10		10			V
Power Supply Current (I_{CC})			5		5		5		mA
Output Offset Voltage (V_{CC})	V_X = 10V, V_Y = V_Z = 10V, Multiplication Mode		5		5		5		mV
Multiplication Accuracy 1	V_X = 10V, V_Y = .03V, V_Z = .01V	−.45	.45	−.65	.65	−.65	.65		% FS
2	V_X = 10V, V_Y = .5V, V_Z = .5V	−.45	.45	−.65	.65	−.65	.65		% FS
3	V_X = 10V, V_Y = 1V, V_Z = 1V	−.45	.45	−.65	.65	−.65	.65		% FS
4	V_X = 10V, V_Y = 5V, V_Z = 5V	−.45	.45	−.65	.65	−.65	.65		% FS
5	V_X = 10V, V_Y = 10V, V_Z = 10V	−.45	.45	−.65	.65	−.65	.65		% FS
Division Accuracy 1	V_X = .5V, V_Y = 10V, V_Z = .01V	−.45	.45	−.65	.65	−.65	.65		% FS
2	V_X = 1V, V_Y = 10V, V_Z = .5V	−.45	.45	−.65	.65	−.65	.65		% FS
3	V_X = 5V, V_Y = 10V, V_Z = 1V	−.45	.45	−.65	.65	−.65	.65		% FS
4	V_X = 10V, V_Y = 10V, V_Z = 5V	−.45	.45	−.65	.65	−.65	.65		% FS
5	V_X = 10V, V_Y = 10V, V_Z = 10V	−.45	.45	−.65	.65	−.65	.65		% FS
Square Accuracy 1	V_X = V_Y = 10V, V_Z = .1V	−1.0	1.0						% FS
2	V_X = V_Y = 10V, V_Z = .5V	−1.0	1.0						% FS
3	V_X = V_Y = 10V, V_Z = 1V	−1.0	1.0						% FS
4	V_X = V_Y = 10V, V_Z = 5V	−1.0	1.0						% FS
5	V_X = V_Y = 10V, V_Z = 10V	−1.0	1.0						% FS
Square Root Accuracy 1	V_X = V_Y = 10V, V_Z = .03V	−.45	.45						% FS
2	V_X = V_Y = 10V, V_Z = .1V	−.45	.45						% FS
3	V_X = V_Y = 10V, V_Z = .5V	−.45	.45						% FS
4	V_X = V_Y = 10V, V_Z = 1V	−.45	.45						% FS
5	V_X = V_Y = 10V, V_Z = 5V	−.45	.45						% FS
6	V_X = V_Y = 10V, V_Z = 10V	−.45	.45						% FS
Input Voltage (V_{IN}) (Note 2)		0	10	0	10	0	10		V

Notes:

1. V_{CC} = ±15V, unless otherwise specified.
2. Tested go-no-go only.

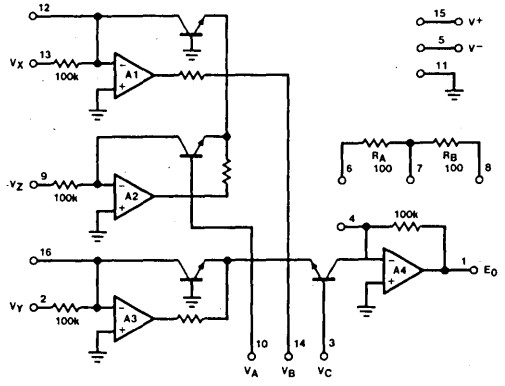
Burn-In Circuit

Dual In-Line Package
(9733HR)



Top View

Simplified Schematic



LH0101/LH0101A Power Operational Amplifier

Absolute Maximum Ratings

Supply Voltage, V_{CC}	±22V
Power Dissipation at T_A = 25°C, P_d (Note 1)	5W
Power Dissipation at T_C = 25°C (Note 2)	62W
Differential Input Voltage, V_{IN}	±40V (< ±V_{CC})
Input Voltage Range, V_{CM}	±20V (< ±V_{CC})
Peak Output Current (50ms pulse), $I_{O(PK)}$	5A
Output Short Circuit Duration	Continuous (Note 3)
Operating Temperature Range, T_A	−55°C to +125°C
Storage Temperature Range, T_{STG}	−65°C to +150°C
Maximum Junction Temperature, T_J	150°C
Lead Temperature (Soldering < 10 sec)	300°C

General Description

The LH0101 is a wideband power operational amplifier featuring FET inputs, internal compensation, virtually no crossover distortion, and rapid settling time. These features make the LH0101 an ideal choice for DC or AC servo amplifiers, deflection yoke drives, programmable power supplies, and disk head positioner amplifiers. The LH0101 is packaged in an 8 pin TO-3 hermetic package, rated at 20 watts with a suitable heat sink.

Features

- 5 Amp peak, 2 Amp continuous output current
- 300kHz power bandwidth
- 850mW standby power (± 15V supplies)
- 300pA input bias current
- 10V/μs slew rate
- Virtually no crossover distortion
- 2μs settling time to 0.01%
- 5MHz gain bandwidth

RETS0101K, Rev 0A; RETS0101AK, Rev 0A (Teradyne J-273, Test Box HDN-30-273)

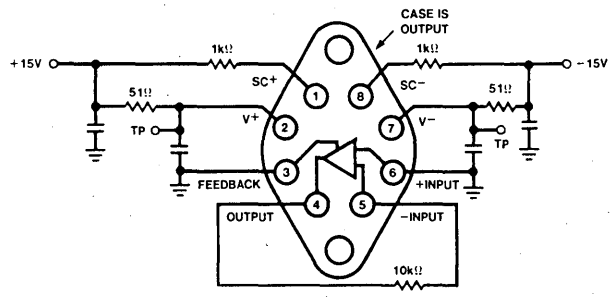
Parameter	Conditions (Note 4)		+25°C Min	+25°C Max	+125°C Min	+125°C Max	(Note 5) −55°C Min	(Note 5) −55°C Max	Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	V_{IN} = 0, R_S = 50Ω	0101		10		15		15		mV
		0101A		3		7		7		mV
Input Offset Current (I_{IO})	V_{IN} = 0	0101		.25		250		250		nA
		0101A		.075		75		75		nA
Input Bias Current (I_{IB})	V_{IN} = 0	0101		1		1000		1000		nA
		0101A		.3		300		300		nA
Large Signal Voltage Gain (A_V)	V_{OUT} = ±10V, R_S = 100Ω (10Ω for 0101A)		50		50		50			V/mV
Output Voltage Swing (V_{OUT})	R_{SC} = 0, A_V = +1, R_L = 100Ω		12		12		12			V
	R_L = 10Ω		11.25		11.25		11.25			V
	R_L = 5Ω		10.5		10.5		10.5			V
Common Mode Rejection Ration (CM_{RR})	ΔV_{IN} = ±10		85		85		85			dB
Supply Voltage Rejection Ratio (SV_{RR})	±5V ≤ V_{CC} ≤ ±15V		85		85		85			dB
Supply Current (I_{CC})				35		35				mA
Slew Rate (S_r) (Note 6)		0101A	7.5							V/μs
Gain Bandwidth (GBW) (Note 6)		0101A	4							MHz

Notes:

1. Derate linearly at 25°C/W to zero at 150°C (see curve).
2. Derate linearly at 2°C/W to zero at 150°C (see curve).
3. Within rated power dissipation, R_{SC} = .35Ω, T_A = 25°C.
4. V_{CC} = ±15V unless otherwise specified.
5. −55°C testing guaranteed
6. Guaranteed parameter, sampled to 10% LTPD.

Burn-in Circuit

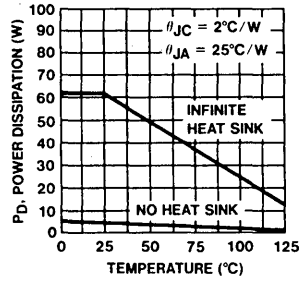
Metal Can (TO-3) Package (9312HR)



Top View

Note: Capacitors are .1μF every fifth socket.

Maximum Power Dissipation



LH1605 5-Amp High Efficiency Switching Regulator

Absolute Maximum Ratings

Input-Output Differential (V_{IN}-V_{OUT})	5V min
Input Voltage (V_{IN})	35V max
Output Current (I_{OUT})	6A max
Operating Temperature (T_J)	150°C
Internal Power Dissipation (Note 1)	20W
Duty Cycle	20% to 80%
V_{7-8}	60V
I_{7-8}	6A
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH1605 is a hybrid switching regulator with high output current capabilities. It incorporates a temperature-compensated voltage reference, a duty cycle modulator with the oscillator frequency programmable, error amplifier, high current-high voltage output swtich, and a power diode. The LH1605 can supply up to 5A of output current over a wide range of regulated output voltage.

Features

- Step down switching regulator
- Output adjustable from 3.0 to 30V
- 5A output current
- High efficiency
- Frequency adjustable to >100kHz
- Standard 8-pin TO-3 package

RETS1605X, Rev Prel. (Teradyne J-273)

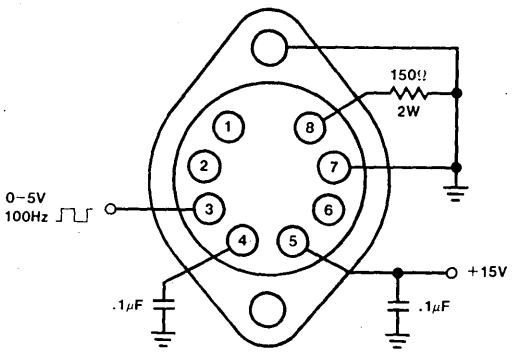
Parameter	Conditions (Note 2)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Output Voltage Range (V_{OUT})	I_{OUT} = 2A, $V_{IN} \geq (V_{OUT} + 5V)$	3.0	30.0						V
Switch Saturation Voltage (V_S)	I_C = 5A		2.0						V
	I_C = 2A		1.2						V
Diode ON Voltage (V_F)	I_D = 5A		2.8						V
	I_D = 2A		2.0						V
Supply Voltage Range (V_{CC})		10	35						V
Diode Reverse Current (I_{RD})	V_{RD} = 25V		5						μA
Quiescent Current (I_Q)	I_{OUT} = .2A, duty cycle = 100%		60						mA
	duty cycle = 0%		20						mA
Pin 2 Voltage (V_{REF})		2.28	2.72						V

Notes:

1. Derate at 30°C/W case to ambient, 6.5°C/W junction to case for operation above 25°C
2. V_{IN} = 15V, V_{OUT} = 10V unless otherwise specified.

Burn-In Circuit

Metal Can (TO-3) Package



Top View

Pin Functions

1
2 External Capacitor (V_{REF})
3 Error Amplifier Input
4 Timing Capacitor C_T
5 Input
6
7 Steering Diode (Anode)
8 Output
Case Ground

LH2011/LH2011B Operational Amplifier

Absolute Maximum Ratings

Total Supply Voltage	40V
Input Current (Note 1)	±10mA
Power Dissipation (Note 2)	500mW
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH2011 is two LM11's in a single package. The LM11 is a precision dc amplifier combining the best features of existing bipolar and FET op amps. It is similar to the LM108A, except that input currents have been reduced by more than a factor of ten. Offset voltage and drift have also been improved.

Compared to FETs, the device provides inherently lower offset voltage and offset voltage drift, along with at least an order of magnitude better long-term stability. Low frequency noise is also somewhat reduced. Bias current is significantly lower even under laboratory conditions, and its low drift makes compensation practical. Offset current is almost unmeasureable. Although not as fast as FETs, it does have a much lower power drain. This low dissipation has the added advantage of eliminating warm-up time in critical applications.

RETS2011X, Rev Prel.; RETS2011XB, Rev Prel. (Teradyne J-273A)

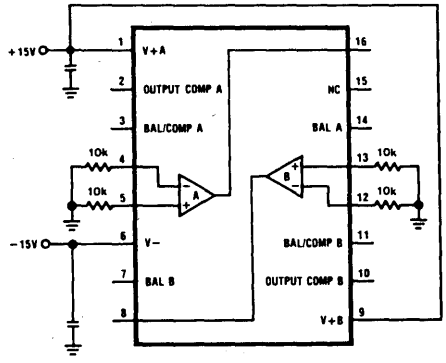
Parameter	Conditions (Note 3)		+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 6) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})		2011		0.3		0.6		0.6	±.1	mV
		2011B		0.6		1.1		1.1	±.2	mV
Input Offset Current (I_{IO})				10		30		30		pA
Input Bias Current (I_{IB})		2011		50		150		150		pA
		2011B		100		300		300		pA
Large Signal Voltage Gain (A_V)	V_{CC} = ±15V, I_{OUT} = ±2mA, V_{OUT} = ±12V		100							V/mV
	V_{CC} = ±15V, I_{OUT} = ±2mA, V_{OUT} = ±11.5V				50		50			V/mV
	V_{CC} = ±15V, I_{OUT} = ±.5mA, V_{OUT} = ±12V		250							V/mV
	V_{CC} = ±15V, I_{OUT} = ±.5mA, V_{OUT} = ±11.5V				100		100			V/mV
Common Mode Rejection Ratio (CM_{RR})	V_{CC} = ±15V, −13V ≤ V_{CM} ≤ 14V		110							dB
	V_{CC} = ±15V, −12.5V ≤ V_{CM} ≤ 14V				100		100			dB
Supply Voltage Rejection Ratio (SV_{RR})	±2.5V ≤ V_{CC} ≤ ±20V		100		96		96			dB
Power Supply Current (I_{CC})		2011		0.6		0.8		0.8		mA
		2011B		0.8		1.0		1.0		mA
Temperature Coefficient of Input Offset Voltage ($\Delta V_{IO}/\Delta T$) (Note 4)	−55°C ≤ TA ≤ 125°C	2011		3.0						μV/°C
		2011B		5.0						μV/°C
Temperature Coefficient of Input Bias Current ($\Delta I_{IB}/\Delta T$) (Note 4)	−55°C ≤ TA ≤ 125°C	2011		1.5						pA/°C
		2011B		3.0						pA/°C
Common Mode Input Voltage Range (V_{CM}) (Note 5)	V_{CC} = ±20V		+19		+19		+19			V
	V_{CC} = ±20V		−18		−17.5		−17.5			V
	V_{CC} = ±2.5V		+1.5		+1.5		+1.5			V
	V_{CC} = ±2.5V		.5		−0		−0			V
	V_{CC} = ±15V		+14		+14		+14			V
	V_{CC} = ±15V		−13		−12.5		−12.5			V

Notes:

1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used. In addition, a 2 kΩ minimum resistance in each input is advised to avoid possible latch up initiated by supply reversals.
2. The maximum operating-junction temperature is 150°C for the LM11. Devices must be derated based on package thermal resistance.
3. V_{CC} ±20V, V_{CM} = 0 unless otherwise specified.
4. Guaranteed parameter.
5. Tested go-no-go only.
6. Class S devices only.

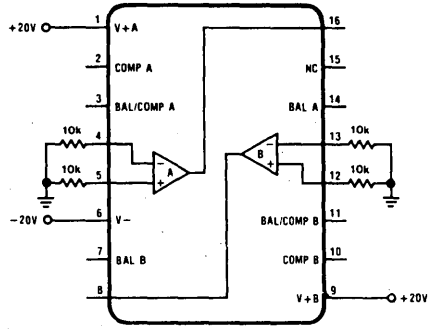
Burn-In Circuits

Dual-In-Line Package (8627HR)



Top View

Flat Package (8776:1R)



Top View

LH2101A Dual High Performance Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	+22V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	+30V
Input Voltage (Note 2)	+15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH2101A dual operational amplifier is two LM101A type op amps in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two singles. For additional information, see the LM101A data sheet and National's Linear Application Handbook.

Features

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

RETS2101AD, Rev OA (Teradyne W-301, TDN-25-301-059)

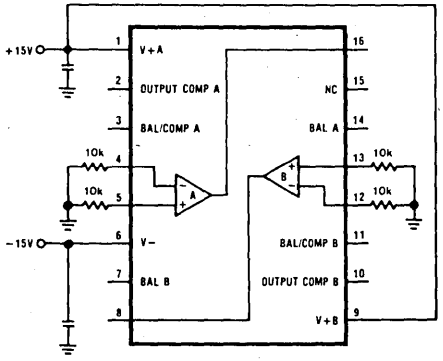
Parameter	Conditions (Note 3)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 50kΩ		2.0		3.0		3.0		mV
Input Offset Current (I_{IO})			10		20		20		nA
Input Bias Current (I_{IB})			75		100		100		nA
Power Supply Current (I_{CC})	V_{CC} = ±20V		3.0		2.5				mA
Supply Voltage Rejection Ratio (SV_{RR})	R_S = 50kΩ, ±5V ≤ V_{CC} ≤ ±20V	80		80		80			dB
Common Mode Rejection Ratio (CM_{RR})	R_S = 50kΩ, −10V ≤ V_{CM} ≤ +10V	80		80		80			dB
Large Signal Voltage Gain (A_V)	V_{OUT} = ±10V, R_L = 2kΩ	50		25		25			V/mV
Short Circuit Current (I_{OS})			±50		±50		±50		mA
Output Voltage Swing (V_{OUT})	R_L = 10kΩ	±12		±12		±12			V
	R_L = 2kΩ	±10		±10		±10			V
Input Resistance (R_{IN}) (Note 4)		1.5							MΩ
Input Voltage Range (V_{IN}) (Note 5)	V_{CC} = ±20V	±15		±15		±15			V
Temperature Coefficient of V_{IO} (Note 4)	−55°C ≤ TA ≤ 125°C		15						μV/°C
Temperature Coefficient of I_{IO} (Note 4)	25°C ≤ TA ≤ 125°C		.1						nA/°C
	−55°C ≤ TA ≤ 25°C		.2						nA/°C

Notes:

1. The maximum junction temperature of the LH2101A is 150°C. For operating temperatures of devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
2. For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. V_{CC} = ±15V unless otherwise specified.
4. Guaranteed parameter.
5. Tested go-no-go only.

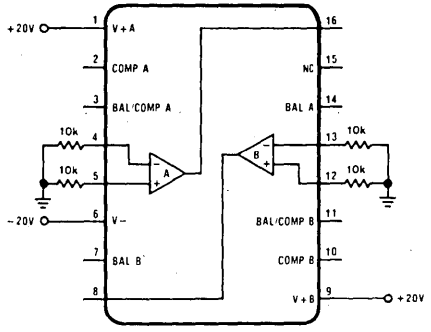
Burn-In Circuits

Dual-In-Line Package (8627HR)



Top View

Flat Package (8776HR)



Top View

LH2108/LH2108A Dual Super Beta Operational Amplifiers

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH2108A and LH2108 of dual operational amplifiers are two LM108A or LM108 type op amps in a single hermetic package. Featuring all the same performance characteristics of the single device, these duals also offer closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two single devices. For additional information see the LM108A or LM108 data sheet and National's Linear Application Handbook.

Features

- Low offset current 50pA
- Low offset voltage 0.7 mV
- Low offset voltage
  - LH2108A 0.3mV
  - LH2108 0.7mV
- Wide input voltage range ±15V
- Wide operating supply range ±3V to ±20V

RETS2108D, Rev 0B; RETS2108AD, Rev 0C (Teradyne J-273A, HDN-30-273-003)

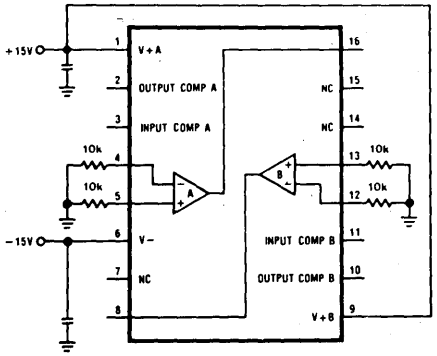
Parameter	Conditions (Note 3)		+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 4) Δ Limit (25°C)	Units
Power Supply Current (I_{CC})				0.6		0.4		0.8		mA
Short Circuit Current (I_{OS})				±30		±30		±30		mA
Output Voltage Swing (V_{OUT})	V_{CC} = ±15V, R_L = 10kΩ		±13		±13		±13			V
Voltage Gain (A_V)	V_{CC} = ±15V, R_L = 10kΩ, V_{OUT} = ±10V	2108	50		25		25			V/mV
		2108A	80		40		40			V/mV
Input Offset Voltage (V_{IO})	R_S = 0, V_{CM} = 0, V_{CM} = ±15V	2108		2.0		3.0		3.0	±.5	mV
		2108A		0.5		1.0		1.0	±.25	mV
	R_S = 1MΩ, V_{CM} = 0, V_{CM} = ±15V	2108		2.0		3.0		3.0	±.5	mV
		2108A		0.5		1.0		1.0	±.25	mV
	V_{CC} = ±5V, V_{CM} = 0, R_S = 0, 1MΩ	2108		2.0		3.0		3.0	±.5	mV
		2108A		0.5		1.0		1.0	±.25	mV
Input Bias Current (I_{IB})	V_{CM} = 0, V_{CM} = ±15V			2.0		3.0		3.0	±1.0	nA
	V_{CC} = ±5V, V_{CM} = 0			2.0		3.0		3.0	±1.0	nA
Input Offset Current (I_{IO})	V_{CM} = 0, V_{CM} = ±15V			0.2		0.4		0.4		nA
	V_{CC} = ±5V, V_{CM} = 0			0.2		0.4		0.4		nA
Common Mode Rejection (CM_{RR})	−15V ≤ V_{CM} ≤ +15V	2108	85		85		85			dB
		2108A	96		96		96			dB
Power Supply Rejection Ratio (SV_{RR})	±5V ≤ V_{CC} ≤ ±20V	2108	80		80		80			dB
		2108A	96		96		96			dB

Notes:

1. The maximum junction temperature of the LH2108A/LH2108 is 150°C. For operating devices in the flat package at elevated temperatures, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
3. V_{CC} = ±20V unless otherwise specified.
4. Class S only.

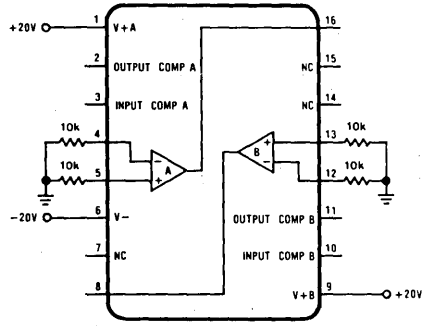
Burn-In Circuits

Dual-In-Line Package (8627HR)



Top View

Flat Package (8776HR)



Top View

LH2110 Dual Voltage Follower

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	+300°C

General Description

The LH2110 dual voltage follower is two LM110 type followers in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information, see the LM110 data sheet and National's Linear Application Notebook.

Features

- Low input current — 1nA
- High input resistance — $10^{10}\Omega$
- High slew rate — 30V/μs
- Wide bandwidth — 20MHz
- Wide operating supply range — ±5V to ±18V
- Output short circuit proof

RETS2110, Rev 1A (Teradyne W-301)

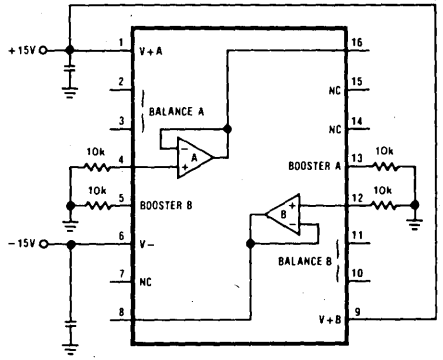
Parameter	Conditions (Note 4)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 10kΩ		±4		±6		±6		mV
Input Bias Current (I_{IB})	R_S = 1MΩ		3.0		10.0		10.0		nA
Voltage Gain (A_V)	V_{OUT} = ±10V, R_L = 8kΩ	.999		.999		.999			V/V
Output Voltage Swing (V_{OUT})	R_L = 10kΩ	±10		±10		±10			V
Supply Current (I_{CC})	V_{IN} = 0 (limit is per follower)		5.5		4.0				mA
Power Supply Rejection Ratio (SV_{RR})	±5V ≤ V_{CC} ≤ ±20V	70							dB
Input Resistance (R_{IN}) (Note 5)		10^{10}							Ω
Output Resistance (R_{OUT}) (Note 5)			2.5						Ω

Notes:

1. The maximum junction temperature of the LH2110 is 150°C. For operating devices in the flat package at elevated temperatures, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Continuous short circuit is allowed for case temperature to 125°C and ambient temperatures to 70°C. It is necessary to insert a resistor greater than 2kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.
4. V_{CC} = ±15V unless otherwise specified.
5. Guaranteed parameter.

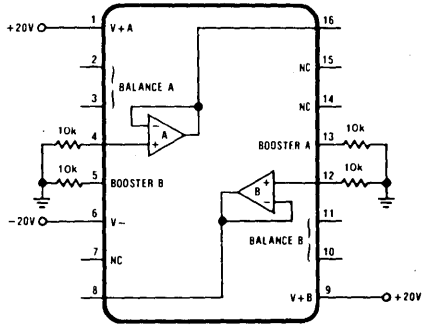
Burn-In Circuits

Dual-In-Line Package (8627HR)



Top View

Flat Package (8776HR)



Top View

LH2111 Dual Voltage Comparator

Absolute Maximum Ratings

Total Supply Voltage ($V^+ - V^-$)	36V
Output to Negative Supply Voltage ($V_{OUT} - V^-$)	−50V
Ground to Negative Supply Voltage ($GND - V^-$)	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH2111 dual voltage comparator is two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information see the LM111 data sheet and National's Linear Application Handbook.

Features

- Wide operating supply range ±15V to a single ±5V
- Low input currents 6nA
- High sensitivity 10μV
- Wide differential input range ±30V
- High output drive 50mA, 50V

RETS2111X, Rev 0 (Teradyne J-273)

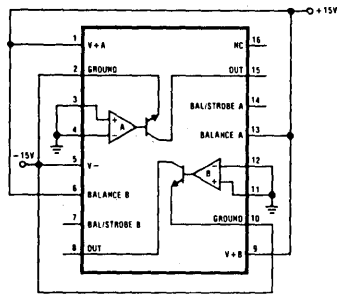
Parameter	Conditions (Note 3)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 5) Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	V_{CM} = +13.5V, −14.5V, 0		3.0		4.0		4.0	±.5	mV
	R_S = 50kΩ, V_{CM} = +13.5V, −14.5V, 0		3.0		4.0		4.0	±.5	mV
	$V_{85} = V_{86}$ = 0, V_{CM} = +13.5V, −14.5V, 0		3.0						mV
	$V_{85} = V_{86}$ = 0, R_S = 50kΩ, V_{CM} = +13.5V, −14.5V, 0		3.0						mV
	V^+ = 4.5V, V^- = 0, V_{OUT} = .4V, V_{CM} = 3V, & .5V		5.0		6.0		6.0		mV
	V^+ = 4.5V, V^- = 0, V_{OUT} = 4.5V, V_{CM} = 3V, .5V		3.0		4.0		4.0		mV
Input Offset Current (I_{IO})	R_S = 50kΩ, V_{CM} = +13.5V, −14.5V, 0		10.0		20.0		2.0		nA
	$V_{85} = V_{86}$ = 0, R_S = 50kΩ, V_{CM} = +13.5V, −14.5V, 0		30.0						nA
Input Bias Current (I_{IB})	R_S = 50kΩ, V_{CM} = +13.5V, −14.5V, 0		100		100		150	±10	nA
Large Signal Gain (A_{VS})	R_L = 1kΩ, V_{OUT} = −12V to +35V	40		30		30			V/mV
Emitter Follower Gain (A_{VEF})	R_L = 600Ω, V_I = −15V to +12V	10		8		8			V/mV
Common Mode Rejection Ratio (CM_{RR})	+13.5V ≥ V_{CM} ≥ −14.5V	80		80		80			dB
Negative Supply Current (I_{CC}^-)			−5.0		−5.0		−15	±.5	mA
Positive Supply Current (I_{CC}^+)			6.0		6.0		15		mA
Input Leakage Current (I_{IL})	V_{CC} = ±18V, V_{28} = 1V, V_{38} = 30V, V_{OUT} = 50V (Note 4)		10		30				nA
	V_{CC} = ±18V, V28 = 30V, V38 = 1V, V_{OUT} = 50V (Note 4)		10		30				nA
Output Leakage Current (I_{LO})	V_{CC} = ±18V, $I_5 + I_6$ = 5mA, V_{OUT} = 50V (Note 4)		25		500				nA
Ground Leakage Current (I_{LG})	V_{CC} = ±18V, $I_5 + I_6$ = 5mA, V_{OUT} = 50V (Note 4)		25		500				nA
Saturation Voltage (V_{SAT})	I_{OUT} = 50mA, V_{IN} = −5mV		1.5						V
	I_{OUT} = 8mA, V_{IN} = −6mV		0.4		0.4		0.4		V
Strobe ON Current (I_{STR}) (Note 6)			4.0						mA
Response Time (t_{resp}) (Note 6)	V_{IN} = 100mV with 5mV overdrive		400						ns

Notes:

1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. The maximum junction temperature is 150°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2 ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
3. V_{CC} = ±15V, V_{CM} = 0, V_{OUT} = 1.4V, V_{56} = 0, R_S = 0, unless otherwise specified (V_{85} = voltage differential between V^+ and balance; V_{86} = voltage differential between V^+ and bal/strobe; V_{56} = voltage differential between balance and bal/strobe; V_{28} = voltage differential between V^+ and In^+, V_{38} = voltage differential between V^+ and In^-; I_5 = current on balance; I_6 = Current on bal/strobe).
4. With respect to V^-.
5. Class S only. V_{IO} deltas are not measured at V_{CM} = 0; I_{IB} deltas are measured only at V_{CM} = 0.
6. Guaranteed parameter.

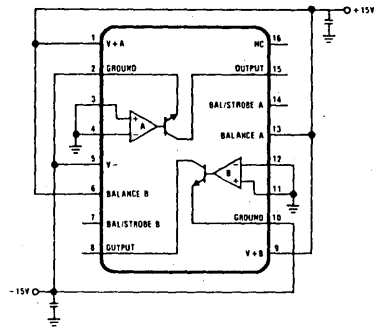
Burn-In Circuits

Dual-In-Line Package (9106HR)



Top View

Flat Package (8626HR)



Top View

LH24250 Dual Programmable Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage (Note 2)	±15V
Input Voltage (Note 3)	±15V
Output Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH24250 dual programmable micropower operational amplifier is two LM4250 type op amps in a single hermetic package. Featuring all the same performance characteristics of the LM4250, the LH24250 duals also offers closer thermal tracking, lower weight, reduced insertion cost and smaller size than two single devices. For additional information, see the LM4250 data sheet and National's Linear Application Handbook.

Features

- ±1V to ±18V power supply operation
- Standby power consumption as low as 20 μW
- Offset current programmable for less than 0.5 nA to 30 nA
- Programmable slew rate
- May be shut-down using standard open collector TTL
- Internally compensated and short circuit proof

RETS24250X, Rev — (Teradyne J-273)		+25°C		+125°C		−55°C		Δ Limit	
Parameter	Conditions (Note 3)	Min	Max	Min	Max	Min	Max	(25°C)	Units
	Electrical testing is performed using the LM4250 test tapes. See RETS4250X in the linear section.								

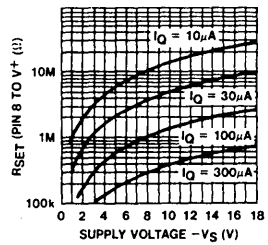
Notes:

1. Derate linearly 2 mW/°C case temperature above 25°C.
2. This rating applies to maximum voltage differential between input terminals. The maximum input voltage on either input terminal is limited to +V up to ±15V.
3. This rating limited to ± supply voltage to a maximum of ±15V.

Typical Quiescent Current Setting Resistor

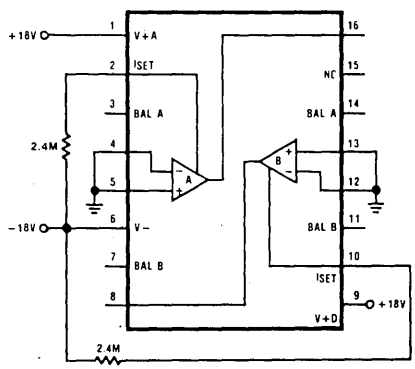
(Pin 8 to V⁻)

V_{CC}	10μA	30μA	100μA	300μA
±1.5V	1.5MΩ	470kΩ	150kΩ	
±3V	3.3MΩ	1.1MΩ	330kΩ	100kΩ
±6V	7.5MΩ	2.7MΩ	750kΩ	220kΩ
±9V	13MΩ	4MΩ	1.3MΩ	350kΩ
±12V	18MΩ	5.6MΩ	1.5MΩ	510kΩ
±15V	22MΩ	7.5MΩ	2.2MΩ	620kΩ



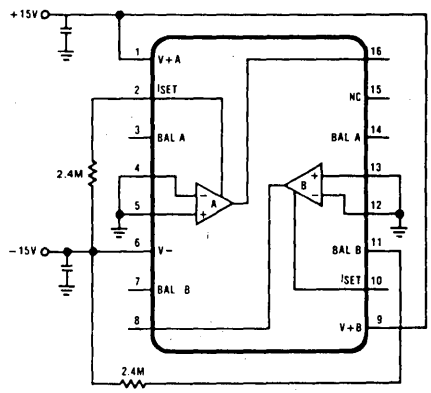
Burn-In Circuits

Dual-In-Line Package (9496HR)



Top View

Flat Package (8837HR)



Top View

LH740A FET Input Operational Amplifier

Absolute Maximum Ratings

Supply Voltage	±22V
Maximum Power Dissipation	500mW
Differential Input Voltage	±5V
Input Voltage	±15V
Short Circuit Duration	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The LH740A is a FET input, general purpose operational amplifier with high input impedance, closely matched input characteristics, and good slew rates.

Features

- Internal 6dB/octave frequency compensation
- Unity gain slew rate in excess of 6V/μs
- Unity gain bandwidth of 1MHz
- Input offset is adjustable with a single 10k pot
- Pin compatible with LM741, LM709, LM101A, and μA740
- Excellent offset current match over temperature, typically 100pA
- Output is continuously short-circuit proof

RETS740AX, Rev – (Teradyne W-301)

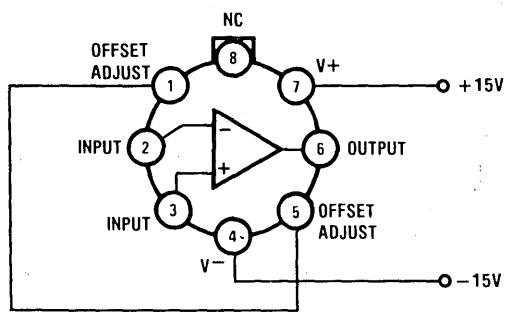
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Input Offset Voltage (V_{IO})	R_S = 100kΩ		15.0		20.0		20.0		mV
Input Offset Current (I_{IO})	(Note 2)		100		500		500		pA
Input Bias Current (I_{IB})	(Note 2)		.2		4.0		4.0		nA
Supply Current (I_{CC})			4.0						mA
Power Supply Rejection Ratio (S_{VRR})	R_S = 10kΩ ±5V ≤ V_{CC} ≤ ±15V	80		80		80			dB
Common Mode Rejection Ratio (C_{MRR})	R_S = 10kΩ V_{IN} = ±10V	80		80		80			dB
Large Signal Voltage Gain (Av)	R_L = 2kΩ, V_{OUT} = ±10V	50		40		40			V/mV
Output Voltage Swing (V_{OUT})	R_L = 2kΩ	±10		±10		±10			V
	R_L = 10kΩ	±12		±12		±12			V
Output Short Circuit Current (I_{OS})			±50						mA
Input Voltage Range (V_{IN}) (Note3)		±12		±12		±12			V
Output Current Swing (I_{OUT}) (Note 3)	V_{OUT} = ±10V	±10		±5		±5			mA
Power Dissipation (P_D) (Note 3)			120						mW
Input Resistance (R_{IN}) (Note 3)		10^8							Ω
Slew Rate (s_r) (Note 4)		2.0							V/μs
Rise Time (t_r) (Note 4)			1.0						μs
Overshoot (O_S) (Note 4)			20						%
Temperature Coefficient of Input Offset Voltage (Note 4) ($\Delta V_{IO}/\Delta T$)	−55°C to + 125°C		50						μV/°C
Temperature Coefficient of Input Offset Current (Note 4) ($\Delta I_{IO}/\Delta T$)	−55°C to + 125°C		4.0						pA/°C
Temperature Coefficient of Input Bias Current (Note 4) ($\Delta I_{IB}/\Delta T$)	−55°C to + 125°C		40						pA/°C

Notes:

1. V_{CC} = ±15V, unless otherwise specified.
2. Parameter guaranteed at 25°C, may be tested at extra cost.
3. Tested go-no-go only.
4. Guaranteed parameter.

Burn-In Circuit

Metal Can Package



Top View

MH0007 DC Coupled MOS Clock Driver

Absolute Maximum Ratings

V_{CC} Supply Voltage	8V
V^- Supply Voltage	−40V
V^+ Supply Voltage	+28V
($V^+ - V^-$) Voltage Differential	30V
Input Voltage	5.5V
Power Dissipation (T_A = 25°C, see curve)	800mW
Peak Output Current	±500mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The MH0007 is a voltage translator and power booster designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with inputs or clocks of MOS FET type devices. The design allows the user a wide latitude in selection of supply voltages, and is especially useful in normally "off" applications, since power dissipation is typically only 5 milliwatts in the "off" state.

Features

- 30 volts (max) output swing
- Standard 5V power supply
- Peak currents in excess of ±300mA available
- Compatible with all MOS devices
- High speed: 5MHz with nominal load
- External trimming possible for increased performance

RETS0007H, Rev A (Teradyne W-301)

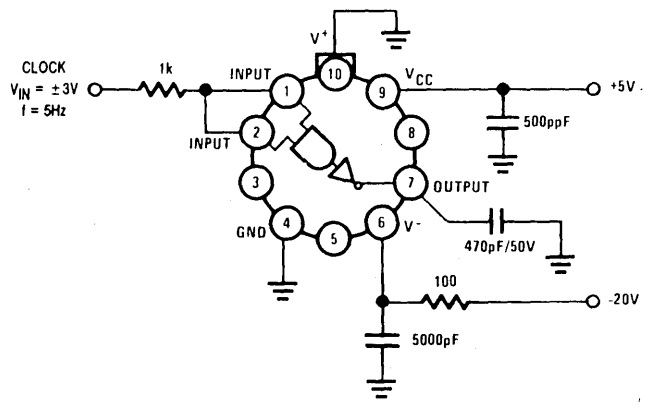
Parameter	Conditions	+25°C Min	+25°C Max	(Note 1) +125°C Min	(Note 1) +125°C Max	(Note 1) −55°C Min	(Note 1) −55°C Max	(Note 4) Δ Limit (25°C)	Units
Logical "1" Output Voltage (V_{OH})	V_{CC} = 5.5V, V^+ = 28V, V^- = −2V, I_{OUT} = −30mA, V_{IN} = .8V	24		24		24		±.2	V
	V_{CC} = 5.5V, V^+ = 28V, V^- = −2V, I_{OUT} = −1mA, V_{IN} = .8V	26		26		26			V
	V_{CC} = 5.5V, V^+ = −10V, V^- = −40V, I_{OUT} = −30mA, V_{IN} = .8V	−14		−14		−14			V
	V_{CC} = 5.5V, V^+ = −10V, V^- = −40V, I_{OUT} = −1mA, V_{IN} = .8V	−12		−12		−12			V
Logical "0" Output Voltage (V_{OL})	V_{CC} = 4.5V, V^+ = 28V, V^- = −2V, I_{OUT} = 30mA, V_{IN} = 2.2V	−2	0	−2	0	−2	0		V
	V_{CC} = 4.5V, V^+ = −10V, V^- = −40V, I_{OUT} = 30mA, V_{IN} = 2.2V	−40	−38	−40	−38	−40	−38		V
Logical "1" Input Current (I_{IH})	V_{CC} = 5.5V, V_{IN} = 5.5V, V^+ = 28V, V^- = −2V		100		100		100	±10	μA
	V_{CC} = 5.5V, V_{IN} = 5.5V, V^+ = −10V, V^- = −40V		100		100		100	±10	μA
Logical "0" Input Current (I_{IL})	V_{CC} = 5.5V, V_{IN} = .4V, V^+ = 28V, V^- = −2V		1.5		1.5		1.5		mA
	V_{CC} = 5.5V, V_{IN} = .4V, V^+ = −10V, V^- = −40V		1.5		1.5		1.5		mA
Logical "1" Input Voltage (Note 2) (V_{IH})		2.2		2.2		2.2			V
Logical "0" Input Voltage (Note 2) (V_{IL})			.8		.8		.8		V
Logical "1" Output Voltage (Note 3) (V_{OH})	V_{CC} = 5.5V, V_{IN} = .8V, I_{OUT} = −30mA	$V^+ - 4$		$V^+ - 4$		$V^+ - 4$			V
	V_{CC} = 5.5V, V_{IN} = .8V, I_{OUT} = −1mA	$V^+ - 2$		$V^+ - 2$		$V^+ - 2$			V
Logical "0" Output Voltage (Note 3) (V_{OL})	V_{CC} = 4.5V, V_{IN} = 2.2V, I_{OUT} = −30mA		$V^- + 2$		$V^- + 2$		$V^- + 2$		V
Propagation Delay Time (Note 3) (t_{pd})	V_{CC} = 5V, V^- = −17V, V^+ = 3V, C_L = 200pF		60						ns
	V_{CC} = 5V, V^- = −17V, V^+ = 3V, C_L = 200pF		80						ns
Rise Time (Note 3) (t_r)	V_{CC} = 5V, V^- = −17V, V^+ = 3V, C_L = 200pF		55						ns
Fall Time (Note 3) (t_f)	V_{CC} = 5V, V^- = −17V, V^+ = 3V, C_L = 200pF		65						ns

Notes:

1. Temperature limits are guaranteed, but may be tested at extra cost.
2. Tested go-no-go only.
3. Guaranteed parameter, no testing available.
4. Class S only.

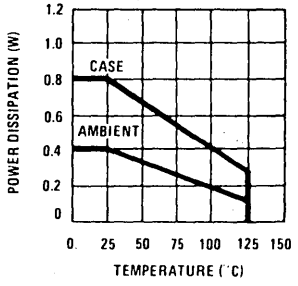
Burn-In Circuit

Metal Can Package
(10-Pin TO-100)



Top View

Maximum Power Dissipation



MH0009 DC Coupled Two Phase MOS Clock Driver

Absolute Maximum Ratings

V^- Supply Voltage: Differential (Pin 5 to Pin 3) or (Pin 5 to Pin 7)	−40V
V^+ Supply Voltage Differential (Pin 11 to Pin 5)	30V
Input Current (Pin 2, 4, or 8)	±75mA
Peak Output Current	±500mA
Power Dissipation (Note 1 and Figure 2)	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The MH0009 is high speed, DC coupled, dual MOS clock driver designed to operate in conjunction with high speed line drivers such as the DM7830, DM5440, or DM7093. The transition from TTL/DTL to MOS logic level is accomplished by PNP input transistors which also assure accurate control of the output pulse width.

Features

- DC logically controlled operation
- Output swings to 30V
- Output currents in excess of ±500mA
- High rep rate in excess of 2 MHz
- Low standby power

RETS0009G, Rev 0 (Teradyne W-301)

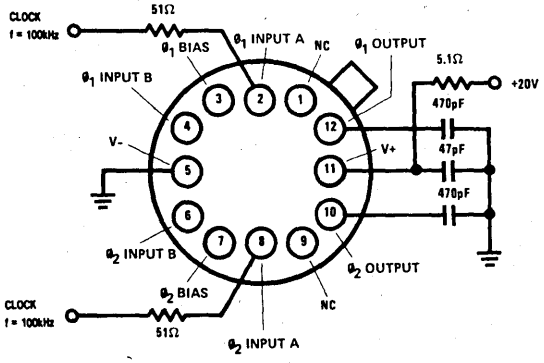
Parameter	Conditions (Note 2)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	(Note 4) Δ Limit (25°C)	Units
Input A Input Voltage ($V_{IN}A$)	I_{IN} = 500μA, V_{BIAS} = 0	.2	.3						V
	I_{IN} = 3mA, V_{BIAS} = 0	.2	.99						V
Bias Input Voltage (V_{IB})	I_{BIAS} = 3mA, $V_{IN}(A)$ = 0	.6	.99						V
Bias Input Current (I_{IB})	V_{BIAS} = 45V, V^- = 0		8.0					±1.0	μA
Input B Input Voltage ($V_{IN}B$)	I_{IN} = 1mA, V^- = 0	.16	.26						V
	I_{IN} = 10mA, V^- = 0	.6	.99						V
Negative Supply Voltage (I_{CC}^-)	I^- = 10mA, $V_{IN}(B)$ = 0	.6	.99						V
Output Voltage (V_{OUT})	V^- = 0, $I_{IN}(B)$ = 8mA, I_{OUT} = 50mA		1.8						V
	V^- = 0, $I_{IN}(B)$ = 8mA, I_{OUT} = 10mA	.6							V
Output Current (I_{OUT})	V^- = 0, $I_{IN}(B)$ = 1mA, V_{OUT} = 35V		50						μA
Positive Supply Voltage (I_{CC}^+)	I^+ = 50mA, V_{OUT} = 0		3.5						V
	I^+ = 10mA, V_{OUT} = 0	.6							V
Turn-On Time (Note 3) (t_{ON})	V^+ = 0, V^- = 20V, C_{IN} = .0022μF, C_L = .001μF		35		35		35		ns
Rise Time (Note 3) (t_r)	V^+ = 0, V^- = 20V, C_{IN} = .0022μF, C_L = .001μF		50		50		50		ns
Fall Time (Note 3) (t_f)	V^+ = 0, V^- = 20V, C_{IN} = .0022μF, C_L = .001μF		120		120		120		ns
Pulse Width (50% to 50%) (Note 3) (t_{pw})	V^+ = 0, V^- = 20V, C_{IN} = .0022μF, C_L = .001μF	340	440	340	440	340	440		ns
	V^+ = 0, V^- = 20V, C_{IN} = 600pF, C_L = 200pF	40	120	40	120	40	120		ns

Notes:

1. Transient power is given by $P = fC_L(V^+ - V^-)^2$ watts, where f = repetition rate, C_L = load capacitance, and $(V^+ - V^-)$ = output swing.
2. All unspecified pins are open.
3. Guaranteed parameter, no testing available.
4. Class S only.

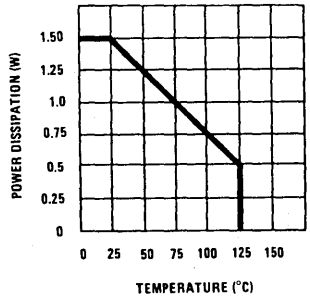
Burn-In Circuit

Metal Can Package
(12-Lead TO-8)



Top View

Maximum Power Dissipation



MH0012 High Speed MOS Clock Driver

Absolute Maximum Ratings

V^- Supply Voltage: Differential (Pin 1 or 2 to Pin 5)	−40V
V^+ Supply Voltage: Differential (Pin 8 or 9 to Pin 1 or 2)	30V
Input Current (Pin 3 or 7)	+75mA
Peak Output Current	+1000mA
Maximum Output Load—See Figure 2	
Power Dissipation—See Figure 1	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

General Description

The MH0012 is a high performance clock driver that is designed to be driven by the DM7830 or other line drivers or buffers with high output current capability. It will provide a fixed width pulse suitable for driving MOS shift registers and other clocked MOS devices.

Features

- High output voltage swings — 12 to 30 volts
- High output current drive capability — 1000mA peak
- High repetition rate — 10MHz at 18 volts into 100pF
- Low standby power — less than 30mW

RETS0012G, Rev OA (Teradyne W-301)

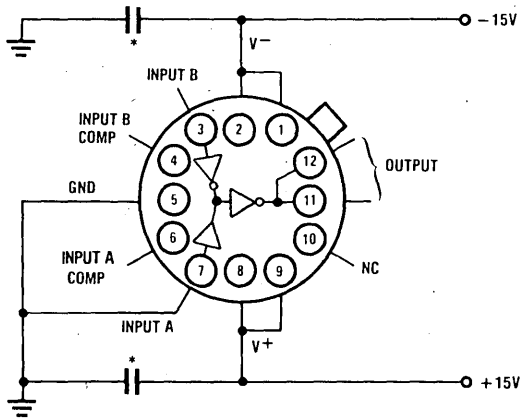
Parameter	Conditions (Note 1)	+25°C Min	+25°C Max	+125°C Min	+125°C Max	−55°C Min	−55°C Max	Δ Limit (25°C)	Units
Logical "1" Input Voltage (Note 2) (V_{IH})	V_{OUT} < 2V		2.0		2.0		2.0		V
Logical "0" Input Voltage (Note 2) (V_{IL})	V_{OUT} > 18.5V	0.4		0.4		0.4			V
Logical "1" Output Voltage (V_{OH})	I_{OUT} = −1mA	8.5		8.5		8.5			V
Logical "0" Output Voltage (V_{OL})	I_{OUT} = 1mA		−8.0		−8.0		−8.0		V
Negative Supply Current (I_{CC}^-)	V_{IN} = 1.5V		−60		−60		−60		mA
Turn-On Delay (Note 3) (t_{ON})	V_{IN} = 5V, C_L = 200pF, f = 1MHz		15						ns
Rise Time (Note 3) (t_r)	V_{IN} = 5V, C_L = 200pF, f = 1MHz		10						ns
Turn-Off Delay (Note 3) (t_{OFF})	V_{IN} = 5V, C_L = 200pF, f = 1MHz		50						ns
Fall Time (Note 3) (t_f)	V_{IN} = 5V, C_L = 200pF, f = 1MHz		45						ns

Notes:

1. V^+ = 10V, V^- = −10V, pin 5 grounded, input compensation = 40pF unless otherwise specified.
2. Tested go-no-go only.
3. Guaranteed parameter.

Burn-In Circuit

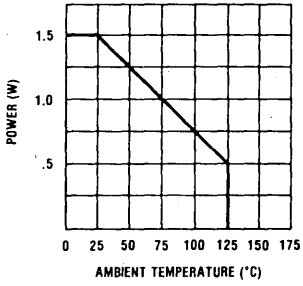
Metal Can Package



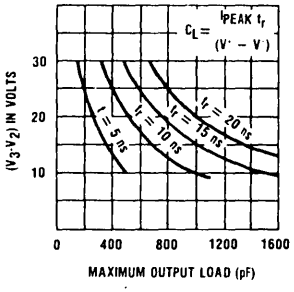
Top View

Note: * All capacitors are .1μF every five sockets.

Power Dissipation



Maximum Output Load vs Voltage Swing vs Rise Times



MH0013 Two Phase MOS Clock Driver

Absolute Maximum Ratings

(V — V) Voltage Differential	30V
Input Current (Pin 2, 4, 6 or 8)	±75mA
Peak Output Current	±600mA
Power Dissipation (Figure 2)	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 sec 1/16" from Case)	300°C

General Description

The MH0013 is a general purpose clock driver that is designed to be driven by DTL or TTL line drivers or buffers with high output current capability. It will provide fixed width clock pulses for both high threshold and low threshold MOS devices. Two external input coupling capacitors set the pulse width maximum, below which the output pulse width will closely follow the input pulse width or logic control of output pulse width may be obtained by using larger value input capacitors and no input resistors.

Features

- High output voltage swings — up to 30V
- High output current drive capability — up to 500mA
- High repetition rate — up to 50MHz
- Pin compatible with the MH0009
- "Zero" quiescent power

RETS0013G, Rev 0B (Teradyne W-301)

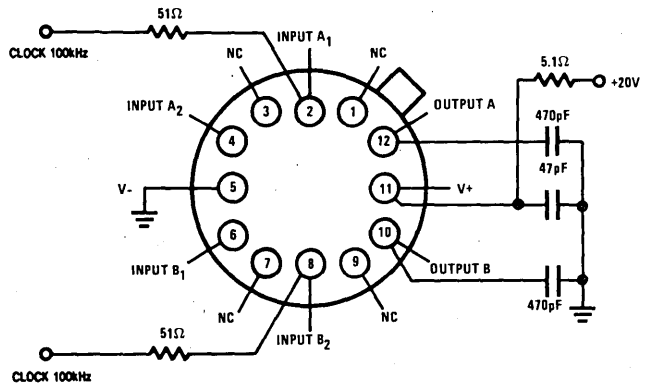
Parameter	Conditions	+25°C Min	+25°C Max	(Note 4) +125°C Min	(Note 4) +125°C Max	(Note 4) −55°C Min	(Note 4) −55°C Max	Δ Limit (25°C)	Units
Negative Input Clamping Voltage (V_{IC}^-)	I_{IN} = −10mA	−1.2	−0.6	−1.2	−0.6	−1.2	−0.6		V
Power Supply Leakage Current (I_{CC})	$V^+ - V^-$ = 30V, $I_{IN} = I_{OUT}$ = 0		100		100		100		μA
Logical "0" Output Voltage (V_{OL})	I_{IN} = 1mA, I_{OUT} = −50mA, V^+ = 0, V^- = −20V	$V^+ - 3$		$V^+ - 3$		$V^+ - 3$			V
	I_{IN} = 1mA, I_{OUT} = −10mA, V^+ = 0, V^- = −20V	$V^+ - 3$	$V^+ - .6$	$V^+ - 3$	$V^+ - .6$	$V^+ - 3$	$V^+ - .6$		V
Logical "1" Output Voltage (V_{OH})	I_{IN} = 10mA, I_{OUT} = 50mA, V^+ = 0, V^- = −20V		$V^+ - 2$		$V^+ - 2$		$V^+ - 2$		V
Turn-on Time (Note 1) (t_{ON})	C_{IN} = .0022μF, R_{IN} = 0, C_L = .001μF		35		35		35		ns
Rise Time (Note 1) (t_r)	C_{IN} = .0022μF, R_{IN} = 0, C_L = .001μF		50		50		50		ns
Fall Time (Notes 1, 2) (t_f)	C_{IN} = .0022μF, R_{IN} = 0, C_L = .001μF	40	80						ns
Fall Time (Notes 1, 3) (t_f)	C_{IN} = .0022μF, R_{IN} = 0, C_L = .001μF	40	120						ns
Pulse Width (Notes 1, 3) (t_{pw})	C_{IN} = .0022μF, R_{IN} = 0, C_L = .001μF	340	470						ns
Turn-Off Time (Notes 1, 2)	C_{IN} = .0022μF, R_{IN} = 0, C_L = .001μF		60						ns

Notes:

1. AC parameters are guaranteed.
2. Parameter values apply for clock pulse width determined by input pulse width.
3. Parameter values apply for input pulse width greater than output clock pulse width.
4. Temperature limits are guaranteed.

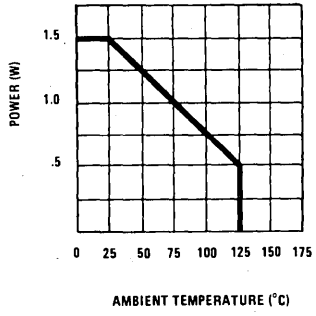
Burn-In Circuit

Metal Can Package
(12-Lead TO-8)



Top View

Package Power Derating



Section 17

Application Notes

Application of the LH0002 Current Amplifier

National Semiconductor
Application Note 13

INTRODUCTION

The LH0002 Current Amplifier integrated building block provides a wide band unity gain amplifier capable of providing peak currents of up to ±200 mA into a 50 ohm load.

The circuit uses thick film technology to integrate 2 NPN and 2 PNP complementary matched silicon transistors with 4 cermet resistors on a single alumina ceramic substrate. A circuit schematic is shown in Figure 1. The negative thermal feedback provided by the close proximity of the components on a single substrate eliminates any thermal runaway problem that could occur if this circuit were constructed using discrete components.

A typical circuit features a dynamic input impedance of 200 Kohms, an output impedance of 6 ohms, DC to 50 MHz bandwidth, and an output voltage swing that approaches supply voltage. A complete list of the guaranteed and typical values for the electrical characteristics under the stated conditions is given in Table 1. These features make the LH0002 ideal for integration with an operational amplifier inside a closed loop configuration

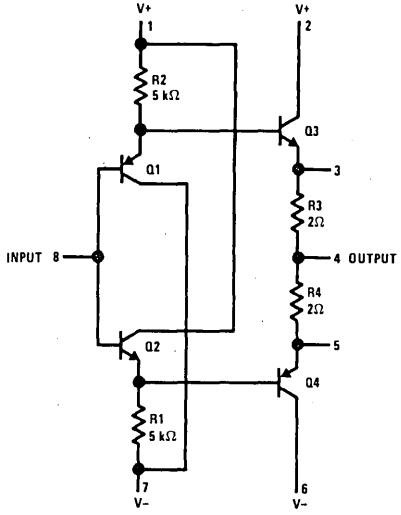


FIGURE 1. Circuit Schematic

TABLE 1. Electrical characteristics, specification applies for T_A = 25°C with +12.0V on pins 1 and 2; −12.0V on pins 6 and 7.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain	R_S = 10 kΩ, R_L = 1.0 kΩ V_{IN} = 3.0 V_{PP}, f = 1.0 kHz T_A = −55°C to 125°C	.95	.97		
Input Impedance	R_S = 200 kΩ, V_{IN} = 1.0 V_{rms}, f = 1.0 kHz, R_L = 1.0 kΩ	180	200	–	kΩ
Output Impedance	V_{IN} = 1.0 V_{rms}, f = 1.0 kHz R_L = 50Ω, R_S = 10 kΩ	–	6	10	Ω
Output Voltage Swing	R_L = 1.0 kΩ, f = 1.0 kHz	±10	±11	–	V
DC Input Offset Voltage	R_S = 10 kΩ, R_L = 1.0 kΩ T_A = −55°C to 125°C	–	±40	±100	mV
DC Input Offset Current	R_S = 10 kΩ, R_L = 1.0 kΩ T_A = −55°C to 125°C	–	±6.0	±10	μA
Harmonic Distortion	V_{IN} = 5.0 V_{rms}, f = 1.0 kHz	–	0.1	–	%
Bandwidth	V_{IN} = 1.0 V_{rms}, R_L = 50Ω, f = 1 MHz	30	50	–	MHz
Positive Supply Current	R_S = 10 kΩ, R_L = 1 kΩ	–	+6.0	+10.0	mA
Negative Supply Current	R_S = 10 kΩ, R_L = 1 kΩ	–	−6.0	−10.0	mA

to increase its current output. The symmetrical class B output portion of the circuit also provides a constant low output impedance for both the positive and negative slopes of output pulses.

CIRCUIT OPERATION

The majority of circuit applications will use symmetrical power supplies, with equal positive voltage being applied to pins 1 and 2, and equal negative voltage applied to pins 6 and 7. The reason that pin 2 and pin 6 are not connected internally to pin 1 and pin 7, respectively, is to increase the versatility of circuit operation by allowing a decreased voltage to be applied to pins 2 and 6 to minimize the power dissipation in Q3 and Q4. The larger voltage applied to the input stage also provides increased current drive as required to the output stage.

The operation of the circuit can be understood by considering that the input pin 8 is at V_{IN}. The emitter of Q1 will be approximately 0.6 volt more positive than V_{IN} at 25°C, and the converse is true for Q2. This 0.6 volt will provide a forward bias on Q3 to cancel out the Q1 base to emitter drop which in turn would provide V_{IN} at the output if all junctions, resistors, power supplies, etc., were electrically identical. The greatest error is introduced because the forward drops in the base-emitter junctions for the NPN and PNP devices are slightly different. For example, the V_{BE} of the NPN will be typically 0.6V and the V_{BE} of the PNP will be typically 0.64V under the same conditions of I_C = 2.4 mA at V_{CE} = 12.0V at 25°C. These are the approximate input stage circuit conditions for Q1 and Q2 for plus and minus 12V supplies. Fortunately, this error in both input and output offset voltage is almost always negligible when it is used inside the closed loop of a high gain operational amplifier.

A plot of input impedance vs frequency is shown in Figure 2. Inspection of this plot shows that the input impedance can be closely approximated to that of a simple first order linear network with a 45° phase lag at 0.6 MHz and a 90° phase lag at approximately one decade higher in frequency. This information is very useful for designers who have to integrate circuits which have large source

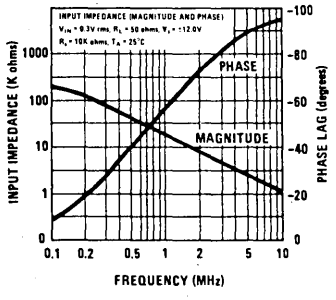


FIGURE 2. Input Impedance vs Frequency

impedances over a wide frequency range. The output impedance of the amplifier is very low, 6 ohms typically, and in conjunction with a voltage bandwidth of approximately 50 MHz can be considered to be insignificant for most applications for this type of device.

A plot of the voltage bandwidth is shown in Figure 3. Inspection of this plot shows that phase information as well as gain information was included to assist users of this device. For example, at 10 MHz, less than an 8° phase lag would be subtracted from the phase margin of an operational amplifier when it is integrated with this device. The open loop gain of the operational amplifier would be decreased by less than 10% at 10 MHz and therefore can be considered to be insignificant for most applications.

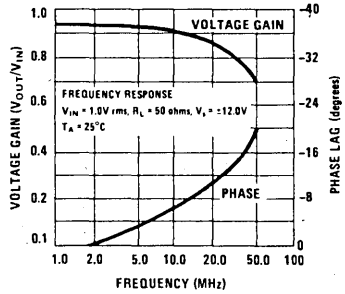


FIGURE 3. Frequency Response

APPLICATIONS

Figure 4 shows the LH0002 integrated with the LH0005 to provide differential inputs and outputs. In order for this circuit to funtion properly, a load must be floated between the outputs of the two devices to provide a complete loop of feedback. A differential head on a scope across the load presents a true waveform of the actual signal being applied to it. If only one end of the load is displayed, it will appear distorted because this information is being fed back negatively to the input in order to cancel out the loop distortion of the overall amplifier. With the compensation shown, a 20V peak to peak signal can be applied to a 100 ohm load to 80 KHz. The overall circuit is approximately 33% efficient under these conditions. A derating factor and/or heat sink must be used at higher temperatures, as shown by the LH0002 and LH0005 data sheets.

Additional output power could also be obtained by connecting another LH0002 to pin 9 of the operational amplifier. The overall load distortion under high circuit voltage gain configurations would also be reduced using two LH0002's because the LH0002 is more linear than the simple output circuits of these particular operational amplifiers.

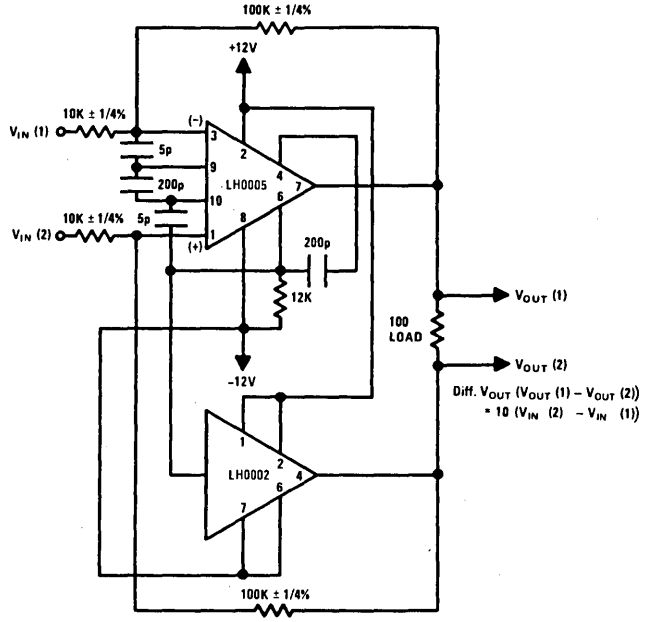


FIGURE 4. Differential Input-Output Operational Amplifier Integration

Figure 5 shows the LH0002 integrated with the LH101 in a booster follower configuration. The configuration is stable without the requirement for any external compensation; however, it would behoove the designer to be conservative and bypass both the negative and positive power supplies with at least a 0.01 μf capacitor to cancel out any power supply lead inductance. A 100 ohm damping resistor, located right at the input of the LH0002, might also be required between the operational amplifier and the booster amplifier. The physical layout will determine the requirement for this type of oscillation suppression. Current limiting can be added by incorporating series resistors from pins 2 and 6 to their respective power supplies. The exact value would be a function of power supply voltage and required operating temperature.

A breadboard of this configuration was assembled to empirically check the increase in offset voltage due to the addition of the LH0002. The offset voltage was measured with and without an LH0002 inside the loop with a voltage gain of 100, at –55°C, 25°C and 125°C. The additional offset voltage was less than 0.3% for all three temperature conditions even though the offset voltage of the LH0002 is much higher than that of the LH101. The high open loop gain of the LH101 divides out this source of circuit error. The integration of this device also allows higher closed loop circuit gain without excessive cross-over distortion than would be obtainable with the simple booster amplifier shown in Figure 6.

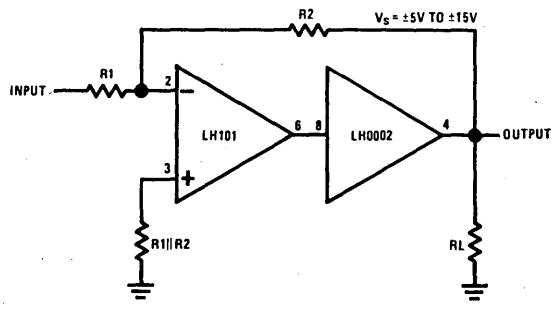


FIGURE 5. LH101-LH0002 Booster Amplifier Integration.

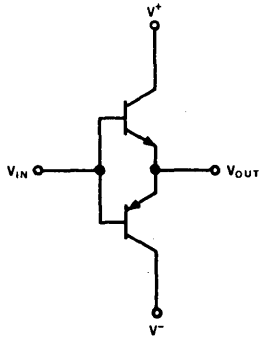


FIGURE 6. Simple Booster Amplifier

Figure 7 shows the LH0002 being used as a level shifter with a high pass filter on the input in order to reference the output to zero quiescent volts. The purpose of the 10 Kohm resistor is to provide current bias to the circuit's input transistors to reduce the output offset voltage. Figure 3, Input Impedance vs Frequency, provides a useful design aid in order to determine the value of the capacitor for the particular application. The 10 Kohm resistor, of course, has to be considered as being in parallel with the circuit's input impedance.

For a pulse input signal, the output impedance of the circuit remains low for both the positive and negative portions of the output pulse. This circuit provides both fast rise and fall times for pulse signals, even with capacitive loading. The LH0002 data sheet shows typical rise and fall times for both positive and negative pulses into a 50 ohm load.

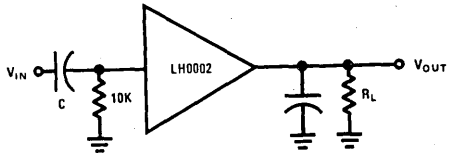


FIGURE 7. Level Shifter

Figure 8 shows the LH0002 being used to drive a pulse-transformer. The low output offset voltage allows the pulse transformer to be directly coupled to the amplifier without using a coupling capacitor to prevent saturation. The pulse transformer can be used to change the amplitude and impedance level of the pulse, the polarity of the pulses, or, with the aid of a center-tapped winding, positive and negative pulses simultaneously.

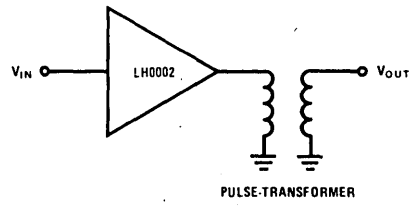


FIGURE 8. Driver for a Pulse-Transformer

The LH0002 can also be used to drive long transmission lines. Figure 9 shows a circuit configuration to match the output impedance of the amplifier to the load and coaxial cable for proper line termination to minimize reflections. A capacitor can be added to empirically adjust the time response of the waveform.

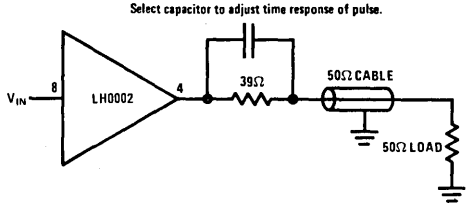


FIGURE 9. Transmission Line Driver

SUMMARY

The multitude of different applications suggested in this article shows the versatility of the LH0002. The applications specially covered were for a differential input-output operational amplifier, booster amplifier, level shifter, driver for a pulse-transformer, and transmission line driver.

High-Speed MOS Commutators

National Semiconductor
Application Note 28
Dale Mrazek

Speed and accuracy of MOS analog commutators are being improved sharply by techniques initially developed to make large-scale MOS digital integrated circuits compatible with bipolar logic circuits. Now, TTL logic can drive an MOS commutator at rates up to 20 MHz, with signal accuracies better than 90%. And at lower frequencies, accuracies very close to 100% can be achieved.

In the past, MOS monolithic commutators and multiplexers were recommended for precision analog switching only at relatively low rates, on the order of 10 kHz. Commutation at higher rates was considered risky because of large noise transients produced by the MOS switching transistors. Considerable time had to be allowed for the transients to settle down before the signal could be sampled accurately.

Transient noises have been reduced to at least half their former level by processes that lower the switching-voltage threshold of the MOS transistors. The processes also cut impedance and leakage current, permitting low-impedance designs that further enhance commutator performance.

Although they switch analog voltages, the MOS field-effect transistors in these commutators can be interfaced with logic ICs almost as readily as low-voltage MOS ICs. Either MOS or bipolar logic can control the MOSFET gate voltages. Only a few volts change in the gate voltage will turn the MOSFETs on or off.

Examples of new multichannel designs for analog/digital data-gathering applications are shown in Figures 1 and 2. Circuit impedances have been optimized in each so that commutation rates are much higher than the normal 200 to 500 kHz rate of low-voltage MOS commutators (rates, incidentally, about twice as high as the maximum rates of high-threshold commutators). The all-MOS system in Figure 1 operates at 1 MHz, while the MOS/TTL system in Figure 2 achieves 20 MHz.

LOWERING THRESHOLD VOLTAGES

Reducing the MOSFET switching-threshold voltage, V_{TH}, improves most of the characteristics that affect commutator performance. Chief result is a reduction in the gate-voltage change needed to

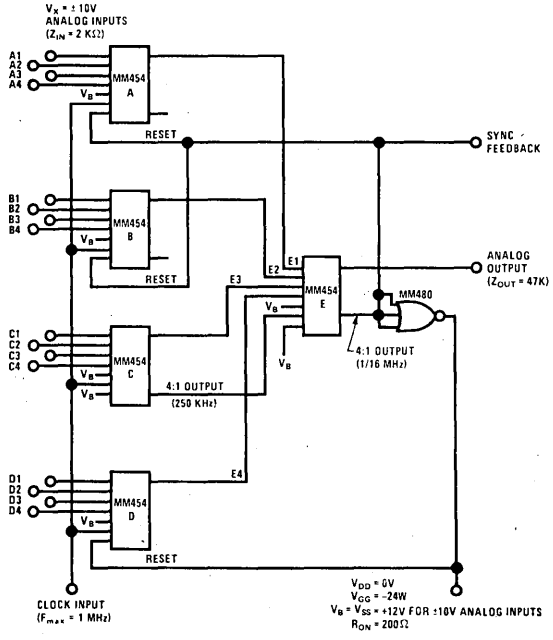


FIGURE 1. All-MOS 1-MHz Multiplexer or Commutator

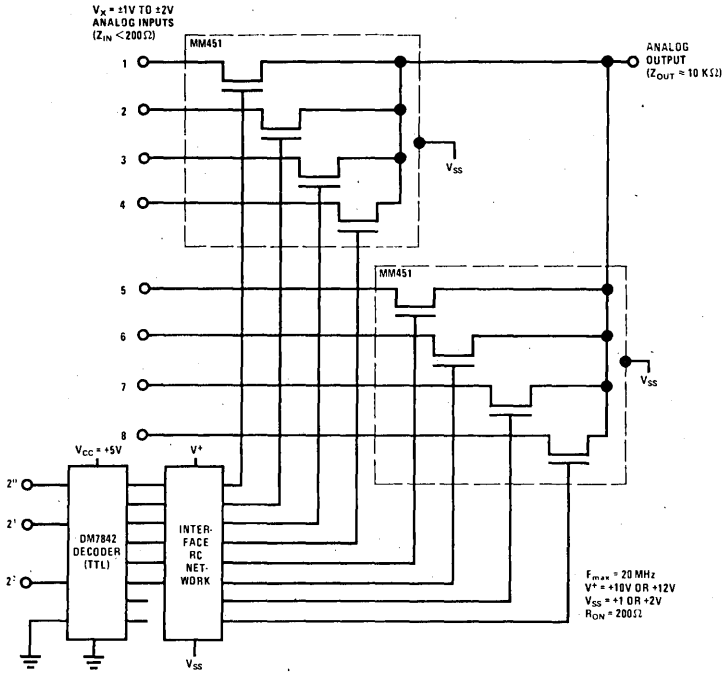


FIGURE 2. Hybrid MOS/TTL 20-MHz Commutator for Low-Level Signals

switch the MOSFET on and off. In turn, switching times and the noise transients and circuit impedances that produce signal errors can all be reduced. The benefits of lowering V_{TH} are additive, particularly in multichannel commutators. The signal may go through several switches in series.

The importance of the threshold voltage is illustrated in Figure 3, which shows schematically the operation of a p-channel enhancement type of MOSFET (the basic element of most MOS integrated circuits). It conducts when the gate voltage is more negative than the potential of the source and the bulk semiconductor substrate V_{SS} by at least V_{TH}. The oxide under the gate electrode acts as the dielectric of a capacitor. The electric field applied to the gate electrode cause holes (absence of electrons) to appear in the channel region starting from the source. The n-type silicon there is converted to p-type, eliminating the p-n diode junctions that had blocked current flow between source and drain (the source is the most positive terminal). V_{TH} is the bias at which the layer of intrinsic semiconductor, with no surplus of electrons or holes, and the p-channel reach the drain diffusion. Conduction begins at this point and increases as V_G goes more negative than V_{TH} (that is, when the gate-to-source voltage $-V_{GS}$ is more than V_{TH}).

The (1-0-0) silicon process described in the appendix produces MOSFETs whose V_{TH} is 1.8 to 2.5 volts when there is no bias between bulk (substrate) and source (V_{BS} = 0). In comparison, a conventional MOSFET made with (1-1-1) silicon has a V_{TH} of about 4V. Practical MOS circuits do have some V_{BS} bias and usually some additional signal voltage at the source, which raise the working value of V_{TH}. As the typical V_{TH} curves in Figure 4 show, the threshold of a device rises with V_{BS}.

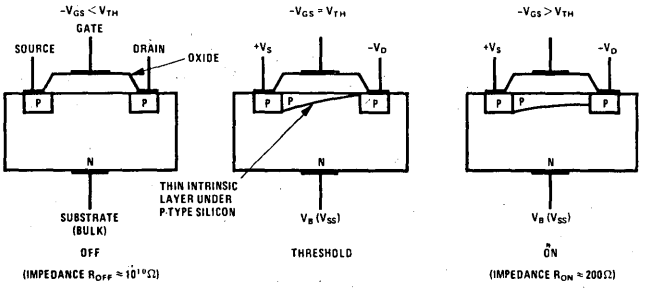


FIGURE 3. Channel Enhancement in MOS Transistors (P Channel)

A general equation describing these relationships is

$$V_{TH} = -K\left[\pm(2\phi_F + V_{BG})\right]^{1/2} + V_{SS}$$

where K is a device constant (usually 0.8 to 1.2) and $\pm 2\phi_F$ is the zero-bias threshold. This equation produces curves such as those in Figure 4.

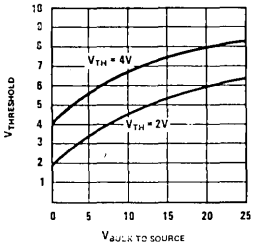


FIGURE 4. Typical Threshold-Voltage Curves

The MOSFET equivalent circuit (Figure 5) offers further insight into the importance of lowering V_{TH}. The smaller change in V_G means that smaller transient voltages will appear at source and drain. The transients are caused by charging and discharging of the capacitances. The time required to change V_G and the duration of the transients will be smaller, too. The value of R_{ON}, the MOSFET's impedance while conducting, will also be less at any given value of V_G more negative than V_{TH}. Any reduction in R_{ON} will make V_{OUT} more nearly equal to V_{IN}. The accuracy of an analog switch is determined by the ratio V_{OUT}/V_{IN}.

CONTROL VOLTAGES

Signal voltage V_X often varies between positive and negative values in commutator applications. To make certain that the MOSFET switches on under all signal conditions, V_G must swing from at least V_X to $(V_{SS}-V_{TH}-\Delta V-VX)$, where $\pm V_X$ are the signal limits and ΔV is the overdrive needed to lower the switch's series resistance to the desired level (mainly, reduction in R_{ON} obtained by making $-V_{GS}$ more negative).

If the signal range is fairly wide, say ±10V, the gate voltage of a MOSFET with a 4V to 6V threshold must swing from +10V to about -26V for accurate commutation. In contrast, a 2V threshold makes the necessary swing only from +10V to about -20V. The difference becomes more significant at lower signal voltages. At $V_X = \pm 1V$, for instance, the high V_{TH} device requires a swing from at least +1V to -10V, while the low V_{TH} device does the job with +1V to -6V — about a third less. High-speed, low-impedance TTL gates can control a commutator in the latter voltage range, as shown in Figure 2, because such small transitions can be made very rapidly. They are close enough to bipolar logic transitions for the use of simple, high-speed TTL-to-MOS interfaces.

Multichannel switches made with (1-0-0) silicon typically operate with a maximum change in control voltage of from +14V to -30V, which permits $V_X = \pm 14V$. Relatively few practical applications require so large a swing. If larger signal voltage must be handled, it would be cheaper to use a scaler than to pay the cost of a high-voltage multiplexer with beefed-up control circuitry.

ON AND OFF RESISTANCES

For best signal accuracy and maximum switching rate, impedances should be low. The resistance of a MOSFET while on, R_{ON}, varies with signal voltage, so it cannot be compensated readily. This produces a variable error term called R_{ON} modulation.

MOS commutators are usually structured as series switches (Figure 6a). Two or more ranks of commutators are generally used, as in Figure 1, to minimize the control circuitry. The added ranks put additional MOSFETs in each signal channel and enlarge the amount and variation in R_{ON} of the conducting channel. If V_X varies, the error ratio V_{OUT}/V_{IN} tends to vary because R_{ON} is a function of the effective switching threshold which rises and falls with V_X.

There is no simple way of keeping R_{ON} constant. Usually, the effect of the variation is reduced by increasing the other impedances, but that lowers the maximum switching rate. A low-V_{TH} eases this problem greatly. All other conditions being equal, the MOSFET with the lowest V_{TH} will conduct better at any given value of V_G more negative than V_{TH}. The p-channel enhancement will be greater

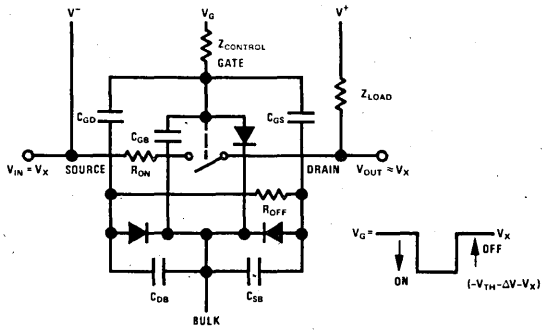


FIGURE 5. Equivalent Circuit of P-Channel MOSFET

and the channel electrically larger. Figure 6c is a typical curve of R_{ON} versus gate bias. Low-V_{TH} analog switches made with (1-0-0) silicon by National Semiconductor as integrated circuits achieve R_{ON} values comparable to those of larger, but higher-V_{TH}, discrete MOSFETs--from 250 to 300 ohms at V_X = −10V and about 100 ohms when V_X = +10V. The R_{ON} of a high-V_{TH} integrated commutator, in contrast, is typically a few hundred ohms higher and some reportedly reach a few kilohms.

To swamp out the voltage-divider effect in Figure 6b, it has been customary to make the load, R_L, much larger than the combination of R_{ON} and R_S. Output impedances in the megohm range are often used with high-V_{TH} devices. But note in Figure 2 that very low values of source and load impedance can be used with low-V_{TH} commutators. These low impedances and the very low impedance of the TTL circuit controlling the gate are two of the main reasons for this commutator's exceptionally high speed.

Source impedance is usually made equal or less than R_{ON} so that leakage currents of the turned-off MOSFETs can return to a low-impedance turned-on channel signal source. Leakage per switch is small in an integrated circuit commutator, but there are several switching devices with a common output in the same semiconductor substrate. Leakage currents could add up to a value that seriously degrades signal accuracy. In any semiconductor device, leakage increases rapidly with temperature. However, the leakage specification is so small in our commutator made with (1-0-0) silicon that they will work well up to a temperature of 125°C, while commutators made with (1-1-1) silicon have been specified for a maximum operating temperature of only 85°C.

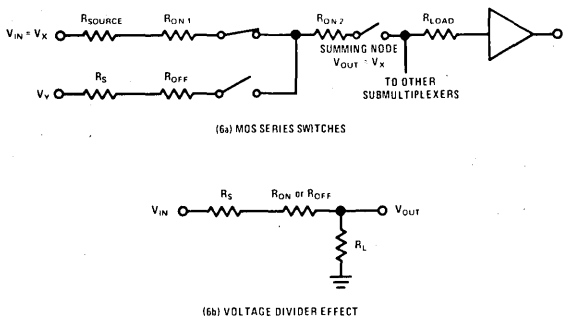
Regardless of the process, the OFF resistance, R_{OFF}, of a well-made MOSFET is generally high enough to prevent the signal in the OFF channel (channel V_Y in Figure 6a) from appearing at the output and degrading the accuracy of the signal through the on channel (V_X in the figure). R_{OFF} is usually around 10^{10} ohms. If V_Y is a high-frequency signal, there may be significant AC feedthrough, but this can be prevented by techniques to be discussed shortly.

SWITCHING SPEED AND NOISE

The absolute switching speed of a commutator is limited by the time required to charge and discharge the device capacitances. Circuit impedances affect speed by contributing to the RC time constants. However, the practical switching rate of a precision commutator depends upon the time required for the output signal to recover from the noise transients produced during the charge-discharge cycles. Low-V_{TH} processing cuts transient recovery time because the transients' duration and amplitude are reduced. Some designs make the recovery time negligible.

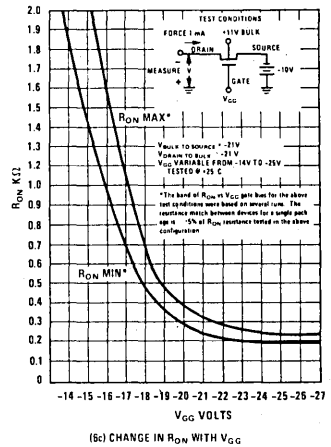
In all MOSFETs, transmission of a turn-on or turn-off signal is followed by a delay whose length depends upon the magnitude and rate of change of the gate-control voltage. At turn-on, the delay is lengthened by the RC time constant of the gate-bulk capacitance (see Figure 5) and the impedance in the control circuit. Capacitances and impedances in the signal path cause a similar delay at turn-off. As V_{GS} goes negative, turning the switch on, energy is pulled from the source and load impedances through the gate-source and gate-drain capacitances, as in the simplified equivalent circuit of Figure 7a. At turn-off, V_{GS} goes to zero volts or positive, and energy is pushed out through the same paths.

Thus, negative turn-on and positive turn-off transients appear at the summing node. The transient waveforms of low V_{TH} and high V_{TH} MOSFETs are shown simplified and superimposed in Figure 7b. The levels are typical for devices with V_{TH} = 2V and V_{TH} = 4V at V_X = ±1V. The larger gate voltages used at higher signal voltages would make durations and amplitudes proportionately larger



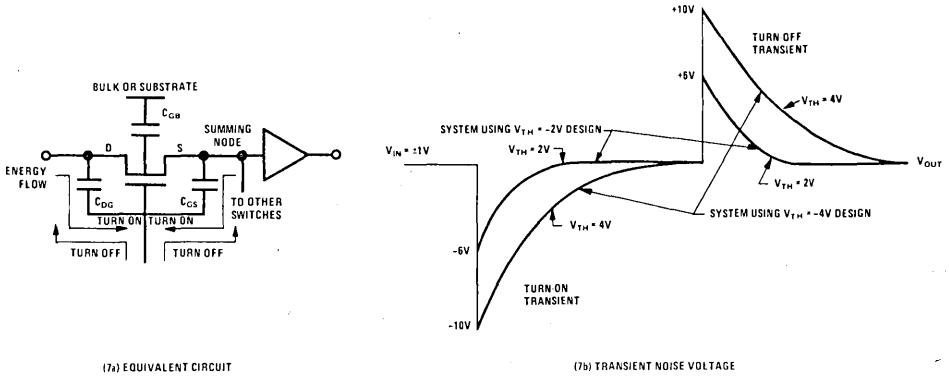
(6a) MOS SERIES SWITCHES

(6b) VOLTAGE DIVIDER EFFECT



(6c) CHANGE IN R_{ON} WITH V_{GG}

FIGURE 6. MOS Commutator Switching Impedances



(7a) EQUIVALENT CIRCUIT

(7b) TRANSIENT NOISE VOLTAGE

FIGURE 7. Transient Noise Generation

(another reason why the Figure 2 circuit is faster than the Figure 1 circuit).

The transients can be much larger than signal voltages, so even the relatively small transients of a low-V_{TH} MOSFET can saturate the buffer amplifier. One of the ways that designers of discrete commutators minimized transients at the summing node was to drive adjacent channels with coincident turn-on and turn-off signals. In this way, negative-going transients from the channels turning on will partially cancel out positive-going transients from the channels turning off. When the output amplifier is an integrator, the amounts of energy pulled through the summing node will be minimized by, in effect, being averaged out.

Coincident drive, discrete component circuits are fairly complex and expensive. Essentially the same effect is obtained in the Figure 2 commutator, at much less cost. The TTL decoder selects channels at such a high rate of speed that a channel is turning on while another channel is turning off. Transitions of the control voltage occur in less time than the turn-on and turn-off delays of the MOSFETs. So the transients are suppressed in a matter of nanoseconds. In fact, when the gate voltage is going negative or positive simultaneously, the transient is practically invisible at the output. That is, the transient actually helps change the output signal to the correct level more rapidly.

You might say that the high commutation rate makes the high commutation rate possible, but it is more pertinent to stress that the TTL decoder could not directly control a high-V_{TH} commutator. Low-impedance drivers are essential for high commutation rates, because they quickly source and sink transients. In this respect, TTL integrated circuits make almost ideal drivers.

In principle, the gate turning on and the gate turning off in a multichannel IC commutator are part of a closed-loop circuit charging the gate capacitance. The noise energy that does get into the summing node should be dissipated quickly to improve the data channel's recovery time. The energy is dissipated in the parallel combination of the summing node resistance and channel-source impedance. The RC time constant of the equivalent circuit in Figure 8 should be optimized to obtain the maximum commutation frequency.

$$F_{max} = [(R_S/R_{node})\, C_{node}]\, [(C_1 + C_2)/2C_{node}]\, [V_{G1} - V_{G0}] \text{ to } 1$$

This equation relates the time constants, gate and transient voltages and transient recovery tolerance. V_{G1} and V_{G0} are the turn-on and turn-off values of V_G; other terms are defined in Figure 8.

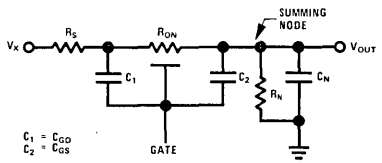


FIGURE 8. RC Network Governing Switching Frequency

HIGH-FREQUENCY NOISE CONTROL

In some cases, the analog input signal is AC rather than DC. That is, it may fluctuate rapidly between positive and negative values. This can vary the effective values of V_{SG}, R_{ON} and perhaps R_{OFF}, and may also cause spurious charging or discharging of the MOSFET capacitance. The condition results in output-voltage fluctuations due to the appearance at the summing node of signal voltages from a channel that is supposed to be off—a problem known as AC feedthrough or channel-feedthrough noise. The main cause is charge transfer through the gate-source and gate-drain capacitances of the turned-off MOSFETs.

Fortunately, most transducer voltage outputs are below 10 kHz in frequency and simply using a low-impedance gate driver prevents the problem. The transients sink into the driver rather than go to the output. A high signal source impedance would make this technique more effective, but would also cause larger transients in the turned-on channel, imposing longer recovery times and slower commutation rates.

There is a simple detour around this impasse, too. The dynamic impedance of the gate driver is allowed to approach a zero-ohm impedance when the channel is turned off (Figure 9). Theoretically, this will prevent any channel feedthrough noise at signal frequencies up to 2 MHz. In practical circuits, signal frequency is limited by load impedance, but can usually be pushed above 1 MHz. The driver impedance itself must also be low at high frequencies, of course.

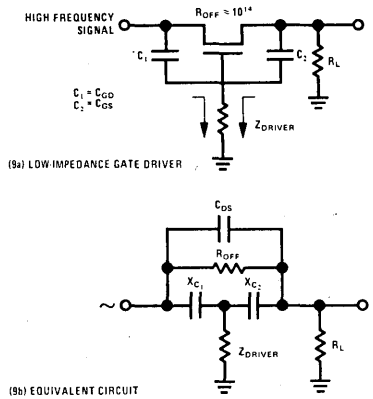


FIGURE 9. Zero-Impedance Driver Return Prevents AC Feedthrough

HIGH-SPEED SYSTEMS

All of these factors have been optimized in the Figure 2 system. At 20 MHz, its accuracy with $V_X = \pm 1V$ is nearly as good as 99%. Source and load impedance are made very low because R_{ON} is not greater than about 200 ohms per channel. The gate change is only 7V (from +1V to −6V), and the high-speed TTL control makes the transients coincide.

The 8-channel configuration shown can be the building block of very large solid-state commutators. Each 4-channel MOSFET switch is a monolithic chip (National Semiconductor MM451). The TTL channel selector is a decoder (DM7842) designed to convert 4-bit binary-coded-decimal inputs into decimal-number outputs. Only 8 outputs are needed here, so the decoder's fourth input is grounded.

The TTL outputs are translated to MOS control signals with an interface network consisting of identical passive circuits on each control line. An interface and its voltage levels are shown in Figure 10. The author used discrete components, but all 16 resistors in the network could be made as a thick-film printed circuit because the values are not large and the tolerances are not critical.

TTL logic outputs are positive, while MOSFETs require negative or positive gate biases to turn on or off. The necessary voltage changes are made with the capacitor in Figure 10.

Assume first that the TTL output is at the normal TTL logic "1" level of about 2.5V. There will be +6V across the capacitor due to R1. Since R2 is connected to +6V (V_{SS} = +1V in this system), the MOSFET gate bias will be no more negative than +1V, and that channel will be held off.

When the TTL output switches from a logic "1" to a logic "0" level, the voltage seen by the capacitor drops from +6 to about 0.4V. Bias on the gate will therefore drop from +1V to about −5V, turning the channel on. The commutator is controlled, then, by selecting the location of an "0" bit in the decoder output and making all other outputs "1".

R1 is connected to a voltage higher than +6V to assure that the TTL output rises rapidly during a transition from logic "0" to logic "1". This is needed for quick, clean turnoff of a channel (a similar technique of interfacing TTL and low-V_{TH} MOS digital circuits enables the MOS circuits to operate at about twice the normal MOS rate). The opposite transition, to the more negative level, is normally quite fast and is assisted by the excellent current-sinking capability of TTL.

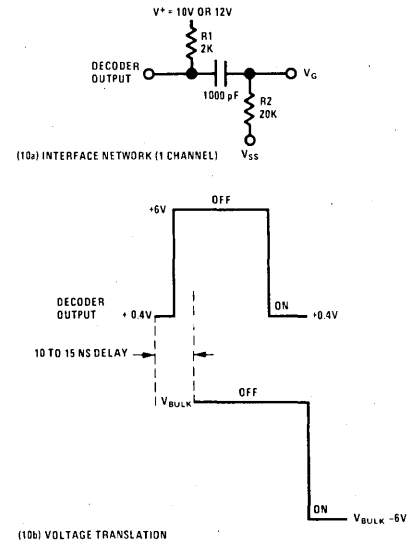


FIGURE 10. High-Speed TTL-to-MOS Control Interface

Care must be taken to select TTL drivers that do not break down when their outputs are pulled up to +10V or +12V. The DM7842 has a diode in the

output stage that protects the output transistor at high voltages, and other devices in the National TTL family have similar output stages. These are equivalent to Series 54 TTL. Suitable TTL control logic can be assembled from other ICs, but the DM7842 is convenient because only one driver chip is needed for every eight channels in the commutator system.

There is a delay of 10 to 15 nanoseconds between a transition in the TTL output and the switching of a channel on or off, mainly due to the RC time constant of the RC interface. However, the delay occurs equally on all channels and does not affect the commutation rate or significantly reduce the 50 ns sampling time permitted by a 20 MHz rate. Commutator output can be kept synchronized to any following data processing subsystem by putting a comparable delay in the line from the system clock to the processor.

The MM451 chip is also available with a DTL monolithic driver in a flatpack. This hybrid IC, the MH453, does not require an external interface network. It will operate at frequencies to 500 kHz and switch analog signals of ±10V under direct control of TTL or DTL logic. The four MOSFETs of the MM451 are connected in a dual differential configuration, useful for combining and comparing signal voltages.

ALL-MOS COMMUTATORS

Commutators built entirely of MOS devices need not be limited to low-frequency operation, despite their larger voltage swings and transients. The system in Figure 2 has better than 99% accuracy at 1 MHz with V_X = ±10V when the previously discussed characteristics of low-V_{TH} devices in this signal range are optimized.

Similar systems, optimized for smaller signal-voltage ranges, have not been built by the author but it is reasonable to expect higher frequencies or accuracies in such systems. Accuracy, of course, would be further improved by operating the optimized designs at lower than their maximum frequency. Longer recovery times would be permitted.

Each of the MM454 4-channel commutators contains four MOSFETs like those in the MM451 and, in the same chip, a 2-bit MOS counter and decoder for channel selection and all-channel blanking (Figure 11).

As shown, the system samples the 16 channels sequentially, much like a rotary driven mechanical commutator. The MM454 is designed as a building block for large sequential sampling systems. However, any particular channel could be selected with external output-gating logic. If random channel selection were the normal operating mode, the MM451 and external selection logic can be used. Two ranks of commutators, similar to Figure 1, simplify the control logic. For example, one gate driver would turn on channels A1, B1, C1 and D1, and a second driver would select channel A1 by turning on channel E1—which takes a lot less control circuitry than selecting 1 out of 16 channels directly and requires only one more monolithic commutator.

Either way, a very critical system design requirement is to guarantee that only the selected channel conducts during the sampling interval. The single 3-input NOR gate in Figure 1 accomplishes that. Commutator C is used as the master element. It divides down the 1 MHz clock signal through a 4:1 countdown circuit, which is provided in the MM454 to facilitate submultiplexing. Commutator E's four channels therefore sequence at a 250 kHz rate. Meanwhile, the four channels in commutators A, B, C and D are each sequencing at 1 MHz. The analog sequences through A1, A2, A3 and A4 in order when E1 is on, B1 through B4 when E2 is on, and so forth.

The 4:1 count-down output of commutator E (1/16 MHz) is fed back through the NOR gate to the reset inputs of commutators A, B and D. The reset every cycle keeps them in step with commu-

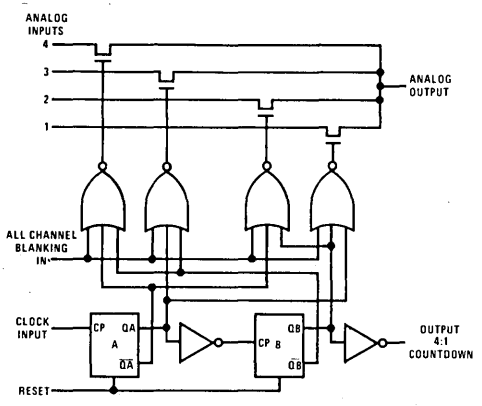


FIGURE 11. MM454 Four-Channel MOS Submultiplexer

tator C and therefore commutator E. The NOR gate's output also can be used to maintain synchronization of the commutator with other signal processing systems.

ANALOG/DIGITAL SYSTEMS

Techniques developed, and being developed, to directly couple bipolar and large-scale MOS digital circuits also depend heavily upon the lowering of threshold voltages. A report compiling and detailing coupling techniques is in preparation. In general, the ability of the MOS digital circuit to accept small, positive transitions in signal voltage, and to operate with smaller differentials in bias and gate voltages are the critical requirements for direct coupling.

Directly coupling MOS digital outputs to bipolar logic also enhances operating speed, again because impedances are lowered. Some of the high-speed TTL/MOS hybrid systems that have been developed are similar in principle to commutators, except that V_X is digital data and scores of MOSFET switching stages are used in each MOS chip. One data-storage system built by the author has achieved data transfer rates up to 16 MHz, by multiplexing high-speed bipolar data into parallel MOS storage circuits.

With all three classes of bipolar/MOS interfaces—analog/digital, logic/logic and logic/analog—now available, system designs can exploit more fully the many speed/cost tradeoffs offered by hybrid bipolar/MOS systems. Bipolar control logic and MOS large-scale storage is an extremely efficient, minimum cost combination suitable for medium-to-high-speed systems.

In other words, low-threshold processing has enabled MOS to move out of the low-frequency range and into the ranges where most modern analog/digital systems operate.

Analog-Signal Commutation

National Semiconductor
Application Note 33
Donald L. Wollesen

INTRODUCTION

Telemetry and other data-acquisition systems have become very compact and efficient, particularly when built with integrated circuits. To keep in step, small, low-power commutators are needed to multiplex large numbers of analog signals. Metal-oxide-semiconductor field-effect transistors do the job well.

MOS IC's containing several MOSFET switching channels are presently available in production quantities and perform excellently as low-level analog commutators if the system designer understands their limitations and exploits their advantages. This report will describe the DC characteristics involved in switching analog signals when the signal input range varies between −10V and +10V.

MOSFET's size up very well against earlier switching devices when their overall characteristics are considered (see Table 1 and the discussion of competitive devices). In addition to being fabricated easily as multichannel IC's—in some cases, complete with switching-control circuitry on the chip—MOSFET's have several significant electrical advantages:

- Power dissipation is essentially zero in most applications. No DC power is consumed in the control gate, and practically no signal power is dissipated in the switch.
- Offset voltage is zero in a well-designed switch.
- Resistance is reasonably low when the channel is conducting.
- Resistance of an OFF channel is practically open-circuit (R_{OFF} is on the order of 10^{12} ohms and leakage currents are very small, about 100 pA).
- Analog signals are well isolated from the switch-control signals.

With all of these things in their favor, MOS analog-switching IC's will come into much wider use, especially in large, multichannel instrumentation and data-transmission systems.

	Mechanical Switch	Bipolar Transistor	Photocell	N Junction FET	P MOS FET
"On" Resistance	$10^{-2}\Omega$	10Ω	1 KΩ	30Ω	100Ω
"Off" Leakage	10 pA	100 pA	10 nA	100 pA	100 pA
Offset Voltage	0	10^{-2}V	0	0	0
Commutation Rate	1 KHz	100 KHz	100 Hz	10 MHz	50 MHz

Table 1
Comparison of Switches

MOS IC STRUCTURE

MOS IC's generally provide four or more channels in a monolithic chip, but two are enough to illustrate the basic construction that governs switch operation. The cutaway view of Figure 1 shows two complete MOSFET's, one of which may be on while the other is off. Figure 2 is the schematic.

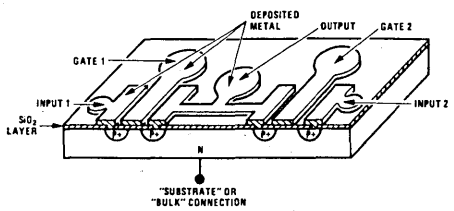


FIGURE 1. Cross-section of Two MOSFET's in an Integrated Circuit.

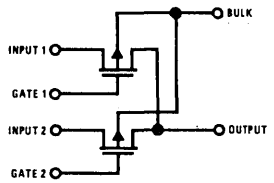
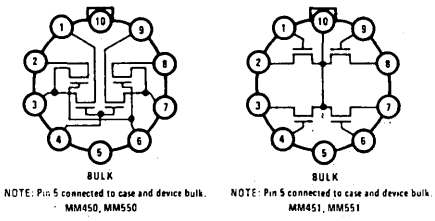


FIGURE 2. Schematic Diagram of Two-Channel Analog Switch.

Both MOSFET's have a common substrate, the "bulk" consisting of lightly doped N type silicon. Thermally grown silicon oxide covers the entire chip surface, except where the oxide was etched away to allow ohmic connections of input and output electrodes to stripes diffused with P+ dopants. These stripes are the MOSFET drain and source regions. Each gate is defined by the gate electrode, which lies over a channel region and is isolated from it by the oxide (hence, MOSFET's are sometimes called insulated-gate FET's or IGFET's).

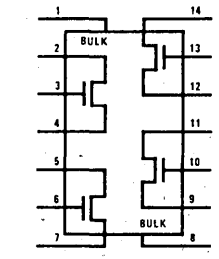
All electrodes are etched from a thin film of deposited aluminum. Each MOSFET has separate input and gate electrodes, but the output electrodes may be paired as shown, connected to a common output pin, or connected to separate output pins on the package. The same basic MOSFET

structure can be used, whether the circuit is a differential switch, a multiplexer, or independent switches in a single package (see Figure 3).



NOTE: Pin 5 connected to case and device bulk. MM450, MM550

NOTE: Pin 5 connected to case and device bulk. MM451, MM551



NOTE: Pins 1 and 8 connected to case and device bulk. MM452, MM552

FIGURE 3. Connection Diagrams of Dual Differential Switch, Four-Channel Switch and Quad MOS Transistor.

MOSFET's are, for practical purposes, bilaterally symmetrical. The drain (or source) can be either the input or output. By strict definition, the drain is the electrode to which majority-carrier current flows. The majority carriers are "holes" in the channel of P-channel MOSFET's (N-channel MOSFET's are not commonly used in MOS IC's). In most analog switching applications, the signal contains AC components, so the direction of current flow frequently alternates.

SWITCHING AND ISOLATION

A P-channel MOSFET turns on when negative voltage is applied between gate and source. The gate is biased negative with respect to the bulk. Electrons accumulate on the gate, creating positive charges in the channel region. This inverts the electric charge thus creating an "enhanced" P type channel in the n-type semiconductor. When the gate is several volts more negative than threshold, a conducting channel is formed, allowing majority carrier current (holes) to flow freely between source and drain. The channel is said to be "enhanced," so these MOSFET's are called P-channel enhancement MOSFET's.

Operating voltages in a typical switching channel are illustrated in Figure 4. In most schematics, the bulk connection would not be shown.

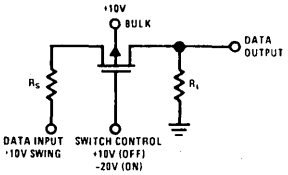


FIGURE 4. Biases on Single MOS Channel at Maximum Signal Range of ±10V.

The applied biases are those that would be used at an analog signal range of ±10V. At any signal range, the following guidelines apply:

1. Bulk bias V_{BB} must equal or be more positive than the most positive excursion of the analog signal. This bias must be maintained at all times, so is taken from a DC supply.
2. To turn the switch ON and make R_{ON} low, the voltage applied to the gate should be *at least* 5V more negative than the most negative excursion of the analog signal (10V is desirable). The actual gate voltage is V_{GG} and the gate bias is $-V_{GB}$.
3. To ensure that the switch turns OFF fully, V_{GG} should be as positive as V_{BB} making $V_{GB} = 0$.

The first rule must be followed to get good performance from the switch. With V_{BB} most positive, the p-n junctions are kept reverse-biased. When the channel is OFF, this condition isolates the drain from the source. When the switch is turned ON and the P-channel is enhanced, the drain-channel-source region is isolated by the p-n junction from the substrate because the substrate is "reverse biased" from all of these regions at all times.

The voltage across the switch, from drain to source, is caused by IR drop whether the switch is on or off. The MOS analog switch does not have any inherent offset voltage. To get $V_{out} = V_{in}$ in a MOSFET switch merely requires that load resistance R_L be much larger than the resistance in the conducting channel, R_{ON}. Since R_L is generally about 100 kilohms in most high-accuracy analog commutator applications, the requirement is easily met.

Figure 5 helps clarify rules (2) and (3). This curve shows how the gate-source threshold voltage changes with bulk-source bias voltage. Channel resistance is high and current flow at the output can only be a few microamperes. A forward bias higher than threshold is needed to enhance the channel. Making gate bias much more negative than V_{TH} at turn-ON does this. Then, at turn-OFF, the gate bias becomes more positive than V_{TH} when $V_{GG} = V_{BB}$. The channel must revert to N-type silicon thus preventing majority carrier current flow.

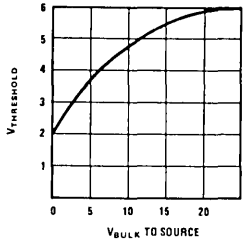
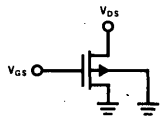


FIGURE 5. Variation in Switching-Threshold Voltage with Changes in Bulk-to-Source Bias Voltage.

The circuit designer must use biases that prevent the drain from having a positive potential when the switch is OFF. For example, V_{in} = +10V and V_{BB} = +9V should not be allowed. Operating with V_{DS} = +1V won't harm the MOSFET, but some of the signal will appear at the output. Effects of improper biasing can be seen in Figure 6. With the source and bulk grounded while V_{DS} varies, output currents at different gate biases are measured to produce the "drain family of curves." The normal family looks like Figure 6b (the drain



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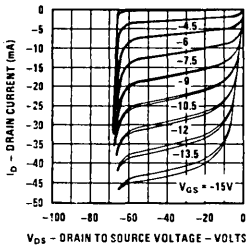
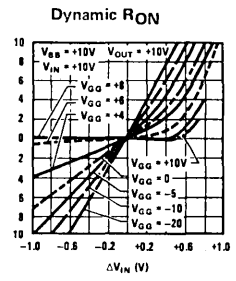


6b



6c

FIGURE 6. Drain-Current Measuring Circuit, Normal Drain Family of Curves, and "Bipolar" Drain Family of Curves.

family of National Semiconductor's MM450/MM550 MOS switching IC's). The "bipolar" family in Figure 6c shows what happens when V_{DS} is allowed to go positive.

During small excursions of V_{DS}, the MOSFET acts as a voltage-variable resistor. But when V_{DS} rises to about +0.6V, there is an abrupt increase in drain current. At this point, the diode drop is exceeded and the drain-bulk junction becomes forward biased. Minority carriers are injected into the n-type channel region, causing grounded-base pnp bipolar transistor action (note in Figure 1 that a MOSFET resembles a lateral pnp transistor in the OFF condition). Output current will be α times the input current. In most MOS devices, the amplification factor will be 0.5 to 0.9.

It is absolutely mandatory that the $V_{DS} \geq +0.6V$ be avoided. Otherwise the effective R_{OFF} will be poor and the channel will seem to have abnormally high leakage current.

Only the upper right corner of the graph in Figure 6b, detailed in the third quadrant of Figure 6c, is useful in practical circuit designs. The useful characteristics are to the right of $-V_{DS} = -1$ and above a load line at about I_D = 0.5 mA.

ON AND OFF RESISTANCE

Both R_{ON} and R_{OFF} normally vary with signal voltage and operating temperature. A positive signal voltage improves channel enhancement by making the gate more negative with respect to drain and source.

R_{ON} is minimum at the most positive signal level. It will increase slowly with temperature, since high temperatures reduce the mobility of majority carriers. Neverthless, R_{ON} will have little effect on signal quality if R_L is much larger. R_{ON} does vary nonlinearly, though, so we investigated its effect upon signal quality. Figure 7 proves that the effect

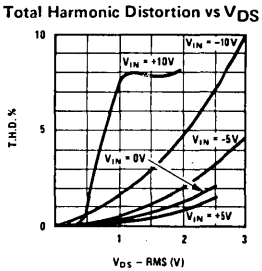


FIGURE 7. Small-Signal Harmonic Distortion (Measured with Only About 100 Ohms Load Resistance).

is negligible provided that the biasing rules are observed.

The curves of small-signal harmonic distortion in Figure 7 were measured with practically no load resistance. AC signals at various voltages were

applied to the MOSFET input and the current flow was measured at the output with the help of a 100-ohm current-sensing resistor. Distortion levels less than 0.1% could not be measured with available instruments. The anomaly in the +10V curve is due to diode distortion of the type illustrated in Figure 6c. The input signal's AC plus DC components exceeded the bulk voltage, V_{BB} = +10V, by more than the +0.6V diode drop.

The harmonic distortion is amply low for practical applications. With a 1-kilohm load, the small-signal distortion typically would be less than 0.5%, with V_{in} = ±10V and V_{DS} almost ±1V. A load of 1 kilohm is unusually small. Small signal distortion would be almost unmeasurable with a 10-kilohm load. When signal accuracy must be very high, 100 kilohms are used by some designers.

Worst-case R_{ON} can be expected at a −10V input. Figure 8 gives the change in R_{ON} of the MM450/MM550 series devices when the analog input is at +10V, 0V and −10V. If lower impedance is essential, the gate can be biased more negative. For instance, at V_{BB} = +10V, V_{GG} can be made −25V or −30V instead of −20V, increasing $-V_{GB}$ to -35V or −40V. Don't go over the specificed maximum bias, which is usually −45V, because excessive bias could reduce the device operating life.

Conversely, all biases can be reduced if the signal voltage range is less than ±10V. The gate-drive circuit will not have to swing as far, the switch can be operated faster, and switching transients will be smaller. Or, the bulk bias can be reduced and the gate bias maintained at the previous ON level. This

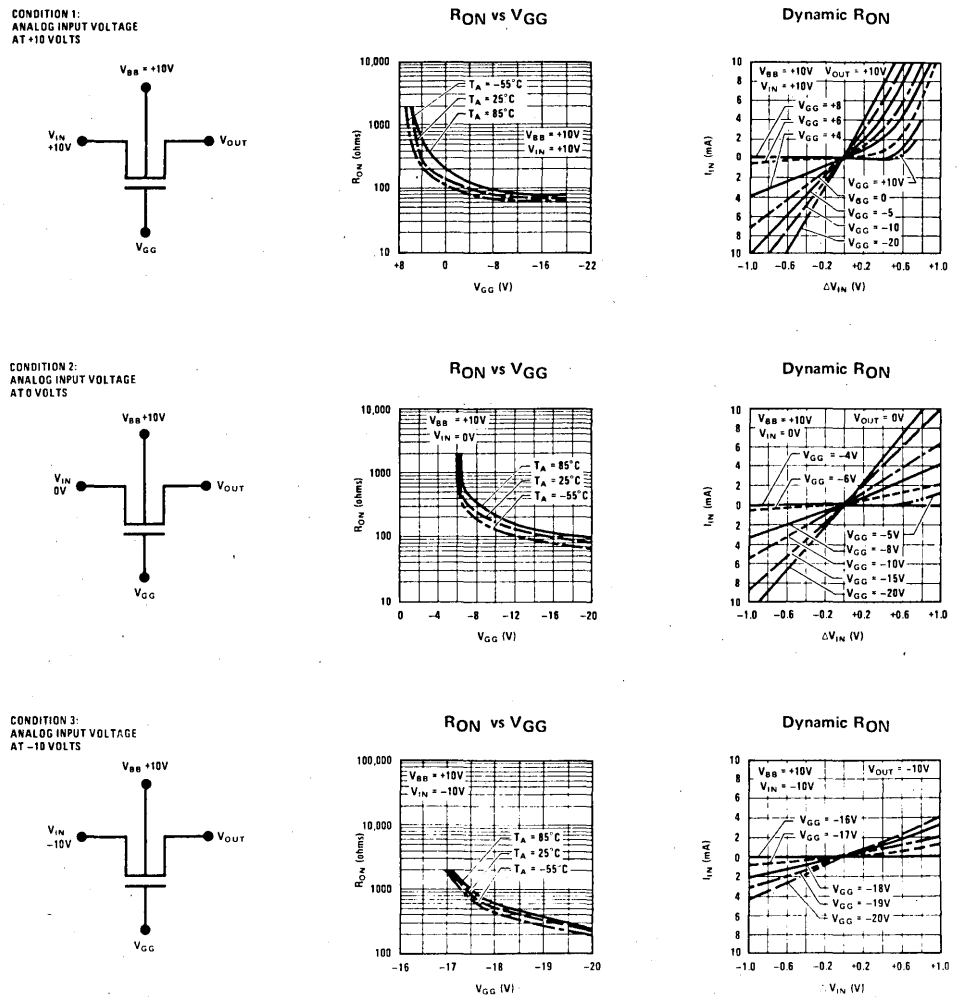


FIGURE 8. Typical R_{ON} Characteristics of MM450/MM550 MOS Devices at Most Positive, Zero and Most Negative Signal Voltages.

will give the effect shown in Figure 9—an improvement in channel enhancement and reductions in R_{ON} at the various signal levels.

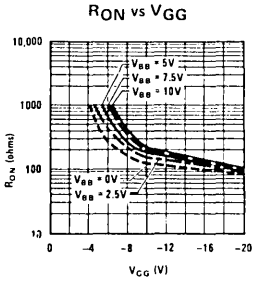


FIGURE 9. Bulk Bias Effect on R_{ON}.

When the gate is turned OFF, impedance between source and drain becomes very high ($R_{OFF} \approx 10^{12}$ ohms). A MOSFET's only significant DC conduction is leakage current. Total leakage in MM450/MM550 devices is typically less than 100 pA at 25°C. It rises more rapidly than R_{ON} with increasing temperature, approximately doubling with every 10°C rise in temperature. However, the MM450 devices are low-leakage types that are specified for use to 125°C. At the maximum temperature, leakage will usually be less than 100 nA. (At very high signal frequencies, another conduction mechanism may occur—analog signal feedthrough in the device capacitances, which can be prevented by making the gate-driver impedance low when the switch is OFF.)

The two significant forms of DC leakage are leakage from source and drain to bulk, and leakage through the channel from input to output. When all channels in the multiplexer are OFF, and the outputs of each MOSFET are connected to a common package pin, total leakage will be the sum of the bulk and channel leakages.

Worst-case leakage is measured with the circuit in Figure 10. The pin at which the leakage current is measured is biased to -25V and all other pins are grounded. This is equivalent to the bulk being biased at +10V, all gates at +10V, and all analog-signal inputs at +10V, with the output at -15V.

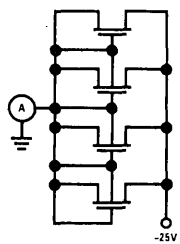


FIGURE 10. Worst-Case Leakage Test Circuit and Typical Worst-Case Total Leakage of MM451 at 25°C.

Channel leakage is measured with the test circuit in Figure 11a. At V_{in} = +10V, the leakage at the output is at its maximum positive value. As V_{in} goes more negative than +10V, channel leakage decreases, goes through zero, and becomes negative, as in Figure 11b.

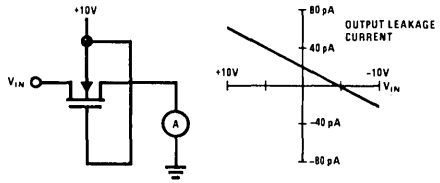


FIGURE 11. Channel-Leakage Test Circuit and Variation in Leakage with Signal Voltage.

The designer of switching systems that require very high R_{OFF} values under all signal conditions should anticipate the possibility of worst-case leakage. But average leakage will generally be considerably less than worst case. First, leakage currents in each switch are voltage-sensitive, and will be less than maximum at signal voltages less than +10V. Secondly, when the analog signals on some channels are positive and those on other channels are negative, the negative currents will subtract from the positive currents, further reducing the total leakage at the output. Also, when a switch is ON, it would not be contributing to the leakage. Assuming signal voltages vary randomly between +10 and -10V, total leakage will run about half that of worst case. Of course, leakage will be still less if the analog signal limits are less than ±10V.

CONCLUSION

Integrated MOSFET switching circuits make excellent low-level analog commutators. Power dissipation is essentially zero, capacitance is reasonably low (typically 8 pF at the analog input), the R_{OFF}/R_{ON} ratio is high, and the control signal is isolated from the input. MOS IC's with four or more switching channels are readily available in production quantities.

Conventional bipolar drive circuitry can control channel switching at rates in the megahertz range. Hybrid integrated circuits containing monolithic MOS multiplexers and bipolar drivers are being manufactured for medium-speed applications (NH0014 and NH0019). Level-changing circuits in these devices allow external TTL or DTL IC's to control the commutator at analog signal levels to ±10V. MOS commutator systems can be built with building-block circuits such as the MM454F in Figure 12. This monolithic IC can commutate at rates to 1 MHz, depending on the range of signal voltages. The control logic on the chip includes a clock-countdown chain that facilitates submultiplexing.

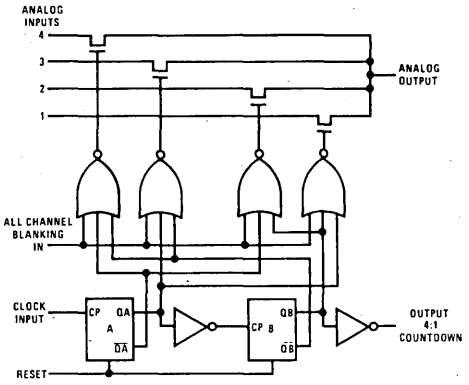


FIGURE 12. Logic Diagram of MM454F Four-Channel MOS Multiplexer. Switches and Control Circuitry Are Fabricated in the Same Monolithic Chip.

MOSFET switches are generally used to commutate low-frequency analog signals. Today, the preferred device for RF-signal multiplexing is the N-channel junction FET, which can handle signal frequencies in the VHF range. MOS IC's have operated successfully, however, in some RF application. The high-frequency capabilities of MOS IC's are being investigated by the author and will be the subject of a future report.

Although the most outstanding feature of MOSFET's is the ease with which they can be fabricated as multichannel monolithic IC's, their electrical characteristics compare quite favorably with those of other switching components. An "order of magnitude" comparison of MOSFET's and other devices that could be used for low-level analog switching is given by Table 1. Better characteristics might be obtained in each case, but these values are typical.

Each type of analog switch has advantages and limitations that must be considered for practical use. No switch is perfect. If a switch were perfect, it would have zero resistance when ON, infinite resistance when OFF, and be 100% efficient–that is, it would consume no power.

Electrically, the mechanical switch comes close to this ideal. It has the highest R_{OFF}/R_{ON} ratio and totally isolates the analog signal from the switching-control function. However, it has mechanical drawbacks that make it noisy and unsuitable for low-level commutation: contact bounce, contact pitting, susceptibility to vibration, and the necessity to move a physical mass to turn the switch on or off. It cannot commutate very fast and consumes more power than a solid-state switch, as a rule.

Bipolar transistors make excellent digital switches, the fastest ever developed, but they are usually a poor choice for multiplexing low-level analog signals. Their main disadvantages are an inherent offset voltage and the impossibility of isolating the switching control signal from the analog signal being switched. Furthermore, analog switching rates are slower than FET's. Their R_{on} is low, though–typically 10 ohms in analog switches (versus milliohms in power transistors). Bipolar transistors fare much better in high-level switching, where DC offset is not a problem.

Photocells make fairly good analog switches. Because light is used as the control signal, the control is completely isolated from the analog electrical signal. However, R_{ON} is high and the R_{OFF}/R_{ON} ratio is relatively poor. Even at moderate R_{OFF}/R_{ON} ratios, photocells cannot commutate much faster than 100 Hz. After exposure to intense light, a photocell made with a semiconductor such as cadmium sulfide or cadmium selenide exhibits a long turn-off decay time. Photocell turn-off time constants may stretch out for many seconds before R_{OFF} reaches an acceptable level. Faster switches can be made with combinations of electroluminescent diodes and phototransistors, but these devices are still very expensive.

Some N-channel junction FET's come close to being ideal switches. Offset voltage is zero, and the admittance-to-input capacitance ratio Y_{fs}/C_{iss} is the highest of any contemporary device. These two parameters govern commutation rate, which can be very high if the impedances of the signal source and the load are made very low. Theoretically, the high majority-carrier mobility in an N-channel J-FET enables it to operate at a frequency higher than any other type of FET. A good example is the 2N4391: R_{OFF}/R_{ON} is about 10^9, $R_{ds\ (on)}$ is a maximum of 30 ohms, and maximum leakage at 25°C is 100 pA. The one major disadvantage of N-channel J-FET's is that they are extremely difficult to make in the form of multichannel IC's. For high-frequency commutation, the P-channel type of J-FET is a poor choice because its majority carrier mobility is lower than N channel J-FET's.

Applications of MOS Analog Switches

National Semiconductor
Application Note 38
R. Stump, D. Wollesen

ABSTRACT

This discussion begins with some basic commutation circuits, then describes some uses in linear amplifier applications such as reset functions and chopper applications. The use of MOS switches as a suppressed carrier double-sideband modulator and a double-sideband demodulator is then covered; followed by a circuit proposal for a phase-locked loop AM-FM detector without tuned circuits.

THE MOS DIFFERENTIAL SWITCH—DC TO RF

The dual differential switch is a particular switch connection scheme which at first glance prompts one to say—so what? It is, however, one of those simple circuit configurations which can find a wide variety of uses in electronic circuits. The dual differential switch could also be called a DPDT switch or two SPDT switches—depending on how they are toggled.

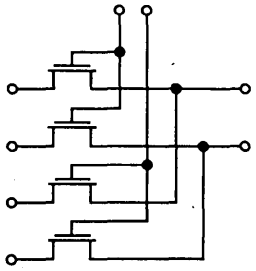
MOS switches have some unique features which make them very useful for data switching[1,2,3]: no offset voltage, high R_{OFF}/R_{ON} ratios, low leakage, fast operation, and matched "on" resistance. Within definite bounds, MOS switches exhibit good isolation between the switching drive and signal path.

MOS switches do have somewhat unique driving requirements. In order to solve this problem, National manufactures a hybrid integrated circuit which provides DTL-TTL drive compatibility with the dual differential switch. These devices use the DM7801 chip with an MM450 chip for the AH0014 and the DM7800 chip with an MM450 chip for the AH0019. The AH0014 is basically a DPDT switch while the AH0019 is two SPDT switches in the same package. Each connection has its particular advantages and disadvantages.

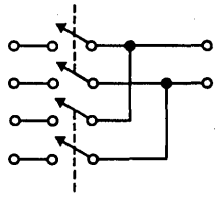
COMMUTATION CIRCUITS

The AH0014 may be used as a two channel commutator only, because two of its four channels are always on. The AH0019 may be used for systems with any number of channels since it can shut all channels off on command.

Figure 3 shows a six channel commutator which may be easily expanded. Data sampling may be done on any format which the user chooses. Sampling format is easily controlled by DTL or TTL logic design independent of the AH0019 Since each buffer-driver of the AH0019 has a dual input gate, all channel blanking is readily achieved. If desired, the format shown in Figure 3 may be



(a) MOS Configuration

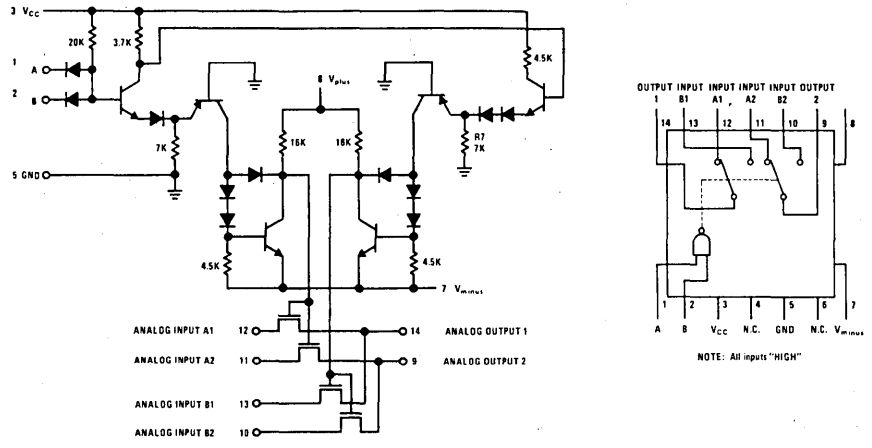


(b) Schematic Configuration

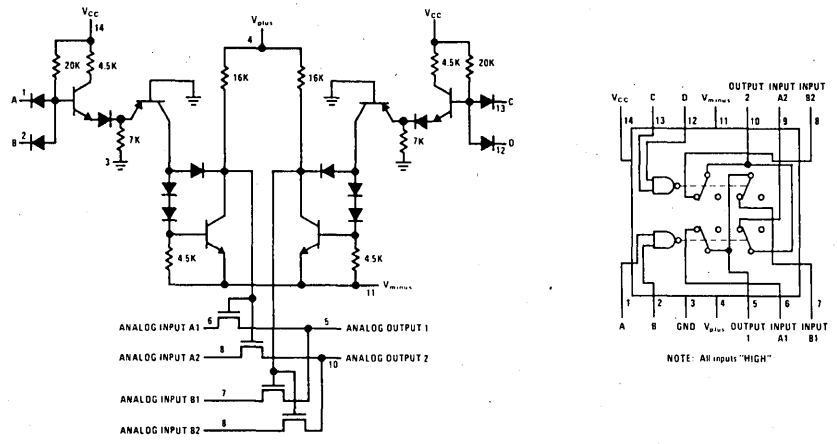
FIGURE 1. MM450/MM550 MOS Dual Differential Switch

modified so as to use the AH0019 logic inputs as binary gates which can reduce the command logic complexity if the blanking function is not required.

Since the multiplexed information is in differential form, common mode noise is greatly reduced. Also, the MOS gate drive spiking is drastically reduced because of the differential channel configuration. Demultiplexing may be accomplished by using a circuit identical to the multiplexer because the MOS device is a true bilateral switch. In hard-wired systems where the multiplex "outputs" are electrically connected as in Figure 4, the signal may be transmitted in either direction. For non-hardwired systems, the modulation-demodulation sequence is still bilateral, but provisions must be made for transmit/receive function control.



(a) AH0014



(b) AH0019

Figure 2. AH0014 and AH0019 DTL-TTL Compatible MOS Analoge switches

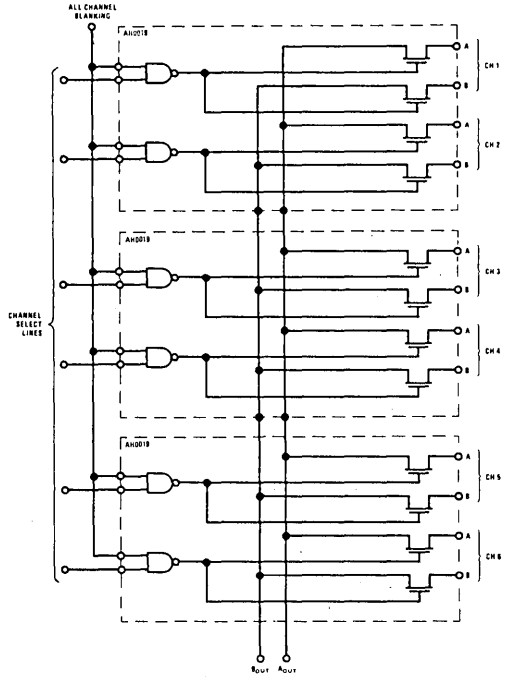


Figure 3. Differential Signal Commutator– AH0019

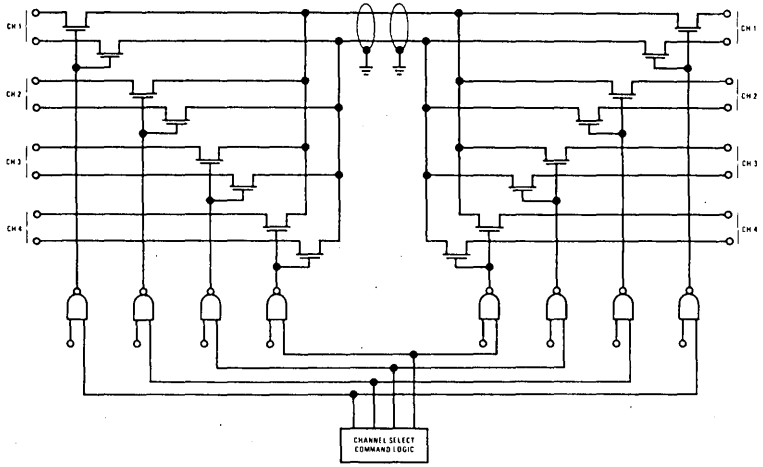


FIGURE 4. Commutation-Modulation and Demodulation

USAGE IN LINEAR AMPLIFIER CIRCUITS

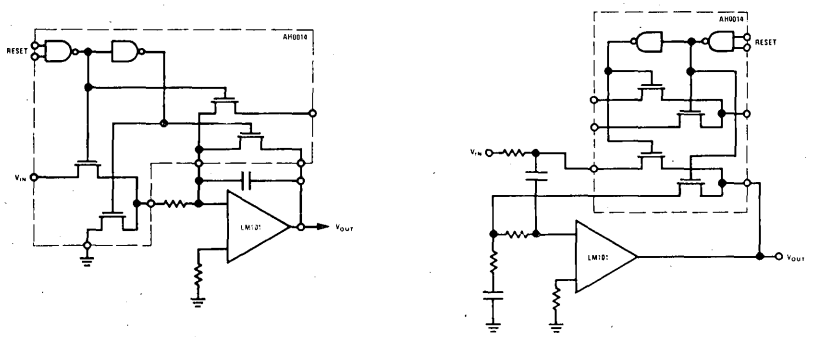
The AH0014 and AH0019 devices are useful for switching functions in linear circuit applications because of high off/on resistance ratio and ease of switching control using logic elements. Sample and hold circuits, integrator reset switching, and reset stabilized amplifiers are a few examples (Figure 5). More detailed information on this type of circuitry is available in National Semiconductor applications notes AN-4, AN-5, AN-20, and AN-29[4-7]

An obvious use of the AH0014 and AH0019 are in chopper stabilized amplifiers (Figure 6). One of the better forms of chopper stabilized amplifiers is the series shunt chopper with sample and hold type of output. The AH0014 does a good job at this because it contains the complete set of switches plus proper drive for the switches. The AH0014 can greatly reduce component count for chopper stabilized amplifiers.

DOUBLE SIDEBAND MODULATOR

The AH0019 can be used as a double sideband modulator. In modulator applications, the AH0019 functions as a DPDT switch which alternately reverses the polarity of the modulating signal at the chopper frequency. MOS switches work quite well at this application because of zero offset voltage and large signal handling ability.

In order to build a double sideband balanced modulator[8,9], one of the two modulating inputs must be applied as a balanced input. For the circuit shown in Figure 7, an LM102 and LM107 were used for an audio phase splitter.



(a) Integrator

(b) Reset Stabilized Amplifier

FIGURE 5. Switching Applications With Linear Circuits

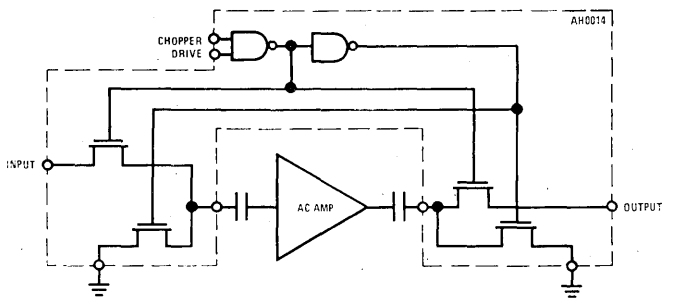


FIGURE 6. Series-Shunt Chopper Stabilized Amplifier

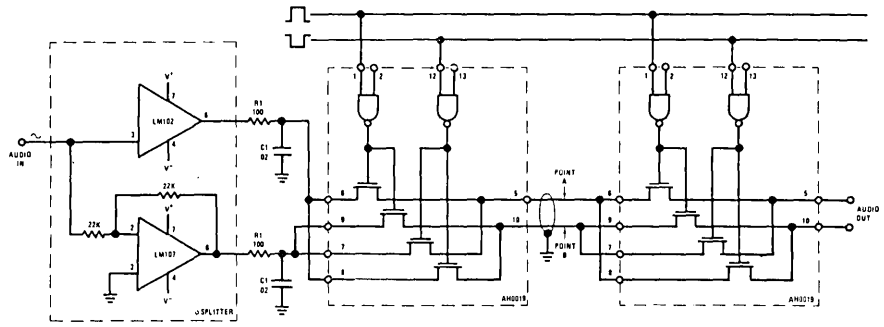


FIGURE 7. Double Sideband Modulator-Demodulator

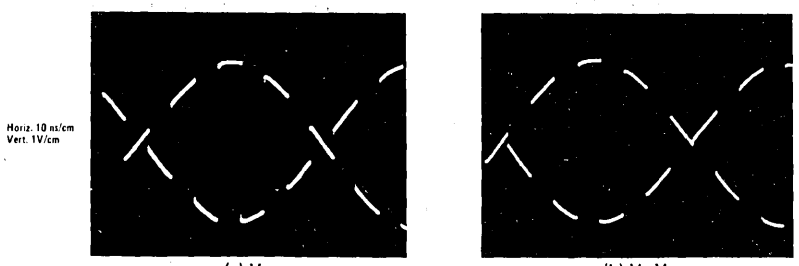
Both point A and point B in Figure 7 are DSB modulated outputs; so, technically, you could get by with only one. The waveform at point A is illustrated in Figure 8a for a carrier frequency of 100 kHz and an audio frequency of 12.5 kHz. Point B is equal and out of phase.

One type of spurious response encountered with MOS switching devices is output spikes caused by a charge being dumped into the channel by the gate drive through gate-channel capacitance. By adding C1, part of the charge can be absorbed, thus reducing the voltage amplitude of the spikes. The R1C1 combination has its 3 dB point at about 80 kc, so output from the phase splitter was not attenuated in the audio range.

The astute observer will notice switching transients on the waveform in Figure 8a. By taking the output in differential form at points A and B, these transients are greatly reduced because the desired signals are equal but of opposite polarity, while the switching transients are an "in phase" or "common mode" error.

To better illustrate the improvement by using a balanced output, the audio signal was reduced to zero volts and the points A, B, and A-B were measured as shown in Figure 9. The improvement operating in the differential mode is obvious.

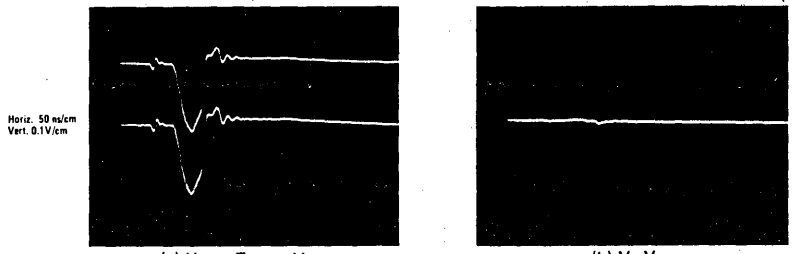
The circuit drive requirements for Figure 7 may be simplified by using the AH0014 since it provides an inverting function internally. Only one phase of toggle drive to the AH0014 is required.



(a) V_a (b) V_a-V_b

FIGURE 8. Double Sideband Signal

The modulation will be distorted more due to the phase lag created by the internal inverter of the AH0014 Figure 10a shows the switching performance of the AH0019 while Figure 10b shows the switching performance of the AH0014 In applications which do not require high carrier frequencies, the AH0014 is adequate, but for carrier frequencies above 100 kHz, the AH0019 provides improved performance because of its symmetrical switching behavior.



(a) Upper Trace - V_a
Lower Trace - V_b

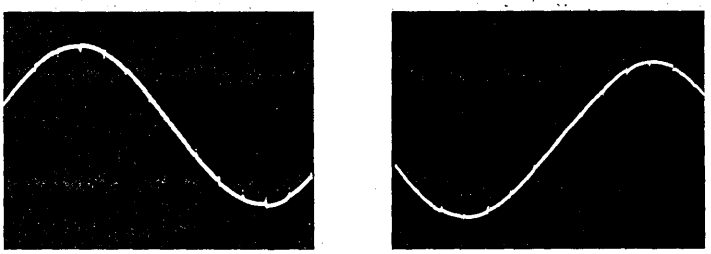
(b) V_a-V_b

FIGURE 9. MOS Switching Transients

(a) NH0019 50 ns/cm

(b) NH0014 50 ns/cm

FIGURE 10. Channel Switching– AH0019 vs AH0014



(a) Single Ended Output

(b) Differential Output

FIGURE 11. Demodulator Recovered Output

DOUBLE SIDEBAND DEMODULATOR

The major requirement of double sideband signal demodulation is proper carrier reinsertion. For maximum output, the carrier must be reinserted exactly in phase or exactly 180° out of phase with respect to the signal. Any departure from this optimum phase relationship will reduce the recovered signal amplitude. By applying the double sideband signal to a second AH0019 as shown in Figure 7, the original modulating waveform may be recovered, along with some switching transients (Figure 11).

These switching transients may be filtered out quite easily. It is, however, instructive to compare the recovered audio signal with the original. The modulating signal had less than 0.1% distortion at 1 kHz. Figure 12 shows the distortion of the recovered signal vs. signal amplitude.

Carrier frequency was 100 Hz for the upper curve and 10 kHz for the lower. These curves indicate that most of the distortion is due to switching transients, especially at low modulation levels. Output filtering will significantly reduce the recovered signal distortion.

Figure 13 emphasizes the affect that switching transients have on harmonic distortion. At carrier frequencies below 10 kHz, the RMS value of the transients is reduced to a point where distortion of the MOS switches themselves can be seen.

The AH0014 and AH0019 data sheet suggests a V plus supply value of 10 volts and a V minus supply value of −20 volts. However, switching transients may be reduced by using different power supply voltages. Figure 14 and Figure 15 show what happens to harmonic distortion caused by spiking versus power supply level. Figure 14 is plotted for V minus with V plus at 10 volts. Figure 15 shows what happens as V plus is varied. All of the previous data was taken at V plus at 14 volts and V minus at −12 volts.

AM-FM DEMODULATOR

Although an AM-FM demodulator was not physically constructed, the previously discussed "double sideband demodulator" performance implies that a very interesting phase detector can be built. The interesting features of this type of a detector are large dynamic range, recovery of both in-phase (amplitude modulated) and quadrature-phase (frequency modulated) signals plus the feasibility of not using any inductors for tuning.

Figure 16 shows the proposed circuit block diagram which uses a phase-locked loop for phase reference signal. The voltage controlled oscillator (VCO) is operated at 4 f_o. Flip Flop #1 provides a two phase output which is fed into FF #2 and FF #3. The outputs of FF #2 and FF #3 are exactly 90° out of phase regardless of the frequency of the VCO. This kind of performance is awfully hard to achieve using tuned circuits. For a 455 kHz detector, the VCO would operate at 1820 kHz. TTL flip flops will operate quite nicely at that frequency and should hold phase shift errors to practically zero. The LM107 provides DC gain to close the phase-locked loop, it forces the VCO to a frequency and phase angle which causes the "FM out" port to zero volts DC; this port is then operating exactly in quadrature with the applied signal. This part of the detector is then insensitive to amplitude modulation and sensitive to frequency modulation. Since the AM detector portion is operating exactly 90° out of phase with the FM portion, its output is insensitive to FM and sensitive to AM.

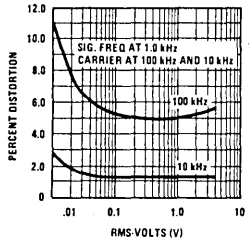


FIGURE 12. Recovered Signal Harmonic Distortion vs Audio Modulation Level

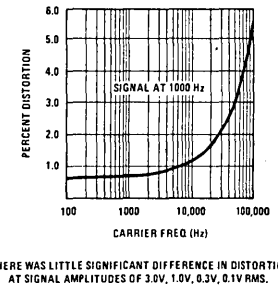


FIGURE 13. Recovered Signal Harmonic Distortion vs Carrier Frequency

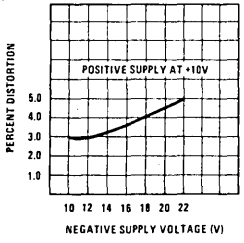


FIGURE 14. Harmonic Distortion vs Negative Power Supply Voltage

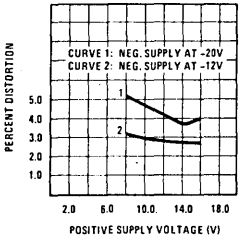


FIGURE 15. Harmonic Distortion vs Positive Supply Voltage

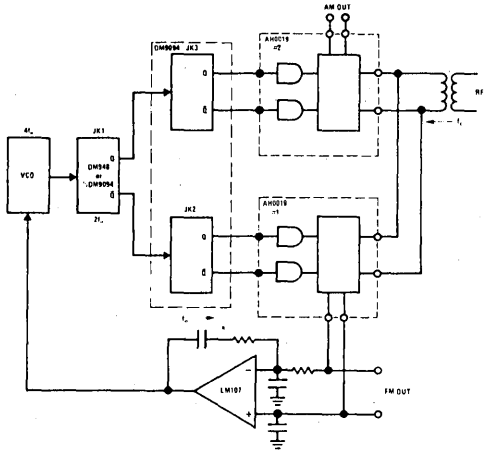


FIGURE 16. AM-FM Demodulator

CONCLUSION

The most obvious use of the AH0014 and AH0019 is in commutator applications, and it indeed is a very useful device for that purpose. The use of these switches in linear circuit applications is also very attractive because of DTL-TTL control compatibility. There are many more uses of these switches possible than the few examples described here.

The unusual application of these devices as suppressed carrier double-sideband modulators and demodulators suggests applications in servo systems and even communications systems due to their high speed operation. The final circuit suggestion, a phase-locked loop AM-FM demodulator without tuned circuits should be very useful in communications systems. The AH0019 will operate quite well at an IF frequency of 455 kHz or less.

These basic capabilities of the MOS dual differential switch should encourage much greater usage of this type of device in new product designs.

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Applications for a New Ultra-High Speed Buffer

National Semiconductor
Application Note 48
Barry Siegel
Leonard Van Der Gaag

INTRODUCTION

Voltage followers have gained in popularity in applications such as sample and hold circuits, general purpose buffers, and active filters since the introduction of IC operational amplifiers. Since they were not specifically designed as followers, these early IC's had limited usage due to low bandwidth, low slew rate and high input current. Usage of voltage followers was expanded in 1967 with the introduction of the LM102, the first IC designed specifically as a voltage follower. With the LM102, engineers were able to obtain an order of magnitude improvement in performance and extend usage into medium speed applications. The LM110, an improved LM102, was introduced in late 1969. However, even higher speeds and lower input currents were needed for very fast sample and holds, A to D and D to A converters, coax cable drivers, and other video applications.

The solution to this application problem was attained by combining technologies into a single package. The result, the LH0033 high speed buffer, utilizes JFET and bipolar technology to produce a ultra-fast voltage follower and buffer whose propagation delay closely approaches speed-of-light delay across its package, while not compromising input impedance or drive characteristics. Table I compares various voltage followers and illustrates the superiority of the LH0033 in both low input current or high speed video applications.

CIRCUIT CONSIDERATIONS

The junction FET makes a nearly ideal input device for a voltage follower, reducing input bias current to the picoamp range. However, FET's exhibit moderate voltage offsets and offset drifts which tend to be difficult to compensate. The simple voltage follower of Figure 1 eliminates initial offset and offset drift if Q_1 and Q_2 are identically matched transistors. Since the gate to source voltage of Q_2 equals zero volts, then Q_1's gate to source voltage equals zero volts. Furthermore as V_{P1} changes with temperature (approximately 2.2 mV/°C), V_{P2} will change by a corresponding amount. However, as load current is drawn from the output, Q_1 and Q_2 will drift at different rates. A circuit which overcomes offset voltage drift is used in a new high speed buffer amplifier, the LH0033. Initial offset is typically 5 mV and offset drift is 20 μV/°C. Resistor R_2 is used to establish the drain current of current source transistor, Q_2 at 10 mA.

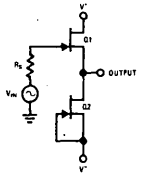

FIGURE 1. Simple Voltage Follower Schematic

The same drain current flows through Q_1 causing a voltage at the source of approximately 1.1V. The 10 mA flowing through R_1 plus Q_3's V_{BE} of 0.6V causes the output to sit at zero volts for zero volts in. Q_3 and Q_4 eliminate loading the input stage (except for base current) and CR_1 and CR_2 establish the output stage collector current.

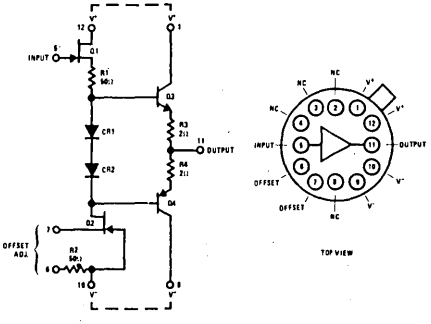

FIGURE 2. LH0033 Schematic

If Q_1 and Q_2 are matched, the resulting drift is reduced to a few μV/°C.

TABLE I COMPARISON OF VOLTAGE FOLLOWERS

PARAMETER	CONVENTIONAL MONOLITHIC OP AMP LM741	FIRST GENERATION VOLTAGE FOLLOWER LM102	SECOND GENERATION VOLTAGE FOLLOWER LM110	SPECIALLY DESIGNED VOLTAGE FOLLOWER LH0033
INPUT BIAS CURRENT	200 nA	3.0 nA	1.0 nA	0.05 nA
SLEW RATE	0.5V/μs	10V/μs	30V/μs	1500V/μs
BANDWIDTH	1.0 MHz	10 MHz	20 MHz	100 MHz
PROP. DELAY TIME	350 ns	35 ns	18 ns	1.2 ns
OUTPUT CURRENT CAPABILITY	±5 mA	±2 mA	±2 mA	±100 mA

PERFORMANCE OF THE LH0033 FAST VOLTAGE FOLLOWER/BUFFER

The major electrical characteristics of the LH0033 are summarized in Table II. All the virtues of a ultra-high speed buffer have been incorporated. Figure 3 is a plot of input bias current vs temperature and shows the typical FET input characteristics. Other typical performance curves are illustrated in Figures 4 through 10. Of particular interest is Figure 8, which demonstrates the performance of the LH0033 in video applications to over 100 MHz.

TABLE II

PARAMETER	CONDITIONS	VALUE	PARAMETER	CONDITIONS	VALUE
Output Offset Voltage	R_S = 100 kΩ	5 mV	Output Current Capability		±100 mA peak
Input Bias Current		50 pA	Slew Rate	R_S = 50Ω, R_L = 1k	1500V/μs
Input Impedance	V_{IN} = 1.0 Vrms R_L = 1k, f = 1 kHz	10^{11} Ω	Propagation Delay		1.2 ns
Voltage Gain	V_{IN} = 1.0 Vrms R_L = 1k, f = 1 kHz, R_S = 100k	0.98	Bandwidth	V_{IN} = 1.0 Vrms R_S = 50Ω, R_L = 1k	100 MHz
Output Voltage Swing	V_S = ±15V, R_S = 100k R_L = 1k	±13V			

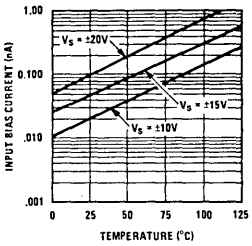

FIGURE 3. Input Bias Current vs Temperature

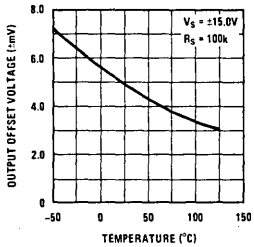

FIGURE 4. Output Offset Voltage vs Temperature

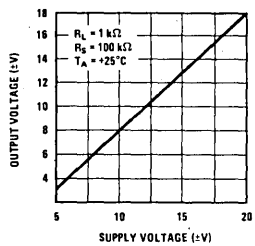

FIGURE 5. Output Voltage vs Supply Voltage

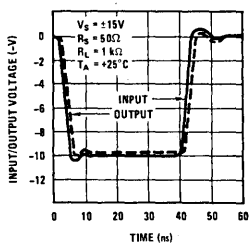

FIGURE 6. Negative Pulse Response

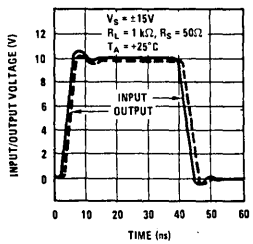

FIGURE 7. Positive Pulse Response

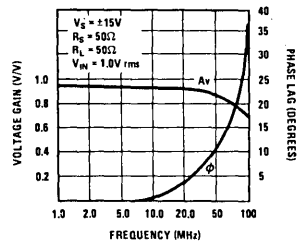

FIGURE 8. Frequency Response

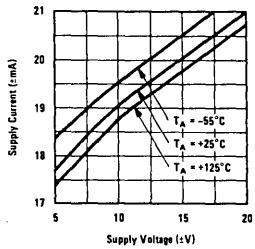

FIGURE 9. Supply Current vs Supply Voltage

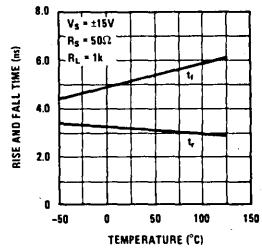

FIGURE 10. Rise and Fall Time vs Temperature

APPLICATIONS FOR ULTRA-FAST FOLLOWERS

The LH0033's high input impedance (10^{11} Ω, shunted by 2 pF) and high slew rate assure minimal loading and high fidelity in following high speed pulses and signals. As shown below, the LH0033 is used as a buffer between MOS logic and a high speed dual limit comparator. The device's high input impedance prevents loading of the MOS logic signal (even a conventional scope probe will distort high output impedance MOS). The LH0033 adds about a 1.5 ns to the total delay of the comparator. Adjustment of voltage divider R_1,R_2 allows interface to TTL, DTL and other high speed logic forms.

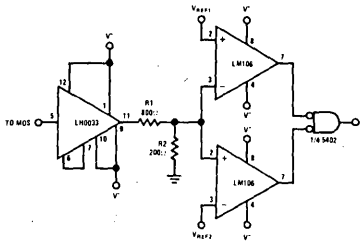

FIGURE 11. High Speed Dual Limit Comparator for MOS Logic

The LH0033 was designed to drive long cables, shielded cables, coaxial cables and other generally stringent line driving requirements. It will typically drive 200 pF with no degradation in slew rate and several thousand pF at a reduced rate. In order to prevent oscillations with large capacitive loads, provision has been made to insert damping resistors between V^+ and pin 1, and V^- and pin 9. Values between 47 and 100Ω work well for $C_L > 1000$ pF. For non-reactive loads, pin 12 should be shorted to pin 1 and pin 10 shorted to pin 9. A coaxial driver is shown in Figure 13. Pin 6 is shorted to pin 7, obtaining an initial offset of 5.0 mV, and the 43Ω coupled with the LH0033's output impedance (about 6Ω) match the coaxial cable's characteristic impedance. C_1 is adjusted as a function of cable length to optimize rise and fall time. Rise time for the circuit as shown in Figure 12, is 10 ns.

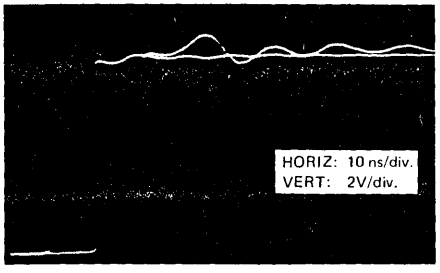

FIGURE 12. LH0033 Pulse Response into 10 Foot Open Ended Coaxial Cable

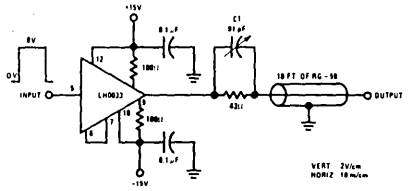

FIGURE 13.

Another application that utilizes the low input current, high speed and high capacitance drive capabilities of the LH0033 is a shield or line driver for high speed automatic test equipment. In this example, the LH0033 is mounted close to the device under test and drives the cable shield thus allowing higher speed operation since the device under test does not have to charge the cable.

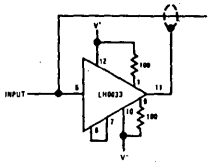

FIGURE 14. Instrumentation Shield/Line Driver

The LH0033's high input impedance and low input bias current may be utilized in medium speed circuits such as Sample and Hold, and D to A converters. Figure 15 shows an LH0033 used as a buffer in medium speed D to A converter.

Offset null is accomplished by connecting a 100Ω pot between pin 7 and V^-. It is generally a good idea to insert 20Ω in series with the pot to prevent excessive power dissipation in the LH0033 when the pot is shorted out. In non-critical or AC coupled applications, pin 6 should be shorted to pin 7. The resulting output offset is typically 5 mV at 25°C.

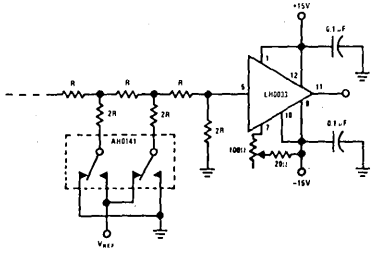

FIGURE 15.

The high output current capability and slew rate of the LH0033 are utilized in the sample and hold circuit of Figure 16. Amplifier, A1 is used to buffer high speed analog signals. With the configuration shown, acquisition time is limited by the time constant of the switch "ON" resistance and sampling capacitor, and is typically 200 or 300 ns. A_2's low input bias current, results in drifts in hold mode of $\frac{50\text{ mV}}{\text{sec}}$ at 25°C and $\frac{1\text{V}}{\text{sec}}$ at 125°C.

The LH0033 may be utilized in AC applications such as video amplifiers and active filters. The circuit of Figure 17 utilizes boot strapping to achieve input impedances in excess of 10 MΩ.

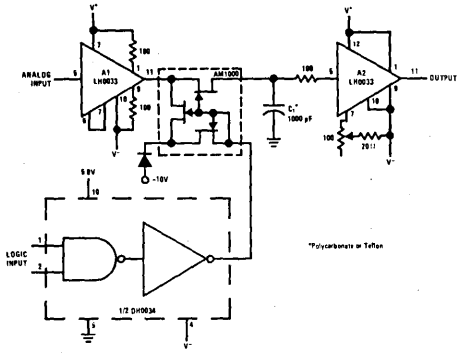

FIGURE 16. High Speed Sample & Hold

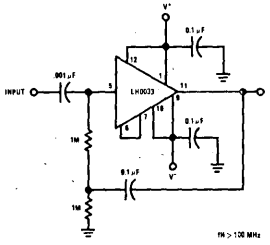

FIGURE 17. High Input Impedance AC Coupled Amplifier

A single supply, AC coupled amplifier is shown in Figure 18. Input impedance is approximately 500k and output swing is in excess of 8V peak-to-peak with a 12V supply.

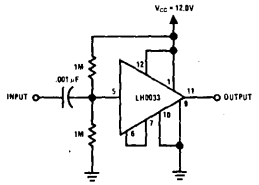

FIGURE 18. Single Supply AC Amplifier

The LH0033 may be readily used in applications where symmetrical supplies are unavailable or may not be desirable. A typical application might be an interface to an MOS shift register where V^+ = 5.0V and V^- = -25V. In this case, an apparent output offset occurs. In reality, the output voltage is due to the LH0033's voltage gain of less than unity. The output voltage shift due to asymmetrical supplies may be predicted by:

$$\Delta V_O \cong (1 - Av)\ \frac{(V^+ - V^-)}{2} = .005\ (V^+ - V^-)$$

where: Av = No load voltage gain, typically 0.99.

V^+ = Positive Supply Voltage.

V^- = Negative Supply Voltage.

For the foregoing application, ΔV_O would be -100 mV. This apparent "offset" may be adjusted to zero as outlined above.

Figure 19 shows a high Q, notch filter which takes advantage of the LH0033's wide bandwidth. For the values shown, the center frequency is 4.5 MHz.

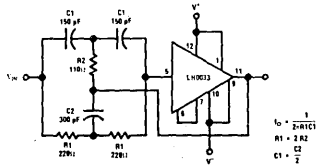

FIGURE 19. 4.5 MHz Notch Filter

The LH0033 can also be used in conjunction with an operational amplifier as current booster as shown in Figure 20. Output currents in excess of 100 mA may be obtained. Inclusion of 150Ω resistors between pins 1 and 12, and 9 and 10 provide short circuit protection, while decoupling pins 1 and 9 with 1000 pF capacitors allow near full output swing.

The value for the short circuit current is given by:

$$I_{SC} \cong \frac{V^+}{R_{LIMIT}} = \frac{V^-}{R_{LIMIT}}$$

where: $I_{SC} \leq 100$ mA.

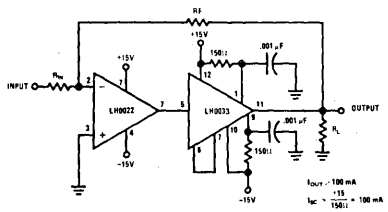

FIGURE 20. Using LH0033 as an Output Buffer

SUMMARY

The advantages of a FET input buffer have been demonstrated. The LH0033 combines very high input impedance, wide bandwidth, very high slew rate, high output capability, and design flexibility, making it an ideal buffer for applications ranging from DC to in excess of 100 MHz.

Pin Diode Drivers

National Semiconductor
Application Note 49
Barry Siegel

INTRODUCTION

The DH0035/DH0035C is a TTL/DTL compatible, DC coupled, high speed PIN diode driver. It is capable of delivering peak currents in excess of one ampere at speeds up to 10 MHz. This article demonstrates how the DH0035 may be applied to driving PIN diodes and comparable loads which require high peak currents at high repetition rates. The salient characteristics of the device are summarized in Table I.

PARAMETER	CONDITIONS	VALUE
Differential Supply Voltage ($V^+ - V^-$)		30V Max.
Output Current		1000 mA
Maximum Power		1.5W
t_{delay}	PRF = 5.0 MHz	10 ns
t_{rise}	$V^+ - V^- = 20V$ 10% to 90%	15 ns
t_{fall}	$V^+ - V^- = 20V$ 90% to 10%	10 ns

Table I DH0035 Characteristics

PIN DIODE SWITCHING REQUIREMENTS

Figure 1 shows a simplified schematic of a PIN diode switch. Typically, the PIN diode is used in RF through microwave frequency modulators and switches. Since the diode is in shunt with the RF path, the RF signal is attenuated when the diode is forward biased ("ON"), and is passed unattenuated when the diode is reversed biased ("OFF"). There are essentially two considerations of interest in the "ON" condition. First, the amount of "ON" control current must be sufficient such that RF signal current will not significantly modulate the "ON" impedance of the diode. Secondly, the time required to achieve the "ON" condition must be minimized.

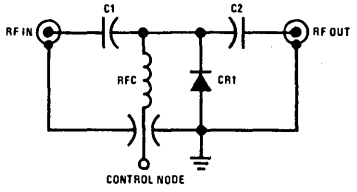

FIGURE 1. Simplified PIN Diode Switch

The charge control model of a diode[1,2] leads to the charge continuity equation given in equation (1).

$$i = \frac{dQ}{dt} + \frac{Q}{\tau} \qquad (1)$$

where: Q = charge due excess minority carriers
τ = mean life time of the minority carriers

Equation (1) implies a circuit model shown in Figure 2. Under steady conditions $\frac{dQ}{dt} = 0$, hence:

$$I_{DC} = \frac{Q}{\tau} \text{ or } Q = I_{DC}\tau \qquad (2)$$

where: I = steady state "ON" current.

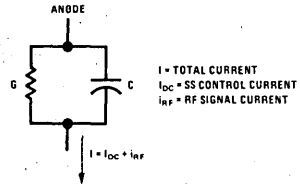

FIGURE 2. Circuit Model for PIN Switch

The conductance is proportional to the current, I; hence, in order to minimize modulation due to the RF signal, $I_{DC} >> i_{RF}$. Typical values for I_{DC} range from 50 mA to 200 mA depending on PIN diode type, and the amount of modulation that can be tolerated.

The time response of the excess charge, Q, may be evaluated by taking the Laplace transform of equation (1) and solving for Q:

$$Q(s) = \frac{\tau I(s)}{1 + s\tau} \qquad (3)$$

Solving equation (3) for Q(t) yields:

$$Q(t) = L^{-1}[Q(s)] = I\tau(1 - \epsilon^{-t/\tau}) \qquad (4)$$

The time response of Q is shown in Figure 3a. As can be seen, several carrier lifetimes are required to achieve the steady state "ON" condition ($Q = I_{DC} \cdot \tau$).

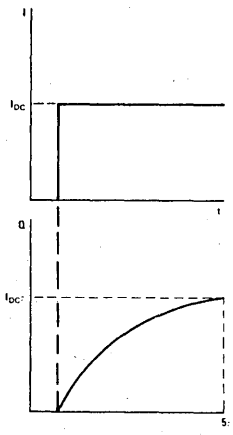

FIGURE 3a.

The time response of the charge, hence the time for the diode to achieve the "ON" state could be shortened by applying a current spike, Ipk, to the diode and then dropping the current to the steady state value, I_{DC}, as shown in Figure 3b. The optimum response would be dictated by:

$$(Ipk)\,(t) = \tau \cdot I_{DC} \qquad (5)$$

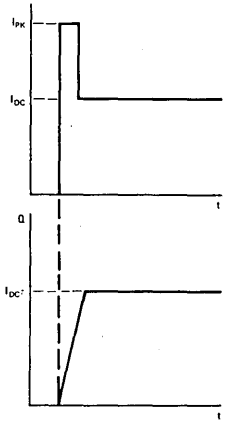

FIGURE 3b.

The turn off requirements for the PIN diode are quite similar to the turn on, except that in the "OFF" condition, the steady current drops to the diode's reverse leakage current.

A charge, $I_{DC} \cdot \tau$, was stored in the diode in the "ON" condition and in order to achieve the "OFF" state this charge must be removed. Again, in order to remove the charge rapidly, a large peak current (in the opposite direction) must be applied to the PIN diode:

$$-Ipk >> \frac{Q}{\tau} \qquad (6)$$

It is interesting to note an implication of equation (5). If the peak turn on current were maintained for a period of time, say equal to τ, then the diode would acquire an excess charge equal to Ipk·T. This same charge must be removed at turn off, instead of a charge $I_{DC} \cdot \tau$, resulting in a considerably slower turn off. Accordingly, control of the width of turn on current peak is critical in achieving rapid turn off.

APPLICATION OF THE DH0035 AS A PIN DIODE DRIVER

The DH0035 is specifically designed to provide both the current levels and timing intervals required to optimally drive PIN diode switches. Its

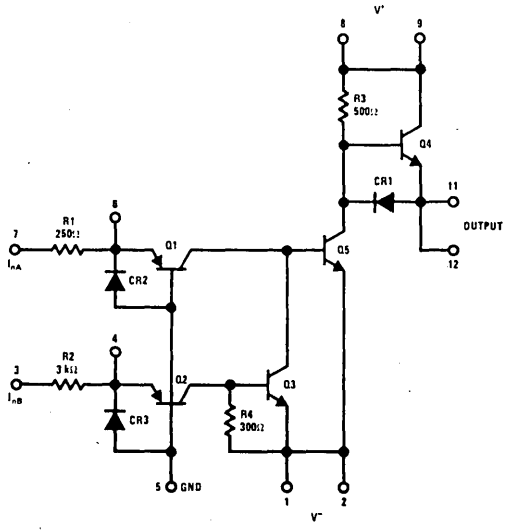

FIGURE 4. DH0035 Schematic Diagram

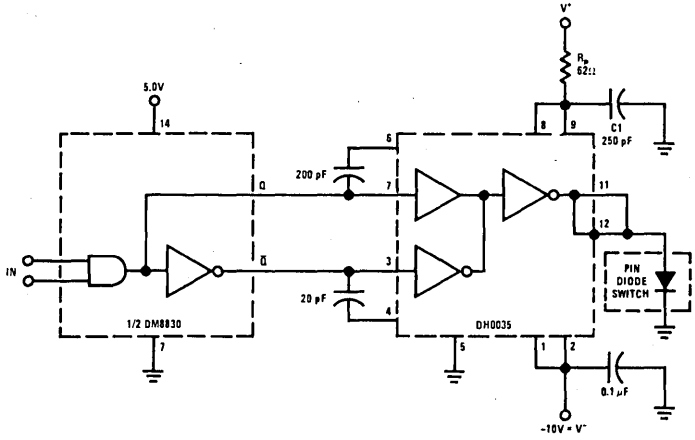

FIGURE 5. Cathode Grounded Design

schematic is shown in Figure 4. The device utilizes a complementary TTL input buffer such as the DM7830/DM8830 or DM5440/DM7440 for its input signals.

Two configurations of PIN diode switch are possible: cathode grounded and anode grounded. The design procedures for the two configurations will be considered separately.

ANODE GROUND DESIGN

Selection of power supply voltages is the first consideration. Table I reveals that the DH0035 can withstand a total of 30V differentially. The supply voltage may be divided symmetrically at ±15V, for example. Or asymmetrically at +20V and −10V. The PIN diode driver shown in Figure 5, uses ±10V supplies.

When the Q output of the DM8830 goes high a transient current of approximately 50 mA is applied to the emitter of Q_1 and in turn to the base of Q_5.

Q_5 has an h_{fe} = 20, and the collector current is h_{fe} x 50 or 1000 mA. This peak current, for the most part, is delivered to the PIN diode turning it "ON" (RF is "OFF").

Ipk flows until C_2 is nearly charged. This time is given by:

$$t = \frac{C2\,\Delta V}{Ipk} \qquad (7)$$

where: ΔV = the change in voltage across C_2.

Prior to Q_5's turn on, C_2 was charged to the minus supply voltage of −10V. C_2's voltage will rise to within two diode drops plus a V_{sat} of ground:

$$V = |V^-| - Vf(\text{PIN Diode}) - Vf_{CR1} - V_{sat_{Q5}} \qquad (8)$$

for V^- = −10V, ΔV = 8V.

Once C_2 is charged, the current will drop to the steady state value, I_{DC}, which is given by:

$$I_{DC} = \frac{V}{R_M} - \frac{V^+}{R_3} - \frac{V_{CC}}{R_1} \qquad (9)$$

where: V_{CC} = 5.0V
$R_1 = 250\Omega$
$R_3 = 500\Omega$

$$\therefore R_M = \frac{(R_3)\,(\Delta V)\,(R_1)}{R_1 V^+ + I_{DC} R_3 R_1 + V_{CC} R_3} \qquad (9a)$$

For the driver of Figure 5, and I_{DC} = 100 mA, R_M is 56 ohms (nearest standard value).

Returning to equation (7) and combining it with equation (5) we obtain:

$$t = \frac{\tau I_{DC}}{Ipk} = \frac{C_2 V}{Ipk} \qquad (10)$$

Solving equation (10) for C_2 gives:

$$C_2 = \frac{I_{DC}\tau}{V} \qquad (11)$$

For τ = 10 ns, C_2 = 120 pF.

One last consideration should be made with the diode in the "ON" state. The power dissipated by the DH0035 is limited to 1.5W (see Table I). The DH0035 dissipates the maximum power with Q_5 "ON". With Q_5 "OFF", neglible power is dissipated by the device. Power dissipation is given by:

$$P\,\text{diss} \cong \left[I_{DC}\,(|V^-| - \Delta V) + \frac{(V^+ - V^-)^2}{R3} \right] \times (\text{D.C.}) \leq P_{max} \qquad (12)$$

where: D.C. = Duty Cycle =

$$\frac{(\text{"ON" time})}{(\text{"ON" time} + \text{"OFF" time})}$$

Pmax = 1.5W

In terms of I_{DC}:

$$I_{DC} \leq \frac{\left[\frac{(Pmax)}{(D.C.)} - \frac{(V^+ - V^-)^2}{500} \right]}{|V^-| - \Delta V} \qquad (12a)$$

For the circuit of Figure 5 and a 50% duty cycle, P diss = 0.5W.

Turn-off of the PIN diode begins when the Q output of the DM8830 returns to logic "0" and the $\overline{Q}$ output goes to logic "1". Q_2 turns "ON", and in turn, causes Q_3 to saturate. Simultaneously, Q_1 is turned "OFF" stopping the base drive to Q_5. Q_3 absorbs the stored base charge of Q_5 facilitating its rapid turn-off. As Q_5's collector begins to rise, Q_4 turns "ON". At this instant, the PIN diode is still in conduction and the emitter of Q_4 is held at approximately −0.7V. The instantaneous current available to clear stored charge out of the PIN diode is:

$$Ipk = \frac{V^+ - V_{BE\,Q4} + V_{f(PIN)}}{\frac{R_3}{h_{fe}+1}} \cong \frac{(h_{fe}+1)\,(V^+)}{R_3} \qquad (13)$$

where:

h_{fe} + 1 = current gain of Q_4 = 20

$V_{BE\,Q4}$ = base-emitter drop of Q_4 = 0.7V

$V_{f(PIN)}$ = forward drop of the PIN diode = 0.7V

For typical values given, Ipk = 400 mA. Increasing V^+ above 10V will improve turn-off time of the diode, but at the expense of power dissipation in the DH0035. Once turn-off of the diode has been achieved, the DH0035 output current drops to the reverse leakage of the PIN diode. The attendant power dissipation is reduced to about 35 mW.

CATHODE GROUND DESIGN

Figure 6 shows the DH0035 driving a cathode grounded PIN diode switch. The peak turn-on current is given by:

$$Ipk \cong \frac{(V^+ - V^-)\,(h_{fe}+1)}{R_3} \qquad (14)$$

= 800 mA for the values shown.

The steady state current, I_{DC}, is set by Rp and is given by:

$$I_{DC} = \frac{V^+ - 2V_{BE}}{\frac{R_3}{h_{fe}+1} + R_P} \qquad (15)$$

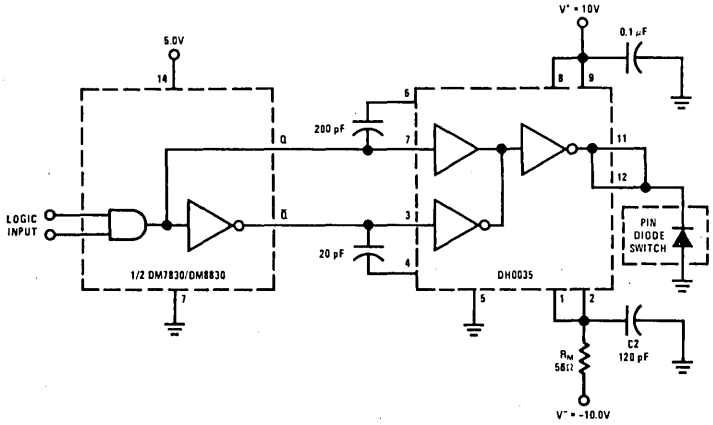

FIGURE 6. Anode Grounded Driver

where: $2V_{BE}$ = forward drop of Q_4 base emitter junction plus V_f of the PIN diode = 1.4V.

In terms of Rp, equation (15) becomes:

$$Rp = \frac{(h_{fe} + 1)\,(V^+ - 2V_{BE}) - I_{DC}R_9}{(h_{fe} + 1)\,I_{DC}} \qquad (15a)$$

For the circuit of Figure 6, and I_{DC} = 100 mA, Rp is 62 ohms (nearest standard value).

It now remains to select the value of C_1. To do this, the change in voltage across C_1 must be evaluated. In the "ON" state, the voltage across C_1, Vc, is given by:

$$(Vc)_{ON} = \frac{V^+R_3 + Rp(h_{fe} + 1)\,(2V_{BE})}{R_3 + (h_{fe} + 1)\,Rp} \qquad (16)$$

For the values indicated above, $(Vc)_{ON}$ = 3.8V.

In the "OFF" state, Vc is given by:

$$(Vc)_{OFF} = \frac{V^+R_3 - |V^-|Rp}{Rp + R_3} \qquad (17)$$

= 8.0V for the circuit of Figure 6.

Hence, the change in voltage across C_1 is:

$$\begin{aligned} V &= (Vc)_{OFF} - (Vc)_{ON} \qquad (18)\\ &= 8.0 - 3.8\\ &= 4.2V \end{aligned}$$

The value of C_4 is given, as before, by equation (11):

$$C_1 = \frac{I_{DC}\tau}{V^-} \qquad (19)$$

For a diode with τ = 10 ns and I_{DC} = 100 mA, C_1 = 250 pF.

Again, the power dissipated by the DH0035 must be considered. In the "OFF" state, the power dissipation is given by:

$$P_{OFF} = \left[\frac{V^+ - V^-)^2}{R_3}\right](D.C.) \qquad (20)$$

where: D.C. = duty cycle =

$$\frac{\text{"OFF" time}}{\text{"OFF" time} + \text{"ON" time}}$$

The "ON" power dissipation is given by:

$$P_{ON} = \left[\frac{(Vc)_{ON}{}^2}{R_3} + I_{DC} \times (Vc)_{ON}\right](1 - D.C.) \qquad (21)$$

where: $(Vc)_{ON}$ is defined by equation (16).

Total power dissipated by the DH0035 is simply $P_{ON} + P_{OFF}$. For a 50% duty cycle and the circuit of Figure 6, P diss = 616 mW.

The peak turn-off current is, as indicated earlier, equal to 50 mA x h_{fe} which is about 1000 mA. Once the excess stored charge is removed, the current through Q_5 drops to the diodes leakage current. Reverse bias across the diode = $V^- - V_{sat} \cong -10V$ for the circuit of Figure 6.

REPETITION RATE CONSIDERATIONS

Although ignored until now, the PRF, in particular, the "OFF" time of the PIN diode is important in selection of C_2, R_M, and C_1, Rp. The capacitors must recharge completely during the diode "OFF" time. In short:

$$4\,R_MC_2 \leq t_{OFF} \qquad (22a)$$

$$4\,RpC_1 \leq t_{OFF} \qquad (22b)$$

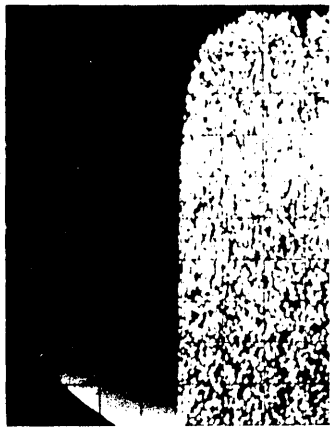

FIGURE 7. RF Turn-On (10 ns/cm)

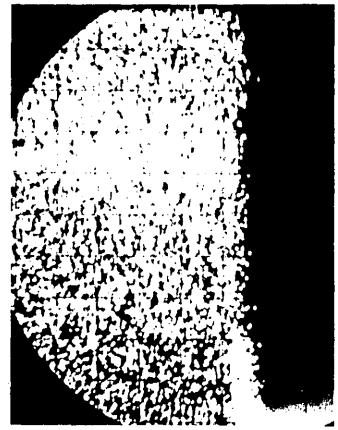

FIGURE 8. RF Turn-Off (10 ns/cm)

CONCLUSION

The circuit of Figure 6 was breadboarded and tested in conjunction with a Hewlett-Packard 33622A PIN diode.

I_{DC} was set at 100 mA, V^+ = 10.0V, V^- = 10V. Input signal to the DM8830 was a 5V peak, 100 kHz, 5 μs wide pulse train. RF turn-on was accomplished in 10-12 ns while turn-off took approximately 5 ns, as shown in Figures 7 and 8.

In practice, adjustment C_2 (C_1) may be required to accommodate the particular PIN diode minority carrier life time.

SUMMARY

A unique circuit utilized in the driving of PIN diodes has been presented. Further a technique has been demonstrated which enable the designer to tailor the DH0035 driver to the PIN diode application.

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2. "Models of Transistors and Diodes", John G. Linvill, *McGraw-Hill Book* Company, Inc., New York, N.Y.
3. *National Semiconductor AN-18,* Bert Mitchell, March 1969.
4. *Hewlett-Packard* Application Note314, January 1967.

New Design Techniques for FET Op Amps

National Semiconductor
Application Note 63
Robert K. Underwood

Introduction

The LH0052, LH0042 and LH0022 series operational amplifiers are "monobrid" integrated circuits consisting of a monolithic dual junction field effect transistor followed by a special linear integrated circuit amplifier chip. Each device features very closely matched input characteristics, very high input impedance, and ultra low input currents with no compromise in noise, common mode rejection ratio, open loop gain or slew rate. The LH0052 is internally laser nulled and features offset current of 100 femtoamps max at 25°C (100 pA at +125°C), offset voltage of 200 microvolts max and offset drift of 5 μV/°C max. Unlike most module FET op amps, this series of op amps does not require "grading" of electrical performance at final test. Different die types are used in each member of the family to assure availability and lowest possible cost. The amplifiers are internally compensated to be unity gain stable and require no external parts for operation with the exception of feedback and input impedances as dictated by the application. Amplifiers are available in TO-99, (TO-5 metal can) or 14-lead cavity dual-in-line package and are specified either for the full military temperature range of −55°C to +125°C or for an expanded commercial temperature range of −25°C to +85°C. Operation is specified for power supply voltages between 10 volts (±5 volts) and 44 volts (±22 volts). Table I below, and Typical Performance Characteristics (last page) give a summary of other major parameters illustrating similarities and differences of members of the series. See individual data sheets for complete specifications.

TABLE I

PERFORMANCE COMPARISON OF LH0052/LH0022/LH0042 FET OP AMP FAMILY

PARAMETER (T_A = 25°C)	LH0052	LH0022	LH0042	UNITS
Offset Voltage (Max)	0.5	4	20	mV
Offset Voltage Drift (Typ)	2	5	5	μV/°C
Offset Current (Max)	2.5	2.0	5.0	pA
Bias Current (Max)	1.0	10	25	pA
Open Loop Gain (Min)	100	100	50	V/mV
Bandwidth (Typ)	1	1	1	MHz
Slew Rate (Typ)	3	3	3	V/μs
Output Current Drive (Min)	±10	±10	±10	mA
Min Supply Voltage	±5	±5	±5	V
Max Supply Voltage	±22	±22	±22	V
Input Voltage Range (Min)	±12	±12	±12	V
CMRR (Min)	80	80	70	dB
Compensation Components	0	0	0	
Output Current Limit	Yes	Yes	Yes	
Simple Offset Null	Yes	Yes	Yes	
Package Types	TO-5	DIP, TO-5	DIP, TO-5	

Why FETs?

The virtue of super gain bipolar transistors as the input stage to operational amplifiers is well known[1,2] and widely used in such amplifiers as the LM108, LM112, and LM216. These amplifiers attain very low input bias currents by special processing that allows the first stage to run at very low emitter currents while achieving current gains of 1500. This results in relatively constant bias and offset currents with temperature tending to increase at low temperatures where transistor gain is lowest. (Figure 1)

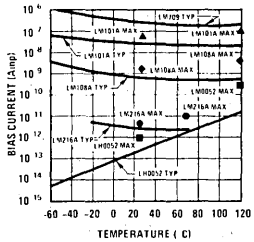


FIGURE 1. Typical I_b vs. Temperature for Several Op Amps

The low emitter current available in the typical super gain amplifier severely limits the slew rate attainable, the devices that have input currents in the same area as the LH0052 family normally have slew rates in the neighborhood of a few tenths of a volt per microsecond. As long as a FET is operated in its normal linear region, its input current is not materially affected by the channel current. The LH0052 family, therefore, runs more input stage current and thus attains a typical slew rate of three volts per microsecond. A soon-to-be announced device (LH0062) has demonstrated slew rates greater than 50 volts per microsecond with the same input characteristics as the LH0052 family.

FET's Feature Superior Noise at High Source Resistances

Figure 2 is a plot of total amplifier noise at 100 Hz (1 Hz bandwidth) vs source resistance for the LH0052 family of FET amplifiers and the LM108, representative of the best super-gain bipolar amplifiers. Thermal noise contributed by the source resistance is also plotted. Note that at low source resistances the LM108 is lower noise; at high source resistance the LH0052 series is superior.

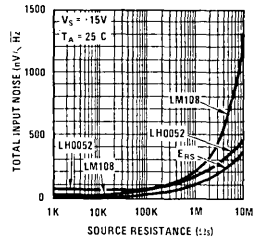


FIGURE 2. Total Equivalent Input Noise Voltage

A useful noise model applicable to operational amplifiers in general is shown in Figure 3. It consists of an ideal noiseless amplifier preceded by a number of noise sources. Amplifier voltage noise, E_N, appears directly in series with one of the inputs. Current noise from the amplifier develops an additional noise voltage across the source resistance. The RMS value of thermal noise from the source resistances can be calculated from the equation $E_{rs} = \sqrt{4kT(BW)R_s}$ which simplifies to $E_{rs} = 4\sqrt{R_s}\ nV/\sqrt{Hz}$ for room temperature calculations and resistor values in kilohms.

The total spot noise present at the input to the ideal amplifier may be found by summing the RMS values of the three noise voltage sources as follows:

$$E_T = \sqrt{E_N^2 + 2\,(R_s I_N)^2 + 2E_{rs}^2}$$

E_N comes directly from data of the type plotted in the figure by looking at the flat portion of the curve

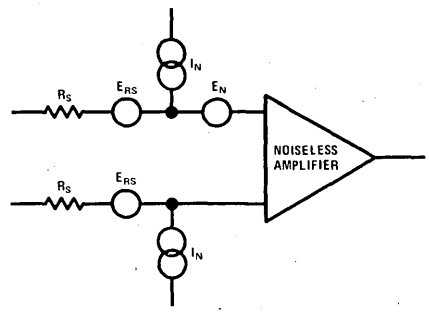


FIGURE 3. Noise Model of an Operational Amplifier

below 10k and assuming that the current noise is insignificant in this area. For the LH0052 and LM108 E_N, at 100 Hz, 1 Hz bandwidth, is 70 nV/$\sqrt{Hz}$ and 35 nV/$\sqrt{Hz}$ respectively. I_N may be computed from a total noise measurement at high source resistance by using a calculated value of E_{rs} and the previously measured value of E_N.

$$I_N = \sqrt{(E_T^2 - E_N^2 - 2E_{rs}^2)/2R_s^2}$$

For the LH0052 family and the LM108, I_N is 10 fA/$\sqrt{Hz}$ and 100 fA/$\sqrt{Hz}$ respectively.

One way to illustrate the importance of noise current in deciding which of two amplifier types will be better in a given situation is to set the total noise equal for the two cases and solve for the value of R_s at which this occurs. The amplifier with the lower noise voltage will be superior at source resistances lower than this value; the one with lower current noise will be better at higher resistances. Note that this is merely calculating the intersection of the curves of Figure 2. The intersection will normally lie near 150k when comparing the LH0052 family with the best of the presently available bipolar amplifiers.

Low Offset Voltage is no Problem with Modern JFETs

FETs have a reputation for poor control of voltage matching characteristics that developed from behavior of the early matched dual discrete devices. These were invariably a pair of separate FET chips mounted on the same header tested for gate to source voltage match at some specified current at room temperature. Devices constructed in this manner tracked rather poorly over temperature due to G_{fs} mismatch and temperature gradients across the header.

The monolithic dual FETs of the FM1100 series interweave the channels of the two halves of the device and achieve a match not only of V_{gs} but of all other parameters. Further, the V_{gs} match is preserved over a wide range of drain currents, drain to source voltage, and temperature. The voltage drift attainable with this technique is exceeded only by the very best bipolar devices.

It is possible to fabricate FETs and bipolar transistors on the same wafer at the same time. Why not build a single monolithic FET/bipolar amplifier utilizing each where it is best suited? It would seem at first glance that this would necessarily result in a cheaper, more reliable product. At the present state of the art, severe compromises are necessary to both the FET and bipolar devices so constructed as exemplified by the 740 and 536 with the net result that specifications must be relaxed and/or a yield loss suffered. The two chip "monobrid" approach taken with the LH0052 family maximizes performance while allowing lowest cost.

Circuit Description

Figure 4 is a simplified schematic typical of all of the amplifiers in the family. The input FET (Q_1, Q_2) is a monolithic dual similar in construction to the discrete FM1100 series device. The stage is operated as a source follower with V^+ applied directly to the drains for the maximum possible common mode range.

A differential common base PNP stage (Q_3, Q_4) serves as the load for the input FETs. The bases of this stage form the bias point for the backside gate of the monolithic input FET[3]. To obtain high voltage gain from the PNP common base stage, the output resistances of Q_5 and Q_6 are used as loads, giving effective values of about 2 megohms while at the same time converting the differential current signal into a single ended voltage. The operating drain current for the input stage is determined by the bias network composed of the current source Q_{10} and the diodes Q_{11} and Q_{12}; target current is 40 microamps per side.

A Darlington driver (Q_{16}, Q_{17}) is used to avoid loading the first stage output. The output stage uses a conventional complementary symmetry design with a bias current of about 60 microamps through Q_{14} and Q_{20} to minimize crossover distortion. Output current is limited to about ±25 mA at 25°C ambient decreasing to about ±17 mA at +125°C. The output characteristics are similar to those of conventional amplifiers.

Simple Offset Voltage Adjustment does not Degrade Drift or CMRR

These amplifiers use the same internal offset nulling technique as the LM741 and others, that is, a single 10k pot connected between the offset nulling pins and V^- as shown in Figure 5. Adjustment of this pot will always produce offset null. With the premium devices of the series, it may be desirable to restrict the range of adjustment to increase the precision of the null. This may be done

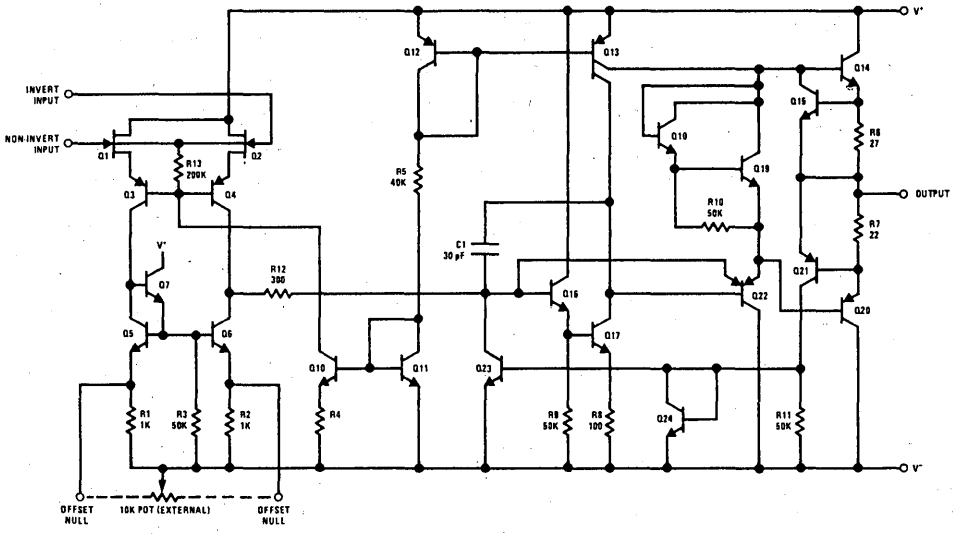


FIGURE 4. Internal Schematic

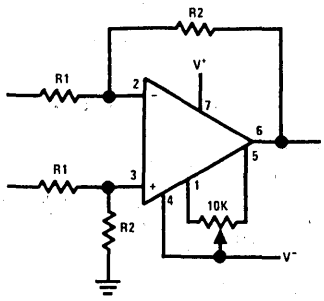


FIGURE 5. Trimpot Offset Trim

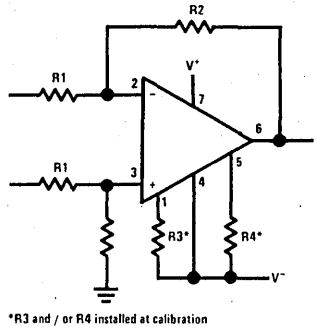


FIGURE 6. Fixed Resistor Offset Trim

by inserting a resistor of about 100k in series with the wiper of the pot. This technique provides a method of externally nulling offset voltage of the amplifiers to zero with virtually no effect on offset voltage drift or CMRR.

By definition, offset voltage is that voltage which must be applied between the input terminals to obtain zero output voltage. This suggests a straightforward and practical "universal"[4] system to null the offset in an operating circuit. Figure 7 illustrates one way that an adjustable voltage in the millivolt range may be connected in series with the input signal to subtract the amplifier offset. If this technique of offset nulling at the inputs of the amplifier is used, the TO-5 devices of the series will be pin compatible with virtually all of the 8 Pin TO-5 amplifiers on the market today, bipolar or FET.

Careful PC Board Layout Must be Observed

In order to realize the full low input current capabilities of these amplifiers, considerable care must be exercised in the design of the input circuitry and in the selection of materials contacting the input conductors. A leakage impedance of even 10^{12} ohms to 15 volts produces a leakage current of 15 pA, much higher than amplifier input current. This level of leakage may be inadvertently produced by socket leakage, poor quality or imperfectly cleaned printed circuit boards, or improperly cured protective coatings. Sockets are to be avoided if possible; they can not only degrade leakage current, but may cause other unsuspected erratic behavior when used in severe environments. (If absolutely unavoidable, they should be high quality, preferably Teflon.) Printed circuit board material should be judged both on initial resistivity and on the likelihood of degradation by

outside influences. Teflon and polycarbonate are particularly recommended; glass epoxy may be used if it is protected with a silicone or epoxy coating to prevent moisture absorption. If operation at high humidities is required, this coating will be desirable anyway to control surface leakage. All residues of previous operations, such as soldering flux, inks, and resists, must of course be thoroughly removed before coating.

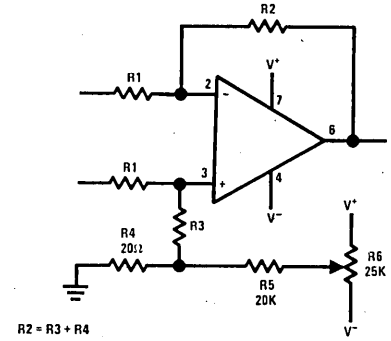


FIGURE 7. Universal Offset Trim

Another approach which has been successfully used with the TO-5 amplifiers is to terminate all critical connections on Teflon standoff insulators. These may be interconnected as required with Teflon insulated wire, keeping connections as short as possible to minimize noise pick-up. A short length of Teflon tubing slipped over the wire from the amplifier prevents contact with the oversize hole in the mounting board. The remainder of the amplifier connections may be terminated conventionally, either to printed circuit lands or to other standoff insulators.

Input Guarding Improves System Performance

Even with properly cleaned and coated printed circuit boards, leakage currents can limit the circuit performance under severe environmental conditions. In most cases with the LH0052 family devices, leakage will be primarily to V^- as the inputs are between the offset null pin (which in normal operation runs at a voltage very near V^-) and the V^- pin itself. This would seem to predict that leakage into the inverting and non-inverting inputs should at least be of the same polarity, but the effects are too unpredictable to make much use of the cancellation which should occur.

These currents may be intercepted before they reach the amplifier inputs by a guard conductor in the leakage path operating at the same potential as the inputs. Resistance between the inputs and the guard will cause little current to flow because of the premise that the guard voltage equals the input voltage. Suggested board layouts for the various package types are shown in Figures 8 through 11.

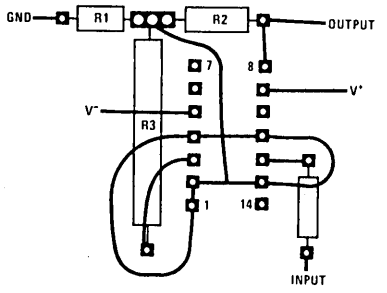


FIGURE 8. DIP Non-Inverting Amplifier PC Layout

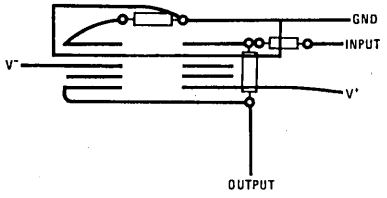


FIGURE 9. Flat Pack Inverting Amplifier PC Layout

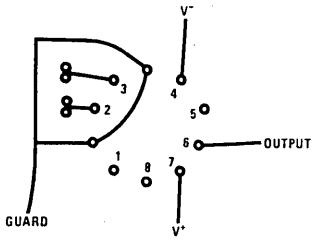


FIGURE 10. TO-5 – 10 Pin Pattern PC Layout

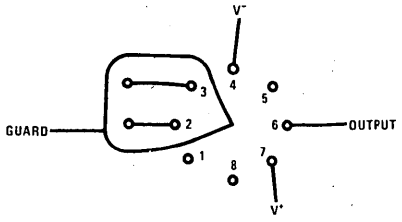


FIGURE 11. TO-5 – 8 Lead Pattern

The flat pack and dual-in-line packages have an unconnected pin on either side of the inputs. These may be used as shown, both to continue the guard into the package and as a convenient method of surrounding the inputs with a guard conductor without running a line between device pins. The

eight lead TO-5 package has only one spare pin, so the leads must either be formed into a 10 lead circle with two gaps, or the pin circle expanded sufficiently to allow a conductor to pass between device pins. If the board is double sided or multilayer, the guard pattern should be repeated on all conductor planes.

Figures 12 through 15 show how the guard is committed on the more common op amp circuits. With an integrator or inverting amplifier, where the inputs are close to ground potential, the guard is

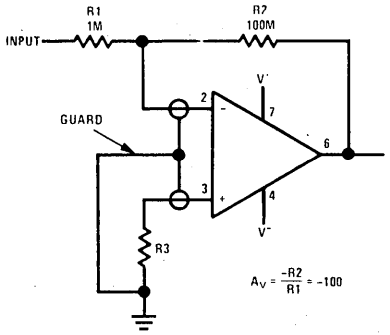


FIGURE 12. Guarded Inverting Amplifier

simply grounded. With the voltage follower, the guard is bootstrapped to the output. If it is desirable to put a resistor in the inverting input to compensate for the source resistance, it is connected as shown in Figure 13.

Guarding a non-inverting amplifier is a little more complicated. A low impedance point must be created by using relatively low value feedback resistors to determine the gain (R_1 and R_2 in Figure 14). The guard is then connected to the

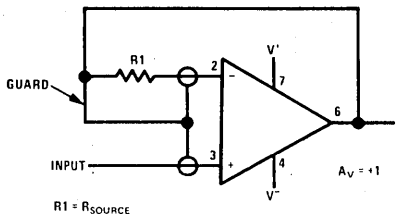


FIGURE 13. Guarded Voltage Follower

junction of the feedback resistors. Low impedance in this context means that expected leakage currents should not be capable of generating deleterious error voltages. A resistor, R_3, may be added to balance the source resistance and thus cancel the effect of bias current.

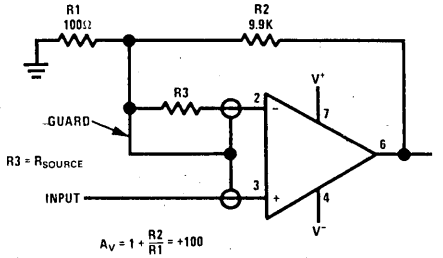


FIGURE 14. Guarded Non-Inverting Amplifier

The general case of a full differential configuration may require the use of a guard driver amplifier A_2 as shown in Figure 15. Resistors R_5 and R_6 develop the proper voltage for the guard at their junction, but it will normally be impractical to make them low enough resistance due to source

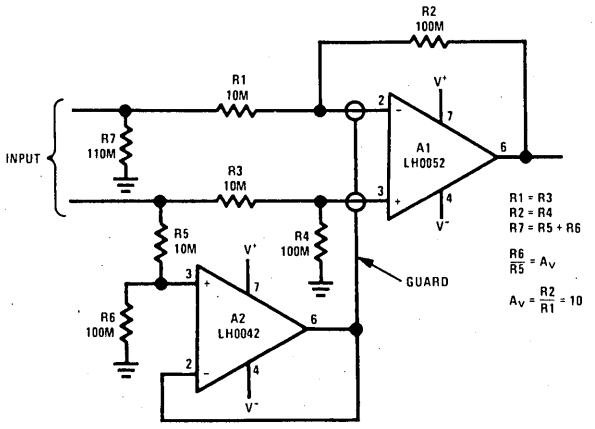


FIGURE 15. Guarded Full Differential Amplifier

loading. R_7 is included to balance the effect of R_5 plus R_6 and thus not degrade the closed loop common mode rejection.

Voltage Followers

The excellent common mode rejection and range of the amplifiers in this series suggest their use as unity gain voltage follower amplifiers. They perform well in this function with the one precaution shown on the circuit of Figure 16. The straightforward circuit with a direct feedback connection

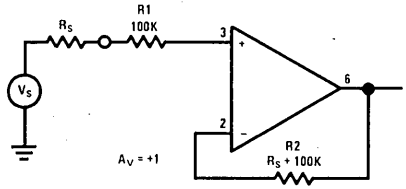


FIGURE 16. Unity Gain Voltage Follower

and no resistors will function, but if a low impedance signal having a slew rate faster than the amplifier can follow is applied to the input, a differential input voltage might be developed in excess of the absolute maximum. R_1 limits the current under these conditions to a safe value of 200 μA. R_2 is included to cancel the error voltage due to bias current and should in general be equal to the source resistance plus R_1.

For applications requiring voltage gain as well as high input impedance, a voltage divider may be included in the feedback path as in Figure 17. The voltage gain of this circuit is approximately $1 + R_2/R_3$ (neglecting amplifier open loop gain).

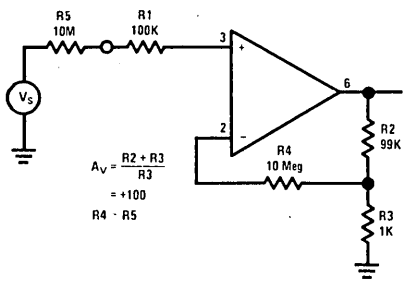


FIGURE 17. Non-Inverting Amplifier

R_4 is included as a convenient variable to equalize resistances in the two amplifier inputs: R_4 in series with the parallel combination of R_2 and R_3 should be set equal to the source resistance plus R_1. Note that all of these resistors may not be necessary depending on the required voltage gain, source impedance, accuracy requirement, temperature range, and amplifier selected.

Precision Integrator

The low input bias currents attainable with amplifiers of this series make them a natural choice for integrator applications requiring long time constants. Figure 18 illustrates a typical practical circuit. R_1 should be selected so that the total

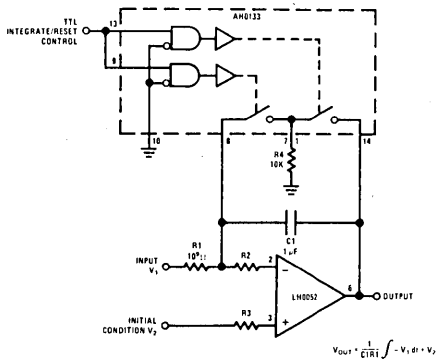


FIGURE 18. Precision Integrator

leakage current at the summing node is smaller than the signal current (V_1/R_1) by a margin sufficiant to insure the required accuracy, i.e. $V_1/R_1 >> I_{b1}$. C_1 should be chosen for low leakage, stability, accuracy, and low voltage coefficient. Polystyrene or polycarbonate dielectric is the best choice for capacitances up to about one microfarad, Teflon is good for the lower values.

R_2 is included to protect the input circuit during the reset transient, although many low speed applications will not require it at all. If the resistance of the reset switch is 100 ohms, the maximum current that could flow in C_1 is 10V/100 = 0.1 amp. In reality this may well be limited to a lower value by I_{DSS}, if the reset switch is an FET. Then the rate of change of voltage cannot exceed 0.1 amp/1 μF = 0.1 V/μs which is well within the slew rate capabilities of the amplifier. R_3, used to balance the resistance in the inputs, should be made equal to the sum of R_2 and the reset switch resistance.

Sample/Hold Amplifiers

The LH0052 family of amplifiers is well suited for use as a buffer amplifier in long hold-time sample/hold circuits. They may be used in any of the common configurations where improved hold performance is required. Figure 19A illustrates one circuit taking advantage of the low bias currents attainable. R_1 serves to bootstrap the connection between analog switch S_1 and S_2 so that there is essentially no voltage across S_1 in the hold mode. When S_1 and S_2 are closed to enter the sample mode, the effect of R_1 is slight as it is much higher resistance than the switches. After a long enough time, C_1 will charge to the input voltage, the amplifier will buffer it to the output, and both

ends of R_1 will be at the input potential so it will have no effect at all after the transient. Figure 19B illustrates an alternate circuit configuration with input buffer amplifier.

Re-Zeroing Amplifier

Figure 20 illustrates a technique which may be useful in situations where a signal has an unknown and variable DC offset, such as in telemetry. In operation, the re-zero command line is enabled while a ground reference signal is applied to the input of the system. This causes C_1 to charge to a level proportional to the system DC offset. When the re-zero line is deactivated, the amplifier behaves like a conventional inverting stage, subtracting off the system offset and giving a true ground referenced output.

If the total worst case leakage at the capacitor node is 1 nA, and if C_1 = 0.01 μF, then the drift rate is $10^{-9}/0.01 \cdot 10^{-6}$ = 0.1 V/s. For a 10 volt full scale system requiring an accuracy of 0.1% (10 mV), the amplifier would need a re-zeroing reference every 100 ms.

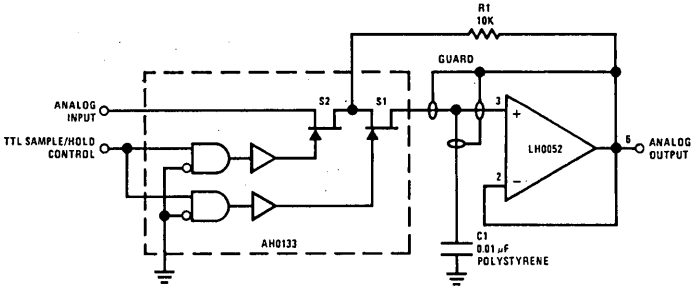


FIGURE 19A. Low Drift Sample/Hold

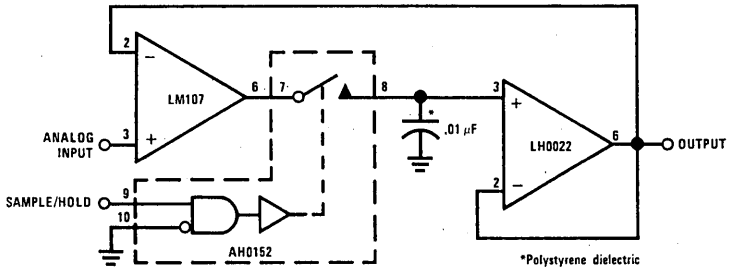


FIGURE 19B. Precision Sample and Hold

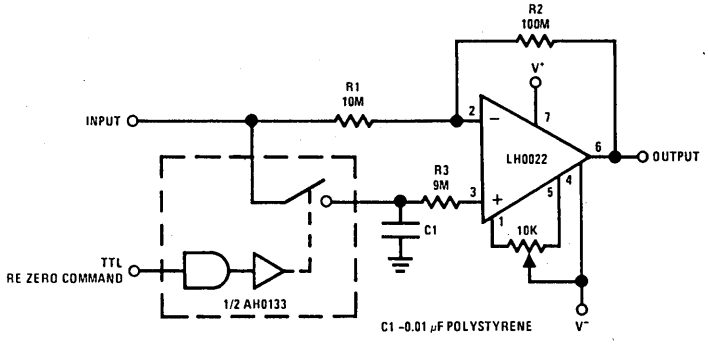


FIGURE 20. Re-Zeroing Amplifier

Precision Current Sink

Figure 21 illustrates a variation on a common technique for generating a precisely regulated current. This circuit could be used in conjunction with another FET input amplifier connected as a

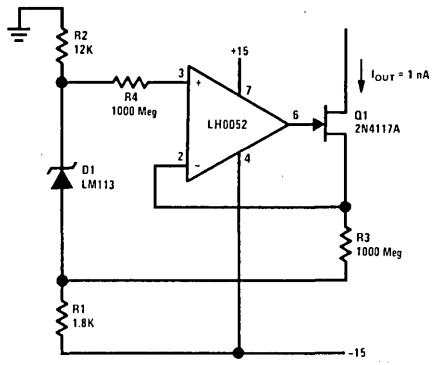


FIGURE 21. Precision Current Sink

high input impedance follower to form an ohmmeter for accurately measuring very high resistances. R_1, R_2 and D_1 form bias and reference voltages near, but within, the common mode and output voltage limits of the amplifier. Q_1 is selected for very low gate leakage so that the current in its source will be nearly identical to the feedback current in its drain. In operation, the amplifier output will cause the gate of Q_1 to be cut off however much is necessary to keep the voltage across R_3 equal to 1.220 volts, the breakdown voltage of D_1. The LM113 diode is available to an initial voltage accuracy of 1% (12.2 mV) and is guaranteed to drift less than 15 mV over the temperature range, thus by specifying the LH0052 amplifier and a 1% resistor, a current sink can be designed for a worst case initial accuracy near 2% and a drift over the temperature range of less than 2%. The technique may be applied over a wide range of currents by properly scaling R_3 and its balancing resistor R_4; a mirror image current source is possible using a P channel FET for Q_1.

Precision Comparator

FET amplifiers have a significant advantage over bipolar in precision voltage comparator applications: the input current is nearly independent of input voltage. With a bipolar input stage, input current is $1/\beta$ of the emitter current, but the emitter current can vary from zero when the stage is cut off to twice the nominal value when fully conducting. Furthermore, the inputs are often internally clamped to a diode drop for protection of the emitter base junctions.

As long as the input and reference signals are no more than 4 volts apart in the circuit of Figure 22, the input currents remain low and constant. This is an adequate signal range for many applications, especially in view of the offset voltage performance available in the top of the line amplifiers. If wider signal range is required, resistors R_1 and R_2 should be included to limit the input current to a safe value. Internal zener junctions will limit the differential input voltage to a safe value if the input current is limited 200 μA.

The output clamp circuit shown in Figure 22 will drive 3 standard TTL loads or 30 National low power TTL loads. Considerable power may be saved by increasing R_3 if full fan-out is not required. If only 2 low power loads are to be driven, the required low state output current is 360 μA, so R_3 = 10V/360 μA = 27k.

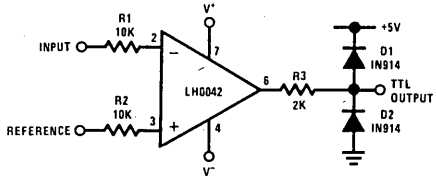


FIGURE 22. Precision Voltage Comparator

True Instrumentation Amplifier

Figure 23A illustrates an instrumentation amplifier that features high differential and common mode input resistance (10^{12} ohms), ±10V common mode and differential mode input range, .01% gain accuracy at A_V = 1000; and 110 dB CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 1 pA and offset drift is less than 5 μV/°C. R_1 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_2 is an initial trim used to maximize CMRR without using super precision matched resistors. Input common voltage is sensed via R_3 and R_4 and the LM110 provides low impedance V_{CM} drive to input cable shields to reduce leakage and coupling to inputs. If the input current of the LH0052 (1 pA max) is not low enough, additional circuitry as shown in figure 23B may be added to provide "Zero" input bias current.

Ultra Low Level Transconductance or Charge Amplifier

A picoamp amplifier for pH meters, medical electronics and radiation detectors is illustrated in Figure 24. A high quality glass sealed feedback resistor such as Victoreen type RX-1 should be employed as well as guard shielding as discussed earlier. Optionally C_1 may be added to convert the circuit to a charge amplifier with R_L used to provide DC stability.

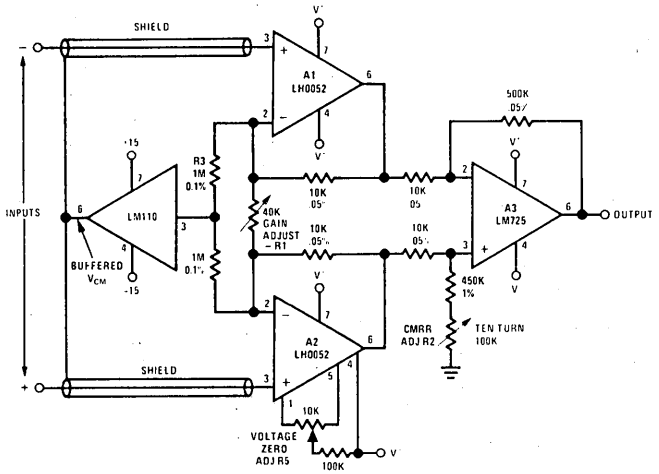


FIGURE 23A. True Instrumentation Amplifier

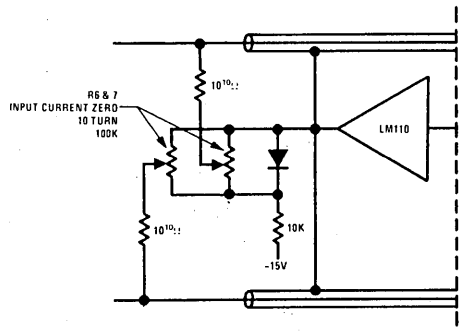


FIGURE 23B. Zero Input Bias Current

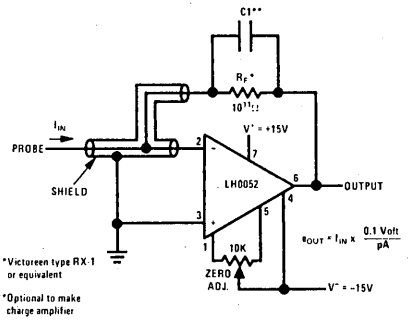


FIGURE 24. Picoamp Amplifier

Precision Subtractor for Automatic Test Gear

It is often necessary in testing linear circuits to take the difference between two voltage readings occurring at different times. The specialized sample/hold circuit shown in Figure 25 performs this function simply and accurately. Initially, S_1 and S_2 are closed and S_3 open with the logic input in the TTL "1" state. This allows capacitor C_1 to charge to the same voltage as the e_{IN1} input signal. When the logic input is taken to TTL "0", S_1 and S_2 open and S_3 closes, causing the difference between the stored value of e_{IN1} and the present value of e_{IN2} to appear at the non-inverting input of the LH0022.

The low leakage and high input impedance of the LH0022 allows the use of a reasonable size hold capacitor while at the same time providing gain for scaling, if needed. Note that the two analog inputs, e_{IN1} and e_{IN2} may be connected together to take the voltage difference on a single line at two different times. The disable input is used to open all switches, for example, to ignore a transient. If not needed, the disable input should be grounded.

Sensitive Low Cost "VTVM"

Figure 26 illustrates a modern approach to constructing VTVM's and VOM's. The LH0042 replaces all active circuitry. Optionally the circuit may be run off of 8 flashlight batteries and only draws 20 mW of power. The clever designer would add some more switching to allow operation of the FET op amp in transconductance mode as shown in Figure 24, thus combining both voltage and current measuring capability into the same circuit.

How to Build a FET Op Amp "Module"

The LH0052 series when compared spec for spec with modules usually offers superior performance and significantly lower cost. What's the difference between modules and these integrated circuit amplifiers? In most cases the answer is nothing but two .01 μF power supply decoupling capacitors. To make your own module merely build a small 1-1/4 x 1-1/4 printed circuit board that adapts the pin-out of the LH0052 to your module requirement. No need to pot the assembly in epoxy, the LH0052 family is completely heremetic and does not absorb moisture. Some modules specify higher output current capability than the ±10 mA of the LH0052. To build a ±100 mA output "module" FET op amp, simply add a LH0002 buffer as shown in Figure 27.

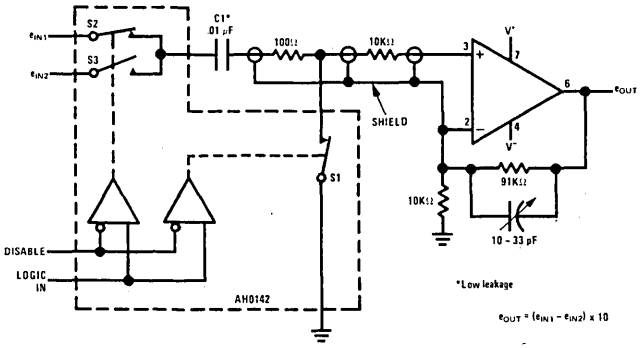


FIGURE 25. Precision Subtractor for Automatic Test Gear

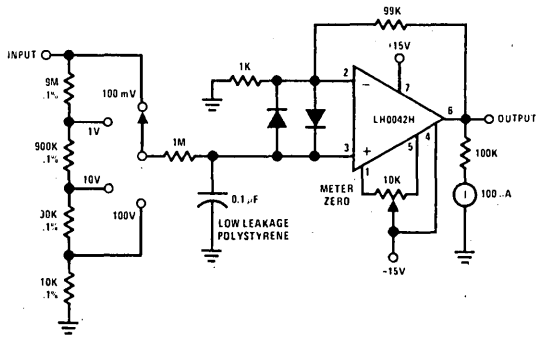


FIGURE 26. Sensitive Low Cost "VTVM"

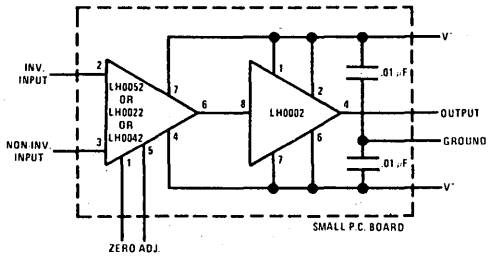
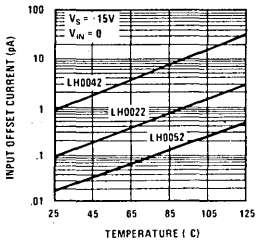


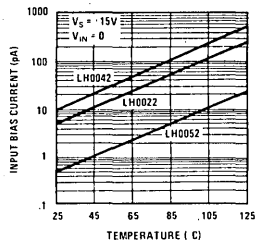
FIGURE 27. 100 mA Output FET Op Amp "Module"

Typical Performance Characteristics

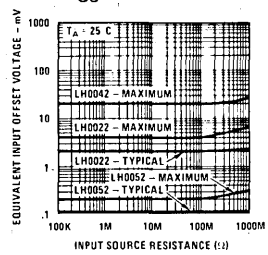
Input Offset Current vs Temperature



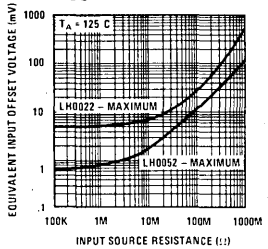
Input Bias Current vs Temperature



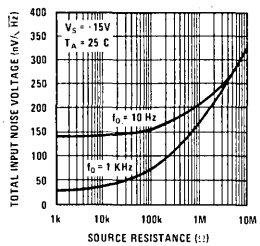
Offset Error (Without V_{OS} Null)



Offset Error (Without V_{OS} Null)

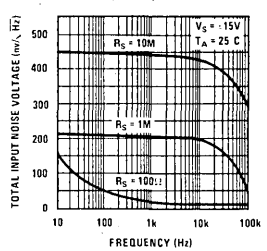


Total Input Noise Voltage* vs Source Resistance



*Noise Voltage Includes Contribution from Source Resistance

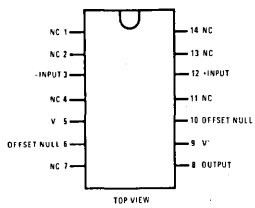
Total Input Noise Voltage* vs Frequency



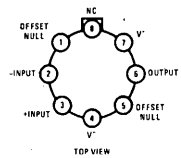
*Noise Voltage Includes Contribution from Source Resistor

Connection Diagrams

Dual-In-Line Package



Metal Can Package



TO-5

Conclusion

The practical advantages of the LH0052 series of FET input operational amplifiers has been demonstrated. The extremely low input bias and offset current make members of the family ideal choices for critical applications in hold amplifiers, active filters and instrumentation. The low input offset voltage and drift, high open loop gain, and excellent common mode rejection combine to make the devices equally well suited for general purpose applications including summers, subtractors, and oscillators.

References

1. R.J. Widlar *"IC Op Amps Equal Discretes"* National Semiconductor TP-9, December 1968
2. R.J. Widlar *"IC Op Amp Beats FETs on Input Current"* National Semiconductor AN-29, December 1969
3. D.L. Wollesen *"How to Bias the Monolithic JFET Dual"* National Semiconductor AN-34, March 1970
4. R.C. Dobkin *"Universal Balancing Techniques"* National Semiconductor LB-9, August 1969
5. W.S. Routh *"An Applications Guide for Operational Amplifiers"* National Semiconductor AN-20, February 1969
6. National Semiconductor Linear Applications Handbook

Applications for a High Speed FET Input Op Amp

National Semiconductor
Application Note 75
Barry Siegel

INTRODUCTION

The principal limitations in speed and bandwidth in IC FET input op amps have been reduced by over an order of magnitude with the introduction of the LH0062/LH0062C. Internal compensation assures unity gain stability with bandwidths in excess of 15 MHz. Voltage follower slew rate is typically 75V/μs and is guaranteed in excess of 50V/μs. Furthermore, external components may be used to extend the slew rate to 120V/μs and settling times under 1μs. The LH0062H (TO-5) is pin compatible with LM101, LM741 and LH0022. A summary of the LH0062's performance characteristics is given in Table 1.

PARAMETER (T_A = 25°C)	MIN	TYP	MAX	UNITS
Input Offset Voltage		2.0	5.0	mV
Input Bias Current			20	pA
Voltage Gain	50	100		V/mV
Slew Rate	50	75		V/μs
Bandwidth		15		MHz

TABLE 1. Summary of LH0062 Characteristics

CIRCUIT DESCRIPTION

The LH0062 is basically a two stage amplifier (Figure 1) consisting of a N channel junction FET input stage (Q_1 and Q_2) and a PNP output stage (Q_4 and Q_5). Q_1 and Q_2 are a well matched interdigitated monolithic pair that provide high common mode rejection and input offset voltage tracking usually associated only with bipolar designs. The current mirror (Q_6 and Q_7) converts to single ended operation in addition to providing active high impedance load for Q_4 and Q_5 thus providing high gain. Q_3 and D_1 provides a temperature compensated current source for the input stage and Q_8, Q_9, D_2 and D_3 form a class AB output buffer. Detailed schematic is illustrated in Figure 2. Note that the FET inputs are protected by 5V zener diodes and input current under transient conditions should be limited by inserting a 1k ohm or larger resistor in series with one of the inputs.

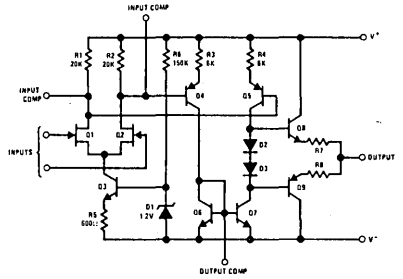


FIGURE 1. Simplified LH0062 Circuit Schematic

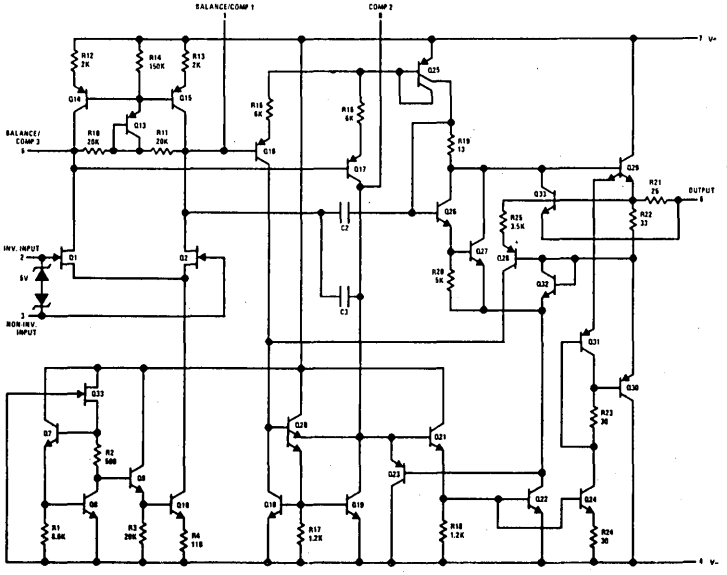


FIGURE 2. Complete LH0062 Schematic

COMPENSATION CONSIDERATIONS

As noted earlier, the LH0062 is internally compensated for unity gain stability. However, a few precautions are advised. Like most wide band amplifiers, the LH0062 is sensitive to power supply inductance, and decoupling the supplies with 0.1μF ceramic disc capacitors within an inch or two of the device will prevent spurious oscillations and save a fair amount of grief. The device is capable

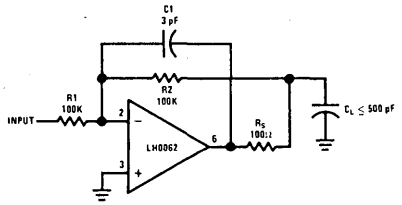


FIGURE 3. Isolating a Capacitive Load up to 500 pF

of driving 50 to 100 pF loads; for larger loads, an isolation resistor, R_3 as shown in Figure 3 is recommended. Alternatively, a current buffer such as the LH0002 or LH0033 may be used for loads in excess of 500 pF with no degradation in slew rate as shown in Figure 4.

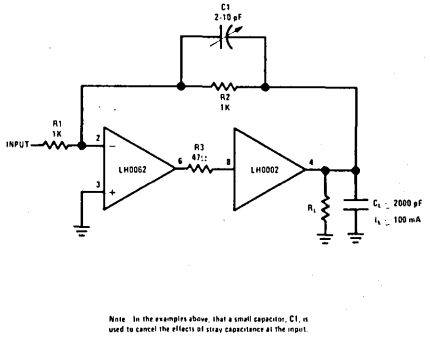


FIGURE 4. Driving Capacitances in Excess of 500 pF and Loads

The LH0062 may be feed-forward compensated in inverting mode applications as shown in Figure 5. This boosts slew rate to over 120V/μs and bandwidth to over 30 MHz. When full bandwidth is

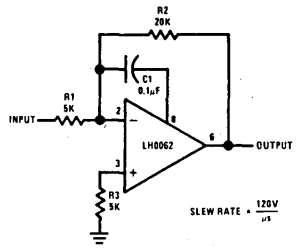


FIGURE 5. Feed Forward Compensation

not required, the device may be over-compensated as shown in Figure 6 to reduce bandwidth to 5 MHz. This technique improves phase margin and reduces susceptibility to spurious oscillations in applications where speed is less critical.

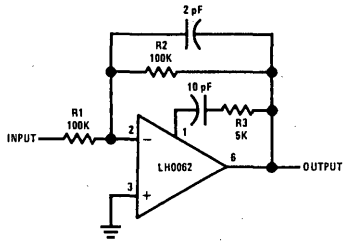


FIGURE 6. Overcompensation

Minimum settling time of less than 1μs to 0.1% for a 20V input step is obtained as illustrated in Figure 7. A small tweak capacitor, C_1 is recommended to cancel stray board layout capacitance, C_S. Once best value of trimmer capacitor C_1 is determined for a particular layout, it may be replaced with a fixed value.

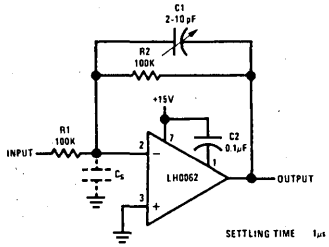


FIGURE 7. Compensation for Minimum Settling Time

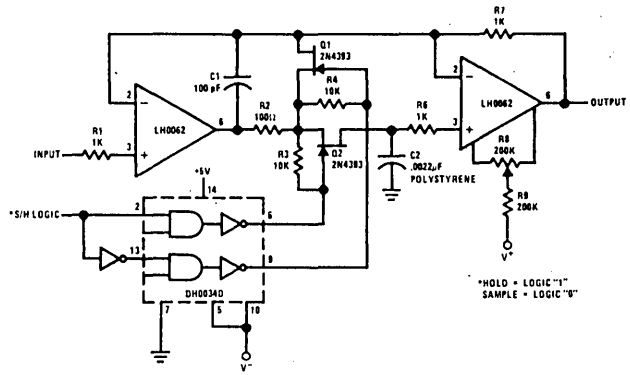


FIGURE 8. High Speed Sample & Hold

APPLICATIONS

The circuit of Figure 8 is a high speed sample and hold with sample acquisition time of 10μs for 0.1% accuracy and aperture time of approximately 25 ns. Resistor, R_6, is used to limit input current during power on and off transients. Although the inputs of the LH0062 are protected by back-to-back diodes excessive input current could damage the device. Resistor R_9 and the pot, R_8, allow null of the output offset with negligible effect on offset drift.

The peak detector of Figure 9 will acquire a +10V peak signal in under 4μs with droop rates under 20 mV/sec. Reversing the polarity of diodes D_1 and D_2 will allow peak detecting negative signals. Any ultra-low leakage diode may be substituted for the 2N930 collector-base junction.

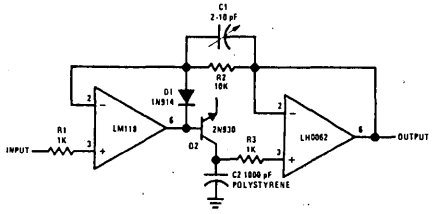


FIGURE 9. High Speed Peak Detector

The circuit of Figure 10 is a programmable integrator with a range in period from 1μs to 1 ms. For best results C_1 through C_4 should be low leakage construction such as polycarbonate or polystyrene. A simple method of implementing the offset adjustment is to momentarily insert a 100k ohm resistor between pins 2 and 6 of the LH0062. With the switches of the AH5009 off, the output may be set to zero with R_2.

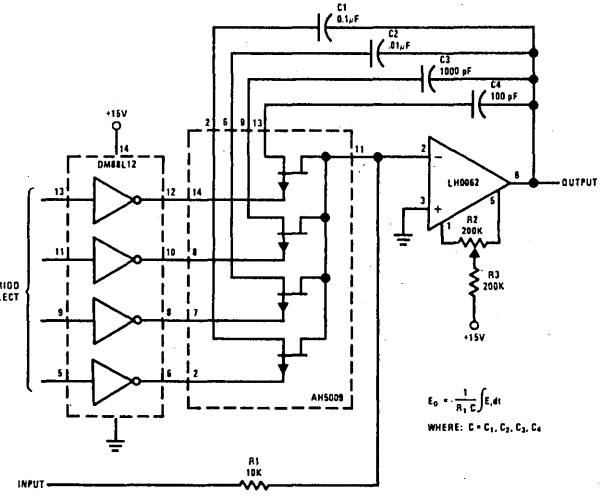


FIGURE 10. Programmable Integrator

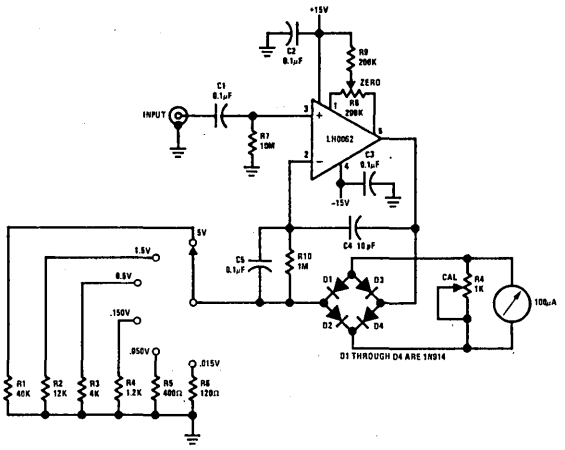


FIGURE 11. Wide Band AC Voltmeter

The circuit of Figure 11 is a wide band AC voltmeter capable of measuring AC signals as low as 15 mV at frequencies from 100 Hz to 500 kHz. Full scale sensitivity may be changed by altering the values R_1 through R_6 ($R \cong V_{IN}/100\mu A$).

HEAT SINKING, GUARDING, AND BOOTSTRAPPING

The LH0062 is specified for operation without an external heat sink. However, standby power is typically 240 mW causing a junction rise of approximately 60°C. A clip-on heat sink can reduce internal heating hence reduce input bias current from 20 pA at 25°C ambient to 2 or 3 pA.

Guarding input leads is recommended in stringent applications. An excellent discussion on guarding is given in AN-63 and the techniques discussed are directly applicable to the LH0062. Another benefit of guarding is reduced input capacitance. By bootstrapping the inputs, as shown in Figure 12, the apparent input capacitance is reduced to fractions of a pico-farad.

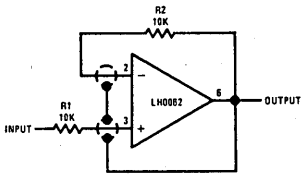


FIGURE 12. Guard/Bootstrap for Unity Gain

Furthermore, the case of the LH0062 is electrically isolated, and the output may be tied to case in order to eliminate stray capacitance introduced by the header.

REFERENCES

1. R. K. Underwood, *"New Design Techniques for FET Op Amps,"* National Semiconductor AN-63, March 1972.

2. R. C. Dobkin, *"LM118 Op Amp Slews 70V/μs,"* National Semiconductor LB-17, September 1971.

Applying Modern Clock Drivers to MOS Memories

National Semiconductor
Application Note 76
B. Siegel, M. Scott

INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input wave forms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types shift registers and RAM's (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of driver, monolithic integrated circuit drivers, the DS0025, DS0026 and DS0056 are selected as examples because of their low cost.

The DS0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage-gold doped process utilizing a collector sinker to minimize $V_{CE\,SAT}$.

The DS0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. The DS0056 is a variation of the DS0026 circuit which allows the system designer to modify the output performance of the circuit. The DS0056 can be connected (using a second power supply) to increase the positive output voltage level and reduce the effect of cross coupling capacitance between the clock lines in the system. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking required, reliability and cost. Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

TABLE I. DS0025 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		15	ns
t_{OFF}	C_{IN} = 0.0022μF, R_{IN} = 0Ω	30	ns
t_r	C_L = 0.0001μF, RO = 50Ω	25	ns
t_f		150	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 1.0$	V
On Supply Current (V^+)	I_{IN} = 10 mA	17	mA

TABLE II. DS0026 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		7.5	ns
t_{OFF}	C_{IN} = 0.001μF, R_{IN} = 0Ω	7.5	ns
t_r	RO = 50Ω, C_L = 1000 pF	25	ns
t_f		25	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = -1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 0.5$	V
On Supply Current (V^+)	I_{IN} = 10 mA	28	mA

The TO-5 ("H") package is rated at 750 mW still air (derate at 200°C/W above 25°C) soldered to PC board. This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on heat sink increases driving capability by 50%.

The 8-pin ("N") molded mini-DIP is rated at 600 mW still air (derate at 90°C/W above 25°C) soldered to PC board (derate at 1.39W). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

To TO-8 ("G") package is rated at 1.5W still air (derate at 100°C/W above 25°C) and 2.3W with clip-on heat sink (Wakefield type 215-1.9 or equivalent-derate at 15 mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

Additional information is given in the section of this data book on Maximum Power Dissipation (page 2).

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

1. Package and heat sink selection
2. Average dc power, P_{DC}
3. Average ac power, P_{AC}
4. Numbers of drivers per package, n

From the package heat sink, and maximum ambient temperature one can determine P_{MAX}, which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of dc power and ac power in each driver times the number of drivers. The total of which must be less than the package power rating.

$$P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \qquad (1)$$

Average dc power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

$$P_{DC} = P_{IN} + P_{OFF} + P_{ON} \qquad (2)$$

For most types of clock drivers, the first two terms are negligible (less than 10 mW) and may be ignored.

Thus:

$$P_{DC} \cong P_{ON} = \frac{(V^+ - V^-)^2}{Req} \times (DC)$$

where:

$V^+ - V^-$ = Total voltage across the driver

Req = Equivalent device resistance in the "ON" state

$$= V^+ - V^-/I_{S(ON)} \qquad (3)$$

DC = Duty Cycle

$$= \frac{\text{"ON" Time}}{\text{"ON" Time + "OFF" Time}}$$

For the DS0025, Req is typically 1 kΩ while Req is typically 600Ω for the DS0026. Graphical solutions for P_{DC} appear in *Figure 1.* For example if V^+ = +5V, V^- = −12V, Req = 500 Ω, and DC = 25%, then P_{DC} = 145 mW. However, if the duty cycle was only 5%, P_{DC} = 29 mW. Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.

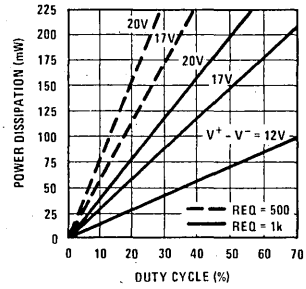


FIGURE 1. P_{DC} vs Duty Cycle

In addition to P_{DC}, the power driving a capacitive load is given approximately by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L \qquad (4)$$

where:

f = Operating frequency

C_L = Load capacitance

Graphical solutions for P_{AC} are illustrated in *Figure 2.* Thus, any type of clock driver will dissipate internally 290 mW per MHz per thousand pF of load. At 5 MHz, this would be 1.5W for a 1000 pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.

Combining equations (1), (2), (3) and (4) yields a criterion for the maximum load capacitance which can be driven by a given driver:

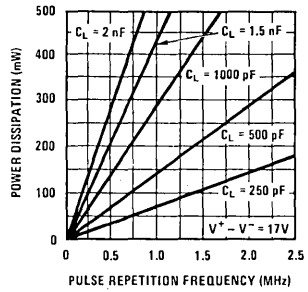


FIGURE 2. P_{AC} vs PRF

$$C_L \leq \frac{1}{f}\left[\frac{P_{MAX}}{n\,(V^+ - V^-)^2} - \frac{(DC)}{Req}\right] \quad (5)$$

As an example, the DS0025CN can dissipate 890 mW at T_A = 70°C when soldered to a printed circuit board. Req is approximately equal to 1k. For V^+ = 5V, V^- = −12V, f = 1 MHz, and dc = 20%, C_L is:

$$C_L \leq \frac{1}{10^6}\left[\frac{(890 \times 10^{-3})}{(2)(17)^2} - \frac{0.2}{1 \times 10^3}\right]$$

$$C_L \leq 1340 \text{ pF (each driver)}$$

A typical application might involve driving an MM5013 triple 64-bit shift register with the DS0025. Using the conditions above and the clock line capacitance of the MM5013 of 60 pF, a single DS0025 can drive 1340 pF/60 pF, or 00 MM5013's.

In summary, the maximum capacitive load that any clock driver can drive is determined by package type and rating, heat sink technique, maximum system ambient temperature, ac power (which depends on frequency, voltage across the device, and capacitive load) and dc power (which is principally determined by duty cycle).

Rise and Fall Time Considerations

In general rise and fall times are determined by (a) clock driver design, (b) reflected effects of heavy external load, and (C) peak transient current available. Details of these are included in Appendixes I and II. *Figures AI-3, AI-4, AII-2 and AIII-3* illustrate performance under various operating conditions. Under light loads, performance is determined by internal design of the driver; for moderate loads, by load C_L being reflected (usually as $C_{L/\beta}$) into the driver, and for large loads by peak output current where:

$$\frac{\Delta V}{\Delta T} = \frac{I_{OUT\ PEAK}}{C_L}$$

Logic rise and fall times must be known in order to assure non-overlap of system timing.

Note the definition of rise and fall times in this application note follow the convention that rise time is the transition from logic "0" to logic "1" levels and vice versa for fall times. Since MOS logic is inverted from normal TTL, "rise time" as used in this note is "voltage fall" and "fall time" is "voltage rise."

Power Supply Decoupling

Although power supply decoupling is a wide spread and accepted practice, the question often arises as to how much and how often. Our own experience indicates that each clock driver should have at least 0.1μF decoupling to ground at the V^+ and V^- supply leads. Capacitors should be located as close as is physically possible to each driver. Capacitors should be non-inductive ceramic discs. This decoupling is necessary because currents in the order of 0.5 to 1.5 amperes flow during logic transitions.

There is a high current transient (as high as 1.5A) during the output transition from high to low through the V^- lead. If the external interconnecting wire from the driving circuit to the V^- lead is electrically long, or has significant dc resistance the current transient will appear as negative feedback and subtract from the switching response. To minimize this effect, short interconnecting wires are necessary and high frequency power supply decoupling capacitors are required if V^- is different from the ground of the driving circuit.

Clock Line Overshoot and Cross Talk

Overshoot: The output waveform of a clock driver can, and often does, overshoot. It is particularly evident on faster drivers. The overshoot is due to the finite inductance of the clock lines. Since most MOS registers require that clock signals not exceed V_{SS}, some method must be found in large systems to eliminate overshoot. A straightforward approach is shown in *Figure 3.* In this instance,

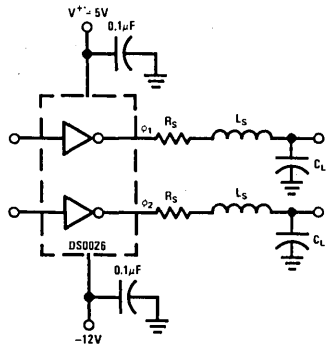


FIGURE 3. Use of Damping Resistor to Eliminate Clock Overshoot

a small damping resistor is inserted between the output of the clock driver and the load. The critical value for R_S is given by:

$$R_S = 2\sqrt{\frac{L_S}{C_L}} \qquad (6)$$

In practice, analytical determination of the value for R_S is rather difficult. However, R_S is readily determined empirically, and typical values range in value between 10 and 50Ω.

Use of the damping resistor has the added benefit of essentially unloading the clock driver; hence a greater number of loads may often be driven by a given driver. In the limit, however, the maximum value that may be used for R_S will be determined by the maximum allowable rise and fall time needed to assure proper operation of the MOS register. In short:

$$t_{r(MAX)} = t_{f(MAX)} \leq 2.2\ R_S C_L \qquad (7)$$

One last word of caution with regard to use of a damping resistor should be mentioned. The power dissipated in R_S can approach $(V^+ - V^-)^2 f C_L$ and accordingly the resistor wattage rating may be in excess of 1W. There are, obviously, applications where degradation of t_r and t_f by use of damping resistors cannot be tolerated. *Figure 4* shows a practical circuit which will limit overshoot to a diode drop. The clamp network should physically be located in the center of the distributed load in order to minimize inductance between the clamp and registers.

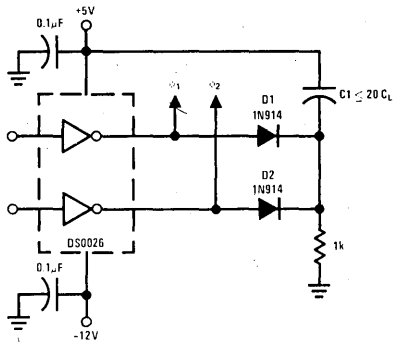


FIGURE 4. Use of High Speed Clamp to Limit Clock Overshoot

Cross Talk: Voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice versa) during the transition of ϕ_1 to MOS logic "1." The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. *Figure 5* illustrates the problem.

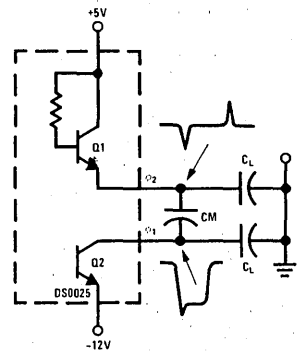


FIGURE 5. Clock Line Cross Talk

The negative going transition of ϕ_1 (to MOS logic "1") is capacitively coupled via C_M to ϕ_2. Obviously, the larger C_M is, the larger the spike. Prior to ϕ_1's transition, Q1 is "OFF" since only μA are drawn from the device.

The DS0056 connected as shown in *Figure 6* will minimize the effect of cross talk. The external resistors to the higher power supply pull the base of a Q1 up to a higher level and forward bias the collector base junction of Q1. In this bias condition the output impedance of the DS0056 is very low and will reduce the amplitude of the spikes.

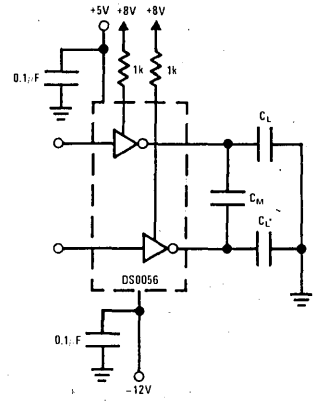


FIGURE 6. Use of DS0056 to Minimize Clock Line Cross Talk

Input Capacitive Coupling

Generally, MOS shift registers are powered from +5V and −12V supplies. A level shift from the TTL levels (+5V) to MOS levels (−12V) is therefore required. The level shift could be made utilizing a PNP transistor or zener diode. The disadvantage to dc level shifting is the increased power dissipation and propagation delay in the level shifting device. Both the DS0025, DS0026 and DS0056 utilize input capacitors when level shifting from

TTL to negative MOS capacitors. Not only do the capacitors perform the level shift function without inherent delay and power dissipation, but as will be shown later, the capacitors also enhance the performance of these circuits.

CONCLUSION

The practical aspects of driving MOS memories with low cost clock drivers has been discussed in detail. When the design guide lines set forth in this paper are followed and reasonable care is taken in circuit layout, the DS0025, DS0026 and DS0056 provide superior performance for most MOS input interface applications.

REFERENCES

1. Bert Mitchell, *"New MOS Clock Driver for MOS Shift Registers,"* National Semiconductor, AN-18, March 1969.

2. John Vennard, *"MOS Clock Drivers,"* National Semiconductor, MB-9, December 1969.

3. Dale Mrazek, *"MOS Delay Lines,"* National Semiconductor, AN-25, April 1969.

4. Dale Mrazek, *"MOS Clock Savers,"* National Semiconductor, MB-5.

5. Dale Mrazek, *"Silicon Disc's Challenge Magnetic Disc Memories,"* EDN/EEE Magazine, Sept. 1971.

6. Richard Percival, *"Dynamic MOS Shift Registers Can Also Simulate Stack and Silo Memories,"* Electronics Magazine, November 8, 1971.

7. Bapat and Mrazek, *"Dynamic MOS Random Access Memory System Considerations,"* National Semiconductor, AN-50, August 1971.

8. Don Femling, *"Using the MM5704 Keyboard Interface in Keyboard Systems,"* National Semiconductor, AN-52.

APPENDIX I

DS0025 Circuit Operation

The schematic diagram of the DS0025 is shown in *Figure AI-1.* With the TTL driver in the logic "0" state Q1 is "OFF" and Q2 is "ON" and the output is at approximately one V_{BE} below the V^+ supply.

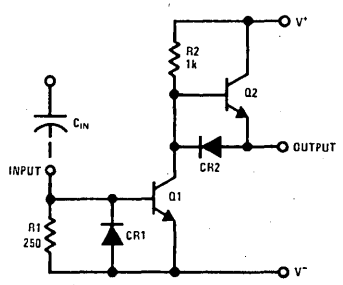


FIGURE AI-1. DS0026 Schematic (One-Half Circuit)

When the output of the TTL driver goes high, current is supplied to the base of Q1, through C_{IN}, turning it "ON." As the collector of Q1 goes negative, Q2 turns "OFF." Diode CR2 assures turn-on of Q1 prior to Q2's turn-off minimizing current spiking on the V^+ line, as well as providing a low impedance path around Q2's base emitter junction.

The negative voltage transition (to MOS logic "1") will be quite linear since the capacitive load will force Q1 into its linear region until the load is discharged and Q1 saturates. Turn-off begins when the input current decays to zero or the output of the TTL driver goes low. Q1 turns "OFF" and Q2 turns "ON" charging the load to within a V_{BE} of the V^+ supply.

Rise Time Considerations

The logic rise time (voltage fall) of the DS0025 is primarily a function of the ac load, C_L, the available input current and total voltage swing. As shown in *Figure AI-2,*

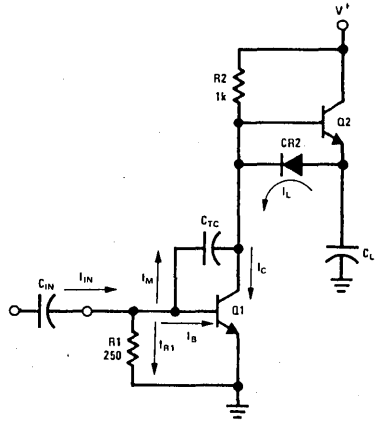


FIGURE AI-2. Rise Time Model for the DS0025

the input current must charge the Miller capacitance of Q1, C_{TC}, as well as supply sufficient base drive to Q1 to discharge C_L rapidly. By inspection:

$$I_{IN} = I_M + I_B + I_{R1} \qquad \text{(AI-1)}$$

$$I_{IN} \cong I_M + I_B, \text{ for } I_M >> I_{R1} \text{ \& } I_B >> I_{R1}$$

$$I_B = I_{IN} - C_{TC} \frac{\Delta V}{\Delta t} \qquad \text{(AI-2)}$$

If the current through R2 is ignored,

$$I_C = I_B h_{FEQ1} = I_L + I_M \qquad \text{(AI-3)}$$

where:

$$I_L = C_L \frac{\Delta V}{\Delta t}$$

Combining equations AI-1, AI-2, AI-3 yields:

$$\frac{\Delta V}{\Delta t}[C_L + C_{TC}(h_{FEQ1} + 1)] = h_{FEQ1} I_{IN} \qquad \text{(AI-4)}$$

or

$$t_r \cong \frac{[C_L + (h_{FEQ1} + 1)C_{TC}]\,\Delta V}{h_{FEQ1} I_{IN}} \qquad \text{(AI-5)}$$

Equation (AI-5) may be used to predict t_r as a function of C_L and ΔV. Values for C_{TC} and h_{FE} are 10 pF and 25 respectively. For example, if a DM7440 with peak output current of 50 mA were used to drive a DS0025 loaded with 1000 pF, rise times of:

$$\frac{(1000\text{ pF} + 250\text{ pF})\,(17\text{V})}{(50\text{ mA})\,(20)}$$

or 21 ns may be expected for $V^+ = 5.0V$, $V^- = -12V$, *Figure AI-3* gives rise time for various values of C_L.

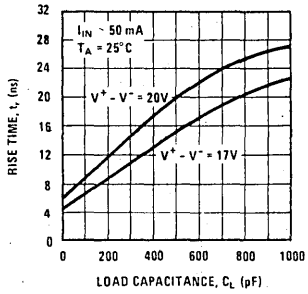


FIGURE AI-3. Rise Time vs C_L for the DS0025

Fall Time Considerations

The MOS logic fall time (voltage rise) of the DS0025 is dictated by the load, C_L, and the output capacitance of Q1. The fall time equivalent circuit of DS0025 may be approximated with the circuit of *Figure AI-4*. In actual

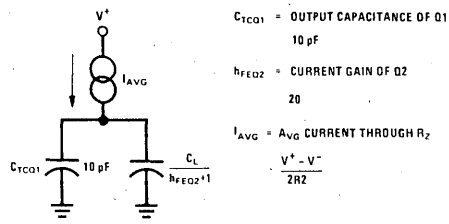


FIGURE AI-4. Fall Time Equivalent Circuit

practice, the base drive to Q2 drops as the output voltage rises toward V^+. A rounding of the waveform occurs as the output voltage reaches to within a volt of V^+. The result is that equation (AI-7) predicts conservative values of t_f for the output voltage at the beginning of the voltage rise and optimistic values at the end. *Figure AI-5* shows t_f as function of C_L.

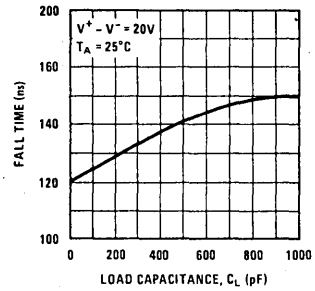


FIGURE AI-5. DS0025 Fall Time vs C_L

Assuming h_{FE2} is a constant of the total transition:

$$\frac{\Delta V}{\Delta t} = \frac{\left(\frac{V^+ - V^-}{2R2}\right)}{C_{TCQ1} + C_L/h_{FEQ1+1}} \qquad \text{(AI-6)}$$

or

$$t_f \cong 2R2\left(C_{TCQ1} + \frac{C_L}{h_{FEQ+1}}\right) \qquad \text{(AI-7)}$$

DS0025 Input Drive Requirements

Since the DS0025 is generally capacitively coupled at the input, the device is sensitive to current not input voltage. The current required by the input is in the 50–60 mA region. It is therefore a good idea to drive the DS0025 from TTL line drivers, such as the DM7440 or DM8830. It is possible to drive the DS0025 from standard 54/74 series gates or flip-flops but t_{ON} and t_r will be somewhat degraded.

Input Capacitor Selection

The DS0025 may be operated in either the logically controlled mode (pulse width out ≅ pulse width in) or C_{IN} may be used to set the output pulse width. In the latter mode a long pulse is supplied to the DS0025.

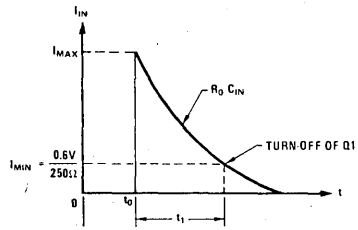


FIGURE AI-6. DS0025 Input Current Waveform

The input current is of the general shape as shown in *Figure AI-6*. I_{MAX} is the peak current delivered by the TTL driver into a short circuit (typically 50–60 mA). Q1 will begin to turn-off when I_{IN} decays below V_{BE}/R1 or about 2.5 mA. In general:

$$I_{IN} = I_{MAX}\, e^{-t/R0\, C_{IN}} \qquad \text{(AI-8)}$$

where:

R0 = Output impedance of the TTL driver

C_{IN} = Input coupling capacitor

Substituting $I_{IN} = I_{MIN} = \frac{V_{BE}}{R1}$ and solving for t_1 yields:

$$t_1 = R0C_{IN}\ \ln\ \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-9)}$$

The total pulse width must include rise and fall time considerations. Therefore, the total expression for pulse width becomes:

$$t_{PW} \cong \frac{t_r + t_f}{2} + t_1$$

$$= \frac{t_r + t_f}{2} + R0C_{IN}\ln\ \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-10)}$$

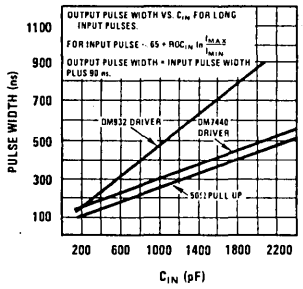


FIGURE AI-7. Output PW Controlled by C_{IN}

The logic "1" output impedance of the DM7440 is approximately 65Ω and the peak current (I_{MAX}) is about 50 mA. The pulse width for C_{IN} = 2,200 pF is:

$$t_{PW} \cong \frac{25\text{ ns} + 150\text{ ns}}{2} + (65\Omega)(2200\text{ pF})\ \ln$$

$$\frac{50\text{ mA}}{2.5\text{ mA}} = 517\text{ ns}$$

A plot of pulse width for various types of drivers is shown in *Figure AI-7*. For applications in which the output pulse width is logically controlled, C_{IN} should be chosen 2 to 3 times larger than the maximum pulse width dictated by equation (AI-10).

DC Coupled Operation

The DS0025 may be direct-coupled in applications when level shifting to a positive value only. For example, the MM1103 RAM typically operates between ground and +20V. The DS0025 is shown in *Figure AI-8* driving the addres or precharge line in the logically controlled mode.

If DC operation to a negative level is desired, a level translator such as the DS7800 or DS0034 may be employed as shown in *Figure AI-9*. Finally, the level shift may be accomplished using PNP transistors are shown in *Figure AI-10*.

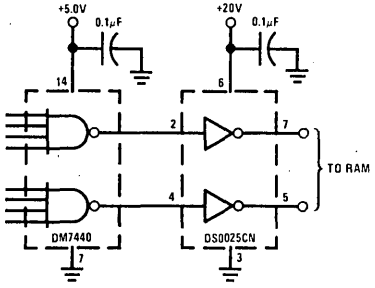


FIGURE AI-8. DC Coupled DS0025 Driving 1103 RAM

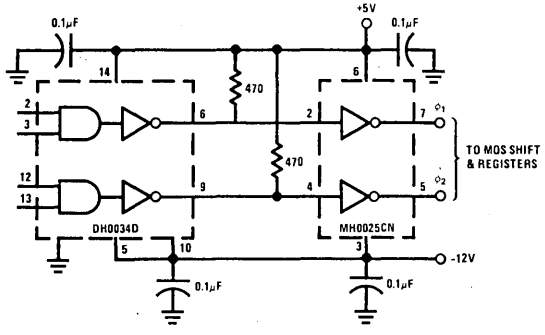


FIGURE AI-9. DC Coupled Clock Driver Using DS0034

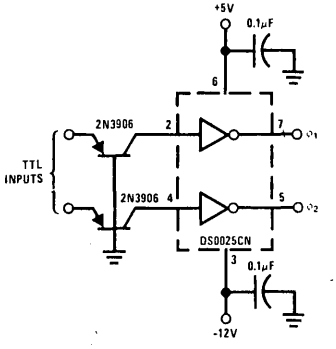


FIGURE AI-10. Transistor Coupled DS0025 Clock Driver

APPENDIX II

DS0026 Circuit Operation

The schematic of the DS0026 is shown in *Figure AII-1*. The device is typically ac coupled on the input and responds to input current as does the DS0025. Internal current gain allows the device to be driven by standard TTL gates and flip-flops.

With the TTL input in the low state Q1, Q2, Q5, Q6 and Q7 are "OFF" allowing Q3 and Q4 to come "ON." R6 assures that the output will pull up to within a V_{BE} of V^+ volts. When the TTL input starts toward logic "1," current is supplied via C_{IN} to the bases of Q1 and Q2 turning them "ON." Simultaneously, Q3 and Q4 are snapped "OFF." As the input voltage rises (to about 1.2V), Q5 and Q6 turn-on. Multiple emitter transistor Q5 provides additional base drive to Q1 and Q2 assuring their complete and rapid turn-on. Since Q3 and Q4 were rapidly turned "OFF" minimal power supply current spiking will occur when Q7 comes "ON."

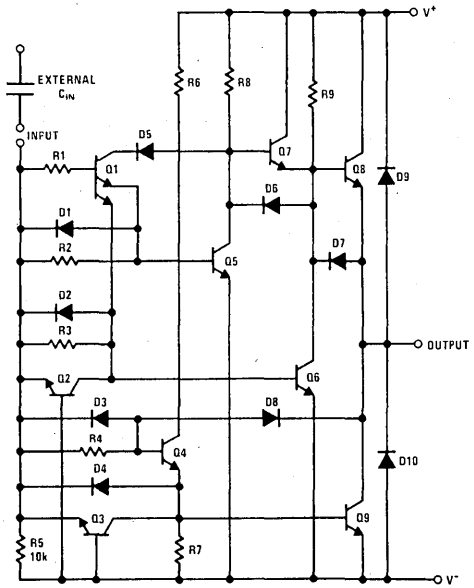


FIGURE AII-1. DS0025 Schematic (One-Half Circuit)

Q6 now provides sufficient base drive to Q7 to turn it "ON." The load capacitance is then rapidly discharged toward V^-. Diode D4 affords a low impedance path to Q6's collector which provides additional drive to the load through current gain of Q7. Diodes D1 and D2 prevent avalanching Q3's and Q4's base-emitter junction as the collectors of Q1 and Q2 go negative. The output of the DS0026 continues negative stopping about 0.5V more positive than V^-.

When the TTL input returns to logic "0," the input voltage to the DS0026 goes negative by an amount proportional to the charge on C_{IN}. Transistors Q8 and Q9 turn-on, pulling stored base charge out of Q7 and Q2 assuring their rapid turn-off. With Q1, Q2, Q6 and Q7 "OFF," Darlington connected Q3 and Q4 turn-on and rapidly charge the load to within a V_{BE} of V^+.

Rise Time Considerations

Predicting the MOS logic rise time (voltage fall) of the DS0026 is considerably involved, but a reasonable approximation may be made by utilizing equation (AI-5), which reduces to:

$$t_r \cong [C_L + 250 \times 10^{-12}]\ \Delta V \qquad \text{(AII-1)}$$

For C_L = 1000 pF, V^+ = 5.0V, V^- = −12V, $t_r \cong$ 21 ns. *Figure AII-2* shows DS0026 rise times vs C_L.

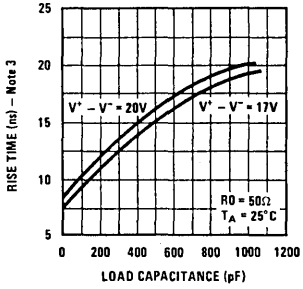


FIGURE AII-2. Rise Time vs Load Capacitance

Fall Time Considerations

The MOS logic fall time of the DS0026 is determined primarily by the capacitance Miller capacitance of Q5 and Q1 and R5. The fall time may be predicted by:

$$t_f \cong (2.2)(R5)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \cong (4.4 \times 10^3)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \qquad \text{(AII-2)}$$

where:

C_S = Capacitance to ground seen at the base of Q3

= 2 pF

$h_{FE}{}^2 = (h_{FEQ3} + 1)(h_{FEQ4} + 1)$

$\cong$ 500

For the values given and C_L = 1000 pF, $t_f \cong$ 17.5 ns. *Figure AII-3* gives t_f for various values of C_L.

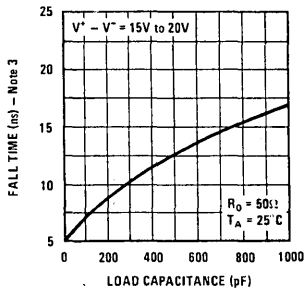


FIGURE AII-3. Fall Time vs Load Capacitance

DS0026 Input Drive Requirements

The DS0026 was designed to be driven by standard 54/74 elements. The device's input characteristics are shown in *Figure AII-4*. There is breakpoint at $V_{IN} \cong$ 0.6V which corresponds to turn-on of Q1 and Q2. The input current then rises with a slope of about 600Ω (R2 || R3) until a second breakpoint at approximately 1.2V is encountered, corresponding to the turn-on of Q5 and Q6. The slope at this point is about 150Ω (R1 || R2 || R3 || R4).

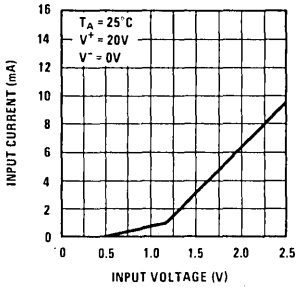


FIGURE AII-4. Input Current vs Input Voltage

The current demanded by the input is in the 5–10 mA region. A standard 54/74 gate can source currents in excess of 20 mA into 1.2V. Obviously, the minimum "1" output voltage of 2.5V under these conditions cannot be maintained. This means that a 54/74 element must be dedicated to driving 1/2 of a DS0026. As far as the DS0026 is concerned, the current is the determining turn-on mechanism not the voltage output level of the 54/74 gate.

Input Capacitor Selection

A major difference between the DS0025 and DS0026 is that the DS0026 requires that the output pulse width be logically controlled. In short, the input pulse width ≅ output pulse width. Selection of C_{IN} boils down to choosing a capacitor small enough to assure the capacitor takes on nearly full charge, but large enough so that the input current does not drop below a minimum level to keep the DS0026 "ON." As before:

$$t_1 = R0C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AII-3)}$$

or

$$C_{IN} = \frac{t_1}{R0 \ln \frac{I_{MAX}}{I_{MIN}}} \qquad \text{(AII-4)}$$

In this case R0 equals the sum of the TTL gate output impedance plus the input impedance of the DS0026 (about 150Ω). I_{MIN} from *Figure AII-5* is about 1 mA. A standard 54/74 series gate has a high state output impedance of about 150Ω in the logic "1" state and an output (short circuit) current of about 20 mA into 1.2V. For an output pulse width of 500 ns,

$$C_{IN} = \frac{500 \times 10^{-9}}{(150\Omega + 150\Omega) \ln \frac{20\text{ mA}}{1\text{ mA}}} = 560\text{ pF}$$

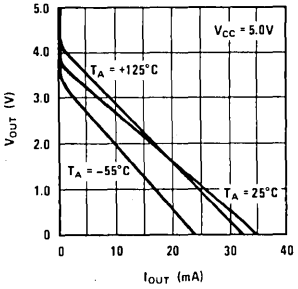


FIGURE AII-5. Logical "1" Output Voltage vs Source Current

In actual practice it's a good idea to use values of about twice those predicted by equation (AII-4) in order to account for manufacturing tolerances in the gate, DS0026 and temperature variations.

A plot of optimum value for C_{IN} vs desired output pulse width is shown in *Figure AII-6*.

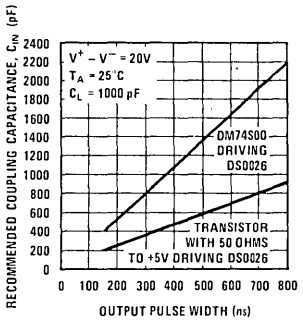


FIGURE AII-6. Suggested Input Capacitance vs Output Pulse Width

DC Coupled Applications

The DS0026 may be applied in direct coupled applications. *Figure AII-7* shows the device driving address or pre-charge lines on an MM1103 RAM.

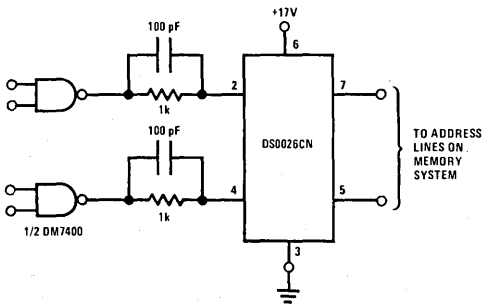


FIGURE AII-7. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

For applications requiring a dc level shift, the circuit of *Figure AII-8 or AII-9* are recommended.

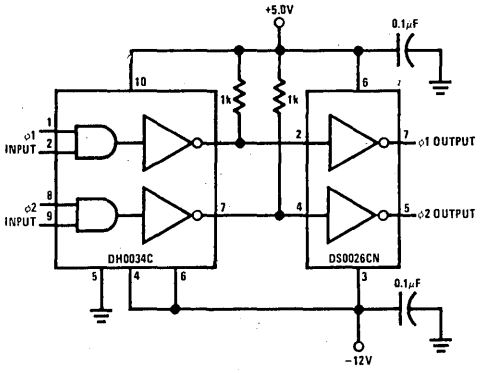


FIGURE AII-8. Transistor Coupled MOS Clock Driver

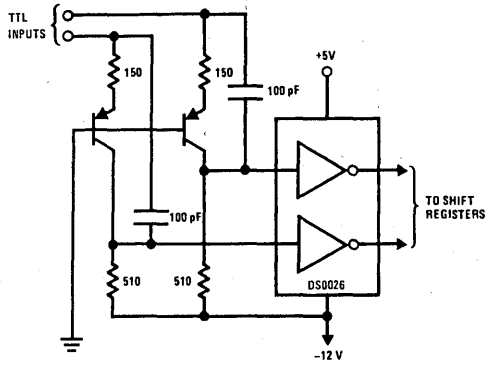


FIGURE AII-9. DC Coupled MOS Clock Driver

APPENDIX III

MOS Interface Circuits

MOS Clock Drivers

MH0007	Direct coupled, single phase, TTL compatible clock driver.
MH0009	Two phase, direct or ac coupled clock driver.
MH0012	10 MHz, single phase direct coupled clock driver.
MH0013	Two phase, ac coupled clock driver.
DS0025	Low cost, two phase clock driver.
DS0026	Low cost, two phase, high speed clock driver.
DS1671	Dual bootstrapped MOS driver.
DS1672	Dual TTL bootstrapped MOS driver.
DS1673	Quad decoded MOS clock driver.
DS1674	Quad MOS clock driver.
DS75361	Dual TTL-to-MOS driver.
DS75365	Quad TTL-to-MOS driver.

MOS Oscillator/Clock Drivers

DS7803/DS7807, DS7813/DS7817	Complete two phase clock system for MOS microprocessors and calculators.

MOS RAM Memory Address and Precharge Drivers

DS0025	Dual address and precharge driver.
DS0026	Dual high speed address and precharge driver.

TTL to MOS Interface

DH0034	Dual high speed TTL to negative level converter.
DS7800	Dual TTL to negative level converter.
DM7810/DM7812/ DM7819	Open collector TTL to positive high level MOS converter gates.
DM78L12	Active pull-up TTL to positive high level MOS converter gates.
DS1640/DS1670	Quad MOS TRI-SHARE™ driver.
DS1645/DS1675	Hex TRI-STATE® MOS driver.
DS1646/DS1676	6-bit TRI-STATE MOS driver refresh counter.
DS1647/DS1677	Quad TRI-STATE MOS driver I/O register.
DS1648/DS1678	TRI-STATE MOS driver multiplexer.
DS1649/DS1679	Hex TRI-STATE MOS driver.
DS16149/DS16179	Hex TRI-STATE MOS driver.

MOS to TTL Converters and Sense Amps

DS7802, DS7806*	Dual sense amp for MM5262 2k MOS RAM memory.
DS165 Series*	Hex sense amp MOS to TTL.
DS163, DS75107, DS75207*	Dual sense amp for MM1103 1k MOS RAM memory.

Voltage Regulators for MOS Systems

LM109, LM140 Series	Positive regulators.
LM120 Series	Negative regulators.
LM125 Series*	Dual +/– regulators.

*To be announced

Specifying A/D and D/A Converters

National Semiconductor
Application Note 156
Jim Sherwin

The specification or selection of analog-to-digital (A/D) or digital-to-analog (D/A) converters can be a chancey thing unless the specifications are understood by the person making the selection. Of course, you know you want an accurate converter of specific resolution; but how do you insure that you get what you want? For example, 12 switches, 12 arbitrarily valued resistors, and a reference will produce a 12-bit DAC exhibiting 12 quantum steps of output voltage. In all probability, the user wants something better than the expected performance of such a DAC. Specifying a 12-bit DAC or an ADC must be made with a full understanding of accuracy, linearity, differential linearity, monotonicity, scale, gain, offset, and hysteresis errors.

This note explains the meanings of and the relationships between the various specifications encountered in A/D and D/A converter descriptions. It is intended that the meanings be presented in the simplest and clearest practical terms. Included are transfer curves showing the several types of errors discussed. Timing and control signals and several binary codes are described as they relate to A/D and D/A converters.

MEANING OF PERFORMANCE SPECS

Resolution describes the smallest standard incremental change in output voltage of a DAC or the amount of input voltage change required to increment the output of an ADC between one code change and the next adjacent code change. A converter with n switches can resolve 1 part in 2^n. The least significant increment is then 2^{-n}, or one least significant bit (LSB). In contrast, the most significant bit (MSB) carries a weight of 2^{-1}. Resolution applies to DACs and ADCs, and may be expressed in percent of full scale or in binary bits. For example, an ADC with 12-bit resolution could resolve 1 part in 2^{12} (1 part in 4096) or 0.0245% of full scale. A converter with 10V full scale could resolve a 2.45mV input change. Likewise, a 12-bit DAC would exhibit an output voltage change of 0.0245% of full scale when the binary input code is incremented one binary bit (1 LSB). Resolution is a design parameter rather than a performance specification; it says nothing about accuracy or linearity.

Accuracy is sometimes considered to be a non-specific term when applied to D/A or A/D converters. A linearity spec is generally considered as more descriptive. An accuracy specification describes the worst case deviation of the DAC output voltage from a straight line drawn between zero and full scale; it includes all errors. A 12-bit DAC could not have a conversion accuracy better than ±½ LSB or ±1 part in 2^{12+1} (±0.0122% of full scale due to finite resolution). This would be the case in figure 1 if there were no errors. Actually, ±0.0122% FS represents a deviation from 100% accuracy; therefore accuracy should be specified as 99.9878%. However, convention would dictate 0.0122% as being an accuracy spec rather than an inaccuracy (tolerance or error) spec.

Accuracy as applied to an ADC would describe the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. If a 12-bit ADC is stated to be ±1 LSB accurate, this is equivalent to ±0.0245% or twice the minimum possible quantizing error of 0.0122%. An accuracy spec describes the maximum sum of all errors including quantizing error, but is rarely provided on data sheets as the several errors are listed separately.

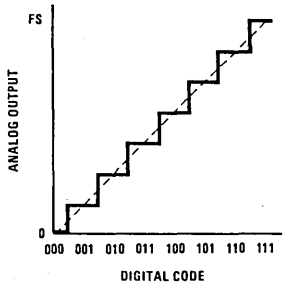
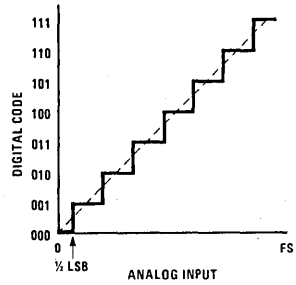


FIGURE 1. Linear DAC Transfer Curve Showing Minimum Resolution Error and Best Possible Accuracy

Quantizing Error is the maximum deviation from a straight line transfer function of a perfect ADC. As, by its very nature, an ADC quantizes the analog input into a finite number of output codes, only an infinite resolution ADC would exhibit zero quantizing error. A perfect ADC, suitably offset ½ LSB at zero scale as shown in figure 2, exhibits only ±½ LSB maximum output error. If not offset, the error will be $\overline{+0}^{1}$ LSB as shown in figure 3. For example, a perfect 12-bit ADC will show a ±½ LSB error of ±0.0122% while the quantizing error of an 8-bit ADC is ±½ part in 2^8 or ±0.195% of full scale. Quantizing error is not strictly applicable to a DAC; the equivalent effect is more properly a resolution error.



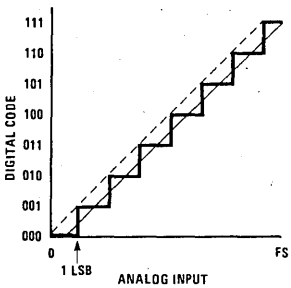


FIGURE 3. ADC Transfer Curve, No Offset

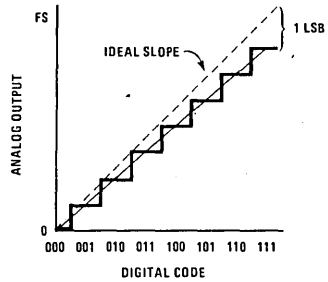


FIGURE 4. Linear, 1 LSB Scale Error

Gain Error is essentially the same as scale error for an ADC. In the case of a DAC with current and voltage mode outputs, the current output could be to scale while the voltage output could exhibit a gain error. The amplifier feedback resistors would be trimmed to correct the gain error.

Offset Error (zero error) is the output voltage of a DAC with zero code input, or it is the required mean value of input voltage of an ADC to set zero code out. (See figure 5.) Offset error is usually caused by amplifier or comparator input offset voltage or current; it can usually be trimmed to zero with an offset zero adjust potentiometer external to the DAC or ADC. Offset error may be expressed in % FS or in fractional LSB.

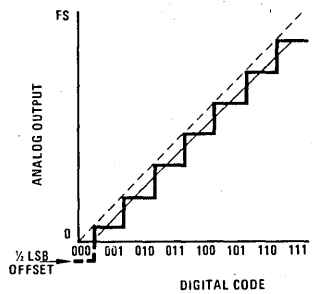


FIGURE 2. ADC Transfer Curve, ½ LSB Offset at Zero

Scale Error (full scale error) is the departure from design output voltage of a DAC for a given input code, usually full-scale code. (See figure 4.) In an ADC it is the departure of actual input voltage from design input voltage for a full-scale output code. Scale errors can be caused by errors in reference voltage, ladder resistor values, or amplifier gain, *et. al.* (See **Temperature Coefficient.**) Scale errors may be corrected by adjusting output amplifier gain or reference voltage. If the transfer curve resembles that of figure 7, a scale adjustment at ¾ scale could improve the overall ± accuracy compared to an adjustment at full scale.

Hysteresis Error in an ADC causes the voltage at which a code transition occurs to be dependent upon the direction from which the transition is approached. This is usually caused by hysteresis in the comparator inside an ADC. Excessive hysteresis may be reduced by design; however, some slight hysteresis is inevitable and may be objectionable in converters if hysteresis approaches ½ LSB.

Linearity, or, more accurately, non-linearity specifications describe the departure from a linear transfer curve for either an ADC or a DAC. Linearity error does not include quantizing, zero, or scale errors. Thus, a specifi-

cation of ±½ LSB linearity implies error in addition to the inherent ±½ LSB quantizing or resolution error. In reference to figure 2, showing no errors other than quantizing error, a linearity error allows for one or more of the steps being greater or less than the ideal shown.

Figure 6 shows a 3-bit DAC transfer curve with no more than ±½ LSB non-linearity, yet one step shown is of zero amplitude. This is within the specification, as the maximum deviation from the ideal straight line is ±1 LSB (½ LSB resolution error plus ½ LSB non-linearity). With any linearity error, there is a differential non-linearity (see below). A ±½ LSB linearity spec guarantees monotonicity (see below) and ⩽ ±1 LSB differential non-linearity (see below). In the example of figure 6, the code transition from 100 to 101 is the worst possible non-linearity, being the transition from 1 LSB high at code 100 to 1 LSB low at 110. Any fractional non-linearity beyond ±½ LSB will allow for a non-monotonic transfer curve. Figure 7 shows a typical non-linear curve; non-linearity is 1¼ LSB yet the curve is smooth and monotonic.

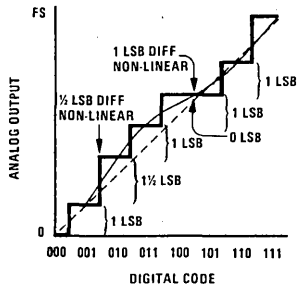


FIGURE 6. ±½ LSB Non-Linearity (Implies 1 LSB Possible Error), 1 LSB Differential Non-Linearity (Implies Monotonicity)

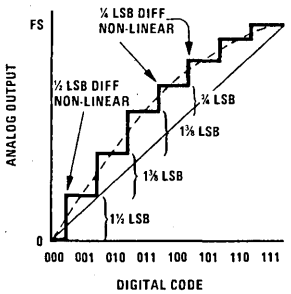


FIGURE 7. 1¼ LSB Non-Linear, ½ LSB Differential Non-Linearity

Linearity specs refer to either ADCs or to DACs, and do not include quantizing, gain, offset, or scale errors. Linearity errors are of prime importance along with differential linearity in either ADC or DAC specs, as all other errors (except quantizing, and temperature and long-term drifts) may be adjusted to zero. Linearity errors may be expressed in % FS or fractional LSB.

Differential Non-Linearity indicates the difference between actual analog voltage change and the ideal (1 LSB) voltage change at any code change of a DAC. For example, a DAC with a 1.5 LSB step at a code change would be said to exhibit ½ LSB differential non-linearity (see figures 6 and 7). Differential non-linearity may be expressed in fractional bits or in % FS.

Differential linearity specs are just as important as linearity specs because the apparent quality of a converter curve can be significantly affected by differential non-linearity even though the linearity spec is good. Figure 6 shows a curve with a ±½ LSB linearity and ±1 LSB differential non-linearity while figure 7 shows a curve with +1¼ LSB linearity and ±½ LSB differential non-linearity. In many user applications, the curve of figure 7 would be preferred over that of figure 6 because the curve is smoother. The differential non-linearity spec describes the smoothness of a curve; therefore it is of great importance to the user. A gross example of differential non-linearity is shown in figure 8 where the linearity spec is ±1 LSB and the differential linearity spec is ±2 LSB. The effect is to allow a transfer curve with grossly degraded resolution; the normal 8-step curve is reduced to 3 steps in figure 8. Similarly, a 16-step curve (4-bit converter) with only 2 LSB differential non-linearity could be reduced to 6 steps (a 2.6-bit converter?). The real message is, "Beware of the specs." Do not ignore or omit differential linearity characteristics on a converter unless the linearity spec is tight enough to guarantee the desired differential linearity. As this characteristic is impractical to measure on a production basis, it is rarely, if ever, specified, and linearity is the primary specified parameter. Differential non-linearity can always be as much as twice the non-linearity, but no more.

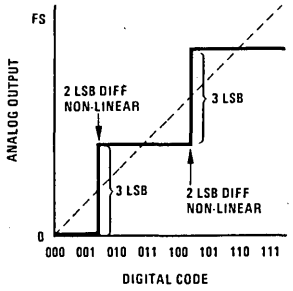


FIGURE 8. ±1 LSB Linear, ±2 LSB Differential Non-Linear

Monotonicity. A monotonic curve has no change in sign of the slope; thus all incremental elements of a monotonically increasing curve will have positive or zero, but never negative slope. The converse is true for decreasing curves. The transfer curve of a monotonic DAC will contain steps of only positive or zero height, and no negative steps. Thus a smooth line connecting all output voltage points will contain no peaks or dips. The transfer function of a monotonic ADC will provide no decreasing output code for increasing input voltage.

Figure 9 shows a non-monotonic DAC transfer curve. For the curve to be non-monotonic, the linearity error must exceed ±½ LSB no matter by how little. The greater the linearity error, the more significant the negative step might be. A non-monotonic curve may not be a special disadvantage in some systems; however, it is a disaster in closed-loop servo systems of any type (including a DAC-controlled ADC). A ±½ LSB maximum linearity spec on an n-bit converter guarantees monotonicity to n bits. A converter exhibiting more than ±½ LSB non-linearity may be monotonic, but is not necessarily monotonic. For example, a 12-bit DAC with ±½ bit linearity to 10 bits (not ±½ LSB) will be monotonic at 10 bits but may or may not be monotonic at 12 bits unless tested and guaranteed to be 12-bit monotonic.

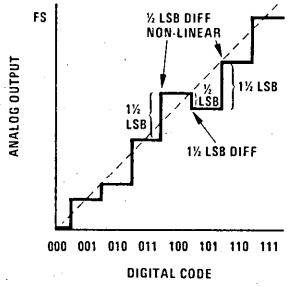
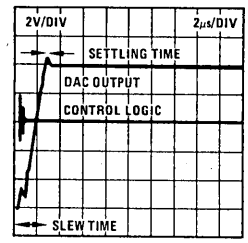
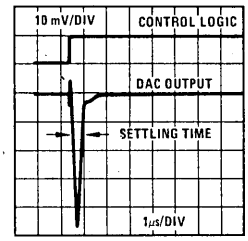


FIGURE 9. Non-Monotonic (Must be > ±½ LSB Non-Linear)



(a) Full-Scale Step



(b) 1 LSB Step

FIGURE 10. DAC Slew and Settling Time

Settling Time is the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ±½ LSB. (See also **Conversion Rate** below.) Settling time is often listed along with a slew rate specification; if so, it may not include slew time. If no slew rate spec is included, the settling time spec must be expected to include slew time. Settling time is usually summed with slew time to obtain total elapsed time for the output to settle to final value. Figure 10 delineates that part of the total elapsed time which is considered to be slew and that part which is settling time. It is apparent from this figure that the total time is greater for a major than for a minor code change due to amplifier slew limitations, but settling time may also be different depending upon amplifier overload recovery characteristics.

Slew Rate is an inherent limitation of the output amplifier in a DAC which limits the rate of change of output voltage after code transitions. Slew rate is usually anywhere from 0.2 to several hundred volts/μs. Delay in reaching final value of DAC output voltage is the sum of slew time and settling time as shown in figure 10.

Overshoot and Glitches occur whenever a code transition occurs in a DAC. There are two causes. The current output of a DAC contains switching glitches due to possible asynchronous switching of the bit currents (expected to be worst at half-scale transition when all bits are switched). These glitches are normally of extremely short duration but could be of ½ scale amplitude. The current switching glitches are generally somewhat attenuated at the voltage output of the DAC because the output amplifier is unable to slew at a very high rate; they are, however, partially coupled around the amplifier via the amplifier feedback network and seen at the output. The output amplifier introduces overshoot and some non-critically damped ringing which may be minimized but not entirely eliminated except at the expense of slew rate and settling time.

Temperature Coefficient of the various components of a DAC or ADC can produce or increase any of the several errors as the operating temperature varies. Zero scale offset error can change due to the TC of the amplifier and comparator input offset voltages and currents. Scale error can occur due to shifts in the reference, changes in ladder resistance or non-compensating RC product shifts in dual-slope ADCs, changes in beta or reference current in current switches, changes in amplifier bias current, or drift in amplifier gain-set resistors. Linearity and monotonicity of the DAC can be affected by differential temperature drifts of the ladder resistors and switches. Overshoot, settling time, and slew rate can be affected by temperature due to internal change in amplifier gain and bandwidth. In short, every specification except resolution and quantizing error can be affected by temperature changes.

Long-Term Drift, due mainly to resistor and semiconductor aging can affect all those characteristics which temperature change can affect. Characteristics most commonly affected are linearity, monotonicity, scale, and offset. Scale change due to reference aging is usually the most important change.

Supply Rejection relates to the ability of a DAC or ADC to maintain scale, offset, TC, slew rate, and linearity when the supply voltage is varied. The reference must, of course, remain constant unless considering a multiplying DAC. Most affected are current sources (affecting linearity and scale) and amplifiers or comparators (affecting offset and slew rate). Supply rejection is usually specified only as a % FS change at or near full scale at 25°C.

Conversion Rate is the speed at which an ADC or DAC can make repetitive data conversions. It is affected by propagation delay in counting circuits, ladder switches and comparators; ladder RC and amplifier settling times; amplifier and comparator slew rates; and integrating time of dual-slope converters. Conversion rate is specified as a number of conversions per second, or conversion time is specified as a number of microseconds to complete one conversion (including the effects of settling time). Sometimes, conversion rate is specified for less than full resolution, thus showing a misleading (high) rate.

Clock Rate is the minimum or maximum pulse rate at which ADC counters may be driven. There is a fixed relationship between the minimum conversion rate and the clock rate depending upon the converter accuracy and type. All factors which affect conversion rate of an ADC limit the clock rate.

Input Impedance of an ADC describes the load placed on the analog source.

Output Drive Capability describes the digital load driving capability of an ADC or the analog load driving capacity of a DAC; it is usually given as a current level or a voltage output into a given load.

CODES

Several types of DAC input or ADC output codes are in common use. Each has its advantages depending upon the system interfacing the converter. Most codes are binary in form; each is described and compared below.

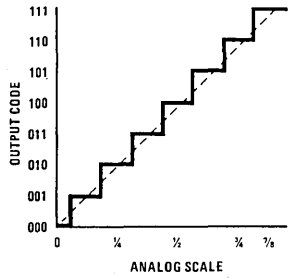
Natural Binary (or simply Binary) is the usual 2^n code with 2, 4, 8, 16, . . . , 2^n progression. An input or output high or "1" is considered a signal, whereas a "0" is considered an absence of signal. This is a positive true binary signal. Zero scale is then all "zeros" while full scale is all "ones."

Complementary Binary (or Inverted Binary) is the negative true binary system. It is identical to the binary code except that all binary bits are inverted. Thus, zero scale is all "ones" while full scale is all "zeros."

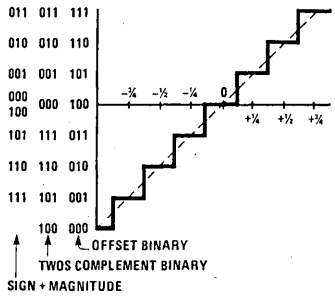
Binary Coded Decimal (BCD) is the representation of decimal numbers in binary form. It is useful in ADC systems intended to drive decimal displays. Its advantage over decimal is that only 4 lines are needed to represent 10 digits. The disadvantage of coding DACs or ADCs in BCD is that a full 4 bits could represent 16 digits while only 10 are represented in BCD. The full-scale resolution of a BCD coded system is less than that of a binary coded system. For example, a 12-bit BCD system has a resolution of only 1 part in 1000 compared to 1 part in 4096 for a binary system. This represents a loss in resolution of over 4:1.

Offset Binary is a natural binary code except that it is offset (usually ½ scale) in order to represent negative and positive values. Maximum negative scale is represented to be all "zeros" while maximum positive scale is represented as all "ones." Zero scale (actually center scale) is then represented as a leading "one" and all remaining "zeros." The comparison with binary is shown in figure 11.

Twos Complement Binary is an alternate and more widely used code to represent negative values. With this code, zero and positive values are represented as in natural binary while all negative values are represented in a twos complement form. That is, the twos complement of a number represents a negative value so that interface to a computer or microprocessor is simplified. The twos complement is formed by complementing each bit and then adding a 1; any overflow is neglected. The decimal number –8 is represented in twos complement as follows: start with binary code of decimal 8 (off scale for ± representation in 4 bits so not a valid code in the ± scale of 4 bits) which is 1000; complement it to 0111; add 0001 to get 1000. The comparison with offset binary is shown in figure 11. Note that the offset binary representation of the ± scale differs from the twos complement representation only in that the MSB is complemented. The conversion from offset binary to twos complement only requires that the MSB be inverted.



(a) Zero to + Full-Scale



(b) ± Full-Scale

FIGURE 11. ADC Codes

Sign Plus Magnitude coding contains polarity information in the MSB (MSB = 1 indicates a negative sign); all other bits represent magnitude only. This code is compared to offset binary and twos complement in figure 11. Note that one code is used up in providing a double code for zero. Sign plus magnitude code is used in certain instrument and audio systems; its advantage is that only one bit need be changed for small scale changes in the vicinity of zero, and plus and minus scales are symmetrical. A DVM might be an example of its use.

CONTROL

Each ADC must accept and/or provide digital control signals telling it and/or the external system what to do and when to do it. Control signals should be compatible with one or more types of logic in common use. Control signal timing must be such that the converter or connected system will accept the signals. Common control signals are listed below.

Start Conversion (SC) is a digital signal to an ADC which initiates a single conversion cycle. Typically, an SC signal must be present at the fall (or rise) of the clock waveform to initiate the cycle. A DAC needs no SC signal; however, such could be provided to gate digital inputs to a DAC.

End of Conversion (EOC) is a digital signal from an ADC which informs the external system that the digital output data is valid. Typically, an EOC output can be connected to an SC input to cause the ADC to operate in continuous conversion mode. In non-continuous conversion systems, the SC signal is a command from the system to the ADC. A DAC does not supply an EOC signal.

Clock signals are required or must be generated within an ADC to control counting or successive approximation registers. The clock controls the conversion speed within the limitations of the ADC. DACs do not require clock signals.

CONCLUSION

Once the user has a working knowledge of DAC or ADC characteristics and specifications, he should be able to select a converter to suit a specific system need. The likelihood of overspecification, and therefore an unnecessarily high cost, is likewise reduced. The user will also be aware that specific parameters, test conditions, test circuits, and even definitions may vary from manufacturer to manufacturer. For practical production reasons, parameters may not be tested in the same manner for all converter types, even those supplied by the same manufacturer. Using information in this note, the user should, however, be able to sort out and understand those specifications (from any manufacturer) pertinent to his needs.

Data Acquisition System Interface to Computers

National Semiconductor
Application Note 159
Jim Sherwin

INTRODUCTION

The need of interfacing several analog data channels to computers has not escaped the attention of the data system firms. There are presently available a number of data acquisition units (DAUs) which will directly interface 8-64 analog data channels to one or more types of computers or microcomputers, and more appear on the market almost monthly. Some of these DAUs are even constructed to plug into the mainframe of the computer for which they are designed. Nearly all of these commercially available DAUs are of more or less conventional design, operating in either a random channel address or sequential address mode. Figure 1 shows a typical functional diagram of such a random channel address DAU. Its advantages are simplicity, straightforward design, and comparatively low cost (depending upon performance and special features). In operation, the computer addresses a specific channel, the analog multiplexer (MUX) is set to the desired channel, a sample and hold (S&H) circuit acquires and holds the analog signal, an analog-to-digital converter (ADC) digitizes the signal, a ready signal is returned to the computer, and the data is presented to the data bus via TRI-STATE® bus drivers. If the data is 12-bit and the data bus is 8-bit, the data word must be broken into two bytes and addressed separately. The prime disadvantage of these DAU designs is that the computer must either enter a wait mode while data is readied or it can proceed with its assigned task, watch for a data-ready flag signal, and return for the data.

From the standpoint of microprocessor system design, it is clearly desirable to access input data as if it were main memory. It is further desirable that input data access time be equivalent to that of main memory so that the processor need not enter a wait mode while data is readied for input. One attractive method of accomplishing this is to use one A/D converter (of a type containing TRI-STATE output data latches) on each input data channel. Henceforth I shall refer to this as parallel conversion. Figure 2 shows such a system containing only an address decoder and multiple A/D converters with all outputs wired in parallel onto the data bus. Note the absence of S&H modules.

The advantages of this DAU system are the immediate data access and its simplicity. However, one's first thought on considering a parallel-conversion system might be that the cost of ADCs would exclude their consideration on a one-per-channel basis. But, although this may have been true in the past, currently available monolithic and hybrid ADCs are priced such that this system concept is entirely feasible. Furthermore, the converter price trend is definitely downward as more monolithic units are released, so the economic feasibility can only improve in the next few years, thus extending the application to an ever larger segment of the market. The ideal converter for use in the system of Figure 1 includes converter, comparator, and buffered TRI-STATE output data latches in one package. The unit would

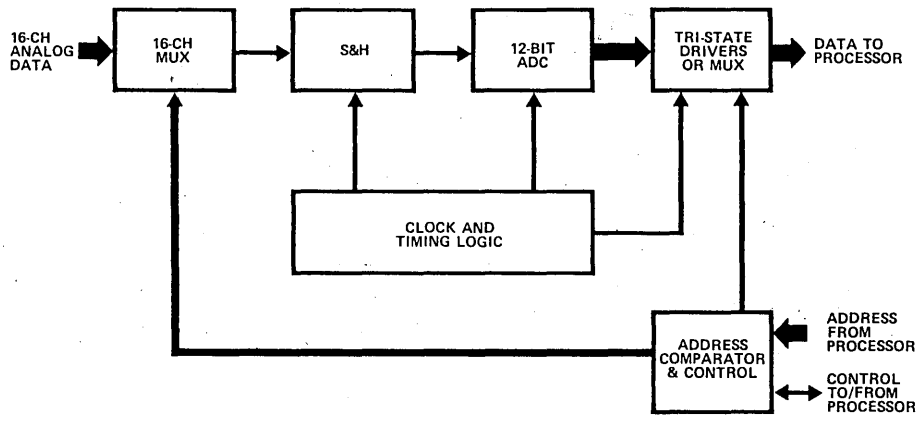


FIGURE 1. Random-Addressed Multiplexed DAU

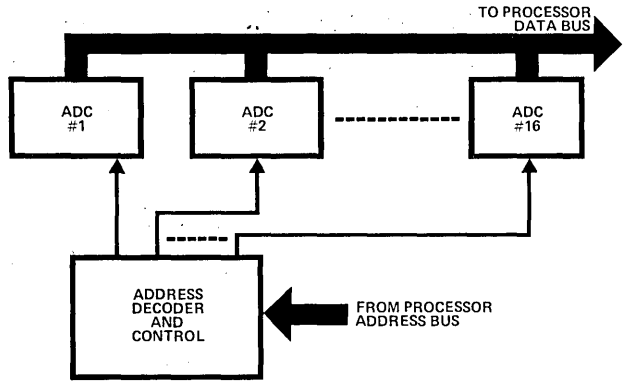


FIGURE 2. Parallel Data Conversion Concept

operate in the continuous convert mode with the last data remaining in the output latches until the next completed conversion shifts new data into the latches. Valid latest data is thus always available for readout on the data bus except for a brief period when the data is being updated. In contrast, a converter without buffered output latches does not hold data after a start-conversion signal and so must be operated in the command mode with a wait for data after the converter is started.

In spite of the advantages of the parallel-conversion DAU, there is (at present ADC prices) a more cost-effective way of providing the same immediate memory-access mode of operation, particularly for 12-bit data. Figure 3 shows a multiplexed DAU with self-contained memory which will interface to computer systems in the memory-access mode without a wait period.

The total package count of this system is lower than that of the parallel-conversion DAU, the cost/channel is lower, and the required space and power is lower. A disadvantage is that the accessed data may be as much as 800μs old, compared to a possible 1-4μs with parallel conversion. The key to the success of the system is the dedicated on-card 16x12 RAM. Neither does the system require a special ADC design with buffered output data latches. Main memory could, of course, be used instead, but then some machine time would be utilized as memory write time. This way, the latest data is always ready and waiting in the DAU (peripheral) memory, and software is considerably simplified.

Before exploring any of the three systems in more detail, it is worth considering the system limitations, the economics, and the probable market segment which could be served by the three types of DAU described.

The required data bandwidth has obvious strong effects on system cost and realization. The bandwidth of a sampled data system is limited by Shannon's sampling criterion and other practical considerations to, say,

$$f_{max} = \frac{1}{5\, t_{conversion}}$$

which is 4kHz for a 50μs conversion cycle time. However, when no S&H module is used ahead of the ADC, as in a parallel-conversion DAU, conversion must take place within the time it takes the input signal to change by ±½ LSB or 1 part in 2^{n+1}. For sine waves, the maximum rate of change is determined as follows:

$$\frac{\Delta v}{\Delta t} = \omega v_{pk},$$

but

$$v_{max} = \frac{2\, v_{pk}}{2^{n+1}}$$

therefore

$$\frac{2\, v_{pk}}{2^{n+1}\, \Delta t} = 2\pi f_{max}\, v_{pk}$$

and

$$f_{max} = \frac{2^{-(n+1)}}{\pi\, t_{conv}}.$$

For the same 50μs conversion time and an 8-bit accuracy requirement of ±½ LSB, f_{max} is 12Hz. Figure 4 compares data bandwidth of 8- to 14-bit systems with and without S&H. The economic effect of adding an S&H module ahead of each ADC in a parallel-conversion DAU is obvious (possibly doubling the cost per channel of an 8-bit system) as is the cost of significantly increasing conversion speed except by use of tracking converters (advantageous only in parallel-conversion systems).

The conventional random-addressed DAU can serve any part of the data acquisition market where the task of the computer is light enough that the system can afford to enter a wait mode at data request. This wait period can be as low as 10-20μs if sufficient money is available for fast S&H circuits and fast ADCs, as high-speed components are traditionally quite expensive. Lower cost systems may require a wait period of 100-200μs before data is available. At the expense of more complex software, the computer could remain busy during the period of data preparation, and would return for the data when it was made ready. The data bandwidth may be deter-

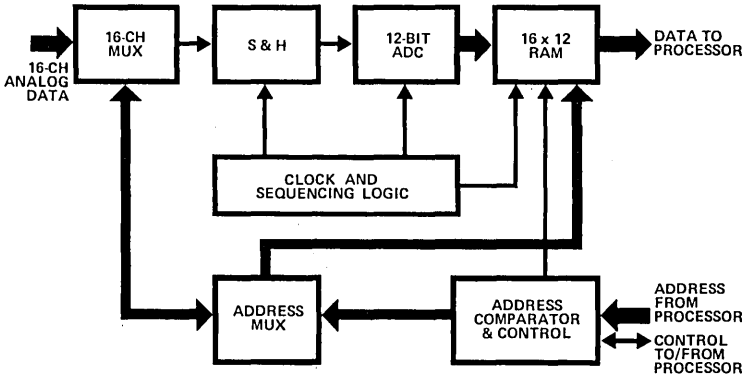


FIGURE 3. Multiplexed Immediate-Data-Access DAU

mined from Figure 4. Sixteen channels of 10Hz data could be available if each channel were sampled once every 20ms. This is a data throughput rate of 16ch x 1/20ms = 800Hz. The higher cost DAUs of this type have capability of 50-100kHz throughput rates. However, if the computer waits while data is made ready, it will be completely occupied with gathering data when the maximum throughput rate is utilized.

The parallel conversion DAU without S&H circuits is destined to operate on low-bandwidth data as indicated in Figure 4. To be economically feasible the ADCs must be of low cost. This means an 8- or 10-bit successive approximation register (SAR) or a 12-bit integrating monolithic ADC must be used. New ADC designs using tracking counters could increase data bandwidth capability over that possible with SAR counters. For purely economic reasons, then, use of parallel-conversion DAU systems will be limited to low bandwidth data – 10-30Hz on 8-bit, 2-5Hz on 10-bit, and less than 1Hz on 12-bit systems. These bandwidth figures for 8- to 10-bit systems could be considerably improved, say by 8-10 times, if tracking converters were used in place of SAR converters. This definitely suggests that there is a need for low-cost tracking converters. Note that S&H circuits are not needed in the parallel-conversion systems.

The multiplexed DAU with memory can serve any segment of the data market. It is limited in bandwidth

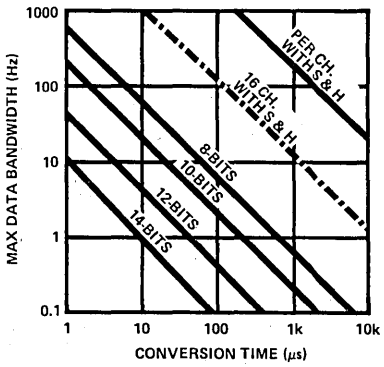


FIGURE 4. Data Bandwidth vs. Conversion Time

or data throughput rate principally by the S&H and ADC operating times, its cost per channel is only slightly higher than that of the conventional DAU, and it allows the computer to operate in the most efficient manner.

A comparison of system costs must include the following for a 16-channel system.

Parallel Conversion	Random Addressed Multiplexed	Multiplexed with Memory
16 A/D Converters	1 A/D Converter	1 A/D Converter
16 Anti-Aliasing Filters	1 S&H Module	1 S&H Module
Control Circuits	1 16-Channel Multiplexer	1 16-Channel Multiplexer
Additional power for extra converters	16 Anti-Aliasing Filters	16 Anti-Aliasing Filters
Lower data bandwidth	More complex control circuits	1 16x12 RAM
Simple software	Longer data access time	More complex control circuits
	Possibly more complex software	High-speed data access
		Simple Software

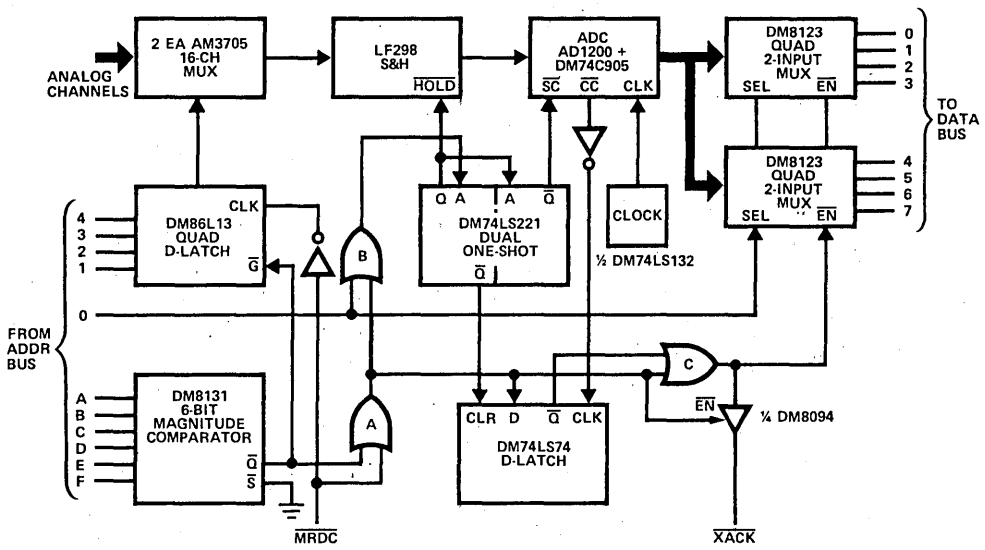


FIGURE 5. Conventional DAU for 8080

The future trends in DAU designs will include an increasing number of parallel-conversion DAUs, especially as cost reductions appear on monolithic ADCs with TRI-STATE output circuits (or latches). We should also start to see some tracking converters in the low-cost monolithics with TRI-STATE output data latches. Expect to see multiplexed DAUs with memory appearing in the near future. Its simplicity from a circuit and software standpoint cannot long go unnoticed.

RANDOM ADDRESSED DATA ACQUISITION UNIT

A conventional, random-addressed, 16-channel, 12-bit DAU is diagrammed in Figure 5. The analog section contains a 16-channel analog multiplexer, a sample-and-hold block, and a 12-bit ADC. A more complete system might contain a differential multiplexer and/or a differential (or instrumentation) amplifier preceding the S&H block. The data output circuits are arranged to interface an 8-bit data bus as found on an 8080 or 6800 microcomputer (μC). Since the data word is 12 bits, the μC must accept it in two 8-bit bytes. Normally the μC would address the DAU with two consecutive address locations corresponding to a 0 and a 1 at the address LSB to load the two bytes of data. The DM8123 multiplexers are ideally suited to this use. They have TRI-STATE output circuits, and the channel-select input may be directly driven from the address LSB. If a 16-bit address bus were being interfaced, such as in the PACE μC, the output multiplexers would be replaced with DM8097 or equivalent TRI-STATE output buffers (see Figure 11). In both instances, low-power versions of these parts, the DM81L23 and DM80L97, could be used to drive a lightly loaded data bus.

The address decoding is accomplished with a DM8161 6-bit magnitude comparator looking at the six most significant address bits. These 6 bits are compared with an address code hard wired into a DIP header which can be different for each DAU card in a system. Comparing only 6 address bits allows a possible 64 cards in a single system and uses up to 64 pages of memory position. If this is not satisfactory, two address comparators ORed together (DM8163) could select from 12 bits of address. The magnitude comparator(s) plus the four address lines to the 16-ch MUX make up the complete address decoding. The output of the magnitude comparator(s) indicates when this DAU has been addressed, and the four address lines to the MUX select the 1-of-16 channels of this DAU.

This circuit is designed to interface the 8080 μC. Thus, a memory read command $\overline{\text{MRDC}}$ must be received, and an acknowledgement $\overline{\text{XACK}}$ must be issued to indicate when data is ready. Operation is as follows: A valid address on address lines A-F causes comparator output $\overline{Q}$ to go low. This gates the inputs of the quad D latch to accept the 1-of-16 address word from address lines 1-4. At the occurrence of $\overline{\text{MRDC}}$ the address is clocked into the quad D latch and presented to the 16-ch MUX which selects the addressed channel. When $\overline{Q}$ and $\overline{\text{MRDC}}$ are both low, the output of OR gate A goes low, which enables the XACK signal buffer. If the address LSB is 0 (byte 1 of a 2-byte data request), OR gate B output goes low to trigger a one-shot.

The one-shot circuits are a simple means of timing the sample period and the converter start commands. There are other methods (see Figure 15) of accomplishing this timing without the hazards associated with one-shot circuits; however, the simplicity of this scheme lends itself to easy understanding of the timing required. The first one-shot generates a sample pulse of 5-30μs as required for the S&H to acquire and settle to 0.01% of value. Its $\overline{Q}$ output presets the single D latch ($\overline{Q}$ = 1). The trailing edge of this pulse returns the S&H to HOLD condition and triggers the next one-shot to generate a start conversion command of about 3μs. When the ADC completes conversion, its $\overline{CC}$ output goes low, thus clocking a 0 into the single D latch to reset its Q output low. Both inputs to OR gate C now being low will enable the output MUX and return a low on the $\overline{XACK}$

line indicating to the μC that data is ready. Address LSB = 0 selects the 8 LSB of the data word for presentation to the data bus. A subsequent address with LSB = 1 selects the 8 MSB of the data word, but will not trigger the one-shot or preset the D latch because the output of OR gate B will remain high. Since the output of OR gates A and C will be low, $\overline{XACK}$ is returned and the output MUXs are enabled to present byte 2 of the data word on the data bus. When $\overline{MRDC}$ returns high, the output circuits are disabled. If the 6-bit comparator does not see a valid address, no action is taken by the DAU.

This represents the simplest possible DAU for interfacing to computers. The interface to the 8080 is one of the simplest. Only minor modifications are required to interface, for example, the 6800 or PACE μCs (see Figures 9 and 11). The only timing anomaly in the logic system shown is that when the $\overline{XACK}$ buffer is enabled there will be a 10-40ns pulse of 0 output. The computer, however, does not act on an XACK signal at this time and so will enter a wait mode until $\overline{XACK}$ is returned later on.

The analog signal section has purposely been omitted from this discussion of interfacing to processors because its details will depend upon analog signal levels, the possible requirement for differential channels, the possible need of an instrumentation amplifier following the multiplexer, and S&H timing requirements. The analog section of the DAU may be made up of various components, depending upon the required performance and operating conditions. A pair of 8-channel multiplexers will give the flexibility of connecting as differential 8-channel or as single ended 16-channel whereas a single 16-channel MUX with space and wiring on the board for another 16-channel MUX would allow for either 32 channels or 16 differential channels. A pair of AM3705s could be used for lowest cost where analog signals are no greater than ±5V. The S&H circuit could be monolithic LF198, hybrid LH0023, LH0043 or LH0053, made up of individual discrete and integrated circuits, or it could be any of several available modules.

The ADC used in this system may be of a conventional design with speed and accuracy being the only important technical considerations. No special TRI-STATE output or output data latches are needed as the data is latched in the register until a new start conversion (SC) command is given. The ADC could be made up of an AD1200 ADC building block plus DM2504 or MM74C905 successive-approximation register, it could be an AD1210 plus LH0071 reference and appropriate MOS-TTL and TTL-MOS buffers, or it could be any one of a number of other ADCs on the market.

Total power is about 2.8 watts and cost is about $9.50 per channel for components as indicated in Table 1. Note that output drivers are standard TTL circuits whereas low power TTL may be used for lower power dissipation where a lightly loaded data bus is to be driven.

PARALLEL-CONVERSION DATA ACQUISITION UNIT

Parallel data conversion is likely the simplest possible μC data system concept which will effect immediate access to latest input data as if it were main memory. It may be treated as main memory by the processor and is only slightly more complex than the simplified system of Figure 2. The individual ADCs in Figure 2 include TRI-STATE output for direct wire ORing on the data bus. However, to make each capable of driving a heavily loaded system bus would require significant and unnecessary power dissipation in each ADC. Accordingly, except in minimally loaded systems, a separate set of TRI-STATE TTL output data buffers would be added to Figure 2. Small differences in the address decoder and control circuits will exist, depending upon which μC system will be used.

The control circuits are exceptionally simple, being required primarily to accept the memory read command and to return a memory ready signal. The most complex part of the control circuits is that required of μC systems which accept data in two 8-bit bytes rather than in one 16-bit byte, yet even this added complexity is minimal.

Table 1. Conventional DAU Power & Cost

		P_D (mW)	$ (100s)
1 –	16-Channel MUX	300	19.55
1 –	S&H	500	74.50
1 –	ADC	600	40.00
2 – DM8123	Quad 2-Input MUX	800	2.56
1 – DM8161	Hex Comparator	250	2.56
1 – DM86L13	Quad D-Latch	30	1.28
1 – DM74LS221	Dual One-Shot	30	3.00
1 – DM74LS132	Quad Schmidt NAND	60	2.00
1 – DM7432	Quad OR Gate	100	.49
1 – DM74LS74	Dual D F-F	20	3.00
1 – DM8094	TRI-STATE 4 x Buffer	144	.71
		2834	150.05
			$9.38/Channel

Table 2. Microprocessor System Characteristics

	8080	PACE	6800	SC/MP
Address Word Length	16-bit	16-bit data/address bus	16-bit	12- or 16-bit
Data Word Length	8-bit		8-bit	8-bit
Address & Data Polarity	All chips are 1 = true; however, if Intel system bus drivers and receivers are used, 8080 system data and address bits are 0 = true.			
Address Strobe	None	NADS = 0 to set memory address latches	VMA = 1 (concurrent with)	NADS = 0
Memory Read Strobe	MRDC = 0 to read data	IDS = 1 to input data	R/W = 1 to read data	NRDS = 0 to read data
Maximum Clock Rate	2MHz	2MHz	1MHz	1MHz

Since μC systems differ somewhat from one another, it is worth our effort to look at the hardware and software details and the system timing requirements of several of them when considering a DAU interface. From this consideration we can establish the desired function and characteristics of the ADCs, DACs, address decoders, control components, and μC interface signals. The following exercises include interfacing parallel conversion DAUs of 8- and 12 bits to the Intel 8080, the National PACE, and the Motorola 6800 microcomputer systems. Interface to other systems such as National's SC/MP will be similar. All request, control, and answer signals are considered along with the required signal polarities and timing relationships. Table 2 summarizes the important characteristics of these three systems.

8080 Interface

The 16-channel, 8-bit parallel-conversion DAU shown in Figure 6 will interface with an 8080 μC system without a wait period in the memory-read cycle. This system can be built with existing components for about $10 per channel. It is a minimal system, capable of driving only a lightly loaded data bus, as the MM5357 ADCs can drive but a single TTL load. When heavier loads must be driven, two quad TRI-STATE output buffers will be needed. The address decoding uses a 4-line to 16-line decoder which selects the addressed channel from the four least significant (LSB) of address bits. A 6-bit address comparator compares the six most significant (MSB) address bits with a code hard-wired into the code-select-header. The comparator output gates the 4:16 decoder only if the proper memory page (1 of 64) is addressed. The comparator output, gated by the memory read command $\overline{\text{MRDC}}$, inhibits the clock to prevent data change in the output latches during the data access period. Concurrence of the correct address and $\overline{\text{MRDC}}$ also returns a data-ready acknowledgement to the μC via the TRI-STATE output of a buffer. No other logic is required; however, inverters are necessary in the ADC enable lines due to a sense mismatch in the 4:16 decoder output and the ADC enable inputs. The system is truly as uncomplicated as indicated in Figure 2.

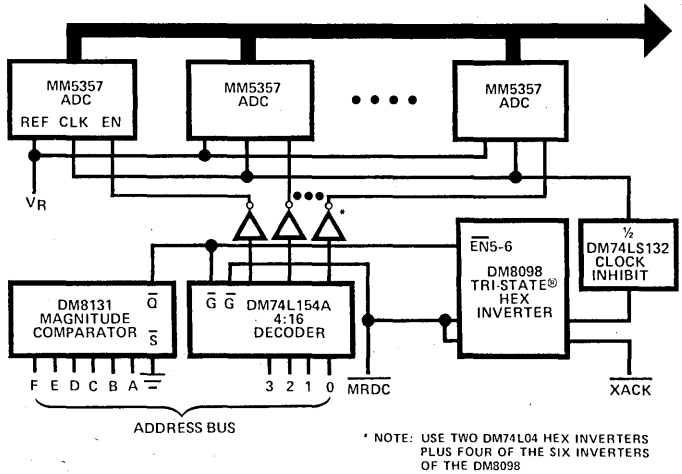


FIGURE 6. 16-Ch, 8-Bit Parallel-Conversion DAU for 8080

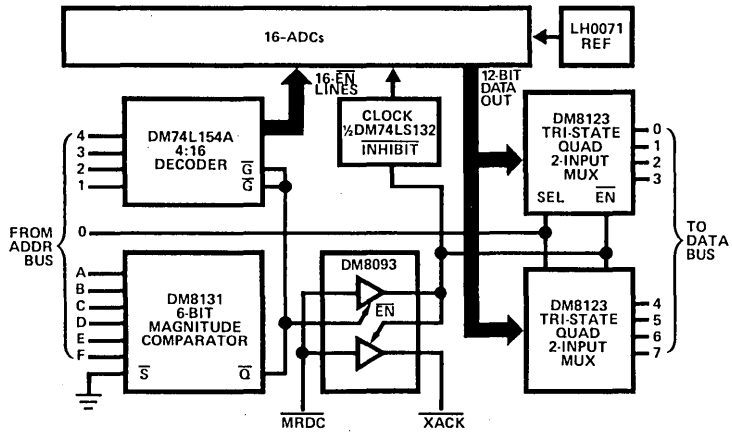


FIGURE 7. 16-Ch, 12-Bit Parallel-Conversion DAU for 8080

As 12-bit data is likely of greater interest in the market, the remainder of the discussion will consider the logic necessary to handle 12-bit data. Accordingly, Figure 7 shows a 16-channel, 12-bit parallel-conversion DAU for the 8080. No part number designation appears on the ADCs because they are hypothectical units possessing the characteristics considered desirable in this application. The converters contain the DAC switches, ladder network, comparator, up/down counter (for tracking conversion), control logic, and TRI-STATE buffered outputs. They operate continuously with the output data buffer updated at the end of each conversion. Such a converter containing CMOS logic could settle in less than 1-4μs (after an initial but longer acquisition period) without being costly to construct, and would thus provide 12-bit accuracy to ±½ LSB at a data bandwidth of 10-20Hz. A single external buffered reference could suffice for all converter channels. An external gated clock could drive all converters. Address decoding is the same as outlined for the 8-bit system. The LSB address bit is used to select byte 1 or byte 2 of the 12-bit output data word by means of the two DM8123 quad, TRI-STATE, 2-input multiplexers. Address bits 1-4 are decoded into 1-of-16 select bits to enable the TRI-STATE output of the selected ADC. Since the 1-of-16 output select of the DM75L154A decoder is 0 true, it is desirable that the ADC enable input be 0 true. Otherwise, 16 inverters would be required. The control timing may be considered in reference to the 8080 timing requirements shown in Figure 8.

The DM8131 address comparator provides an output to gate the 4:16 decoder and to enable the DM8093 quad TRI-STATE line driver. This occurs (+30ns) only if the address is valid for this data card. If the address is valid, the 4:16 decoder accepts the address and the DM8093 is set to accept the MRDC command at inputs 5 and 6 (+250ns). The decoder output to the ADC enable lines is available (+180ns), and valid data is available from the selected ADC (+330ns). As the data card must return a data ready signal (+440ns) to prevent extending the memory access cycle, the DM8093 transmits the $\overline{\text{MRDC}}$

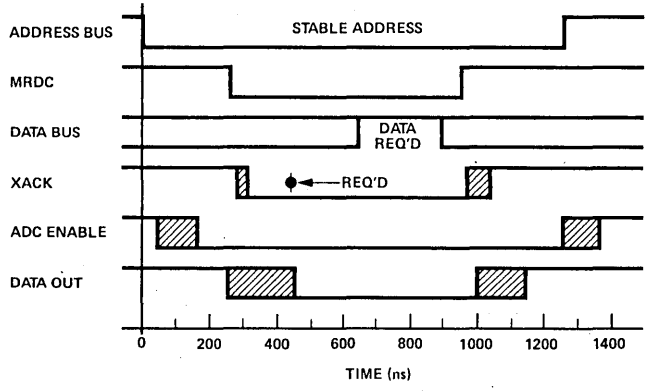


FIGURE 8. Timing and Control for 8080

back out to the μC on the XACK line (+300ns) in advance of the time required. A 0 is placed on the XACK line for the duration of the MRDC command. The MRDC signal also enables the output multiplexer enable lines (+300ns) via the DM8093. This signal also interrupts the clock drive to the ADCs to prevent a change in data output during the remainder of the memory read cycle. A desirable built-in design feature of the ADC for this application might be a clock inhibit or data transfer inhibit operating from the $\overline{EN}$ input. Valid data is present on the data bus (+460ns) at least 200ns before it is required. Valid data remains stable until the end of the MRDC command when XACK and data output lines return to their normal high-impedance states.

Data is placed on the data bus in two 8-bit bytes as controlled by the LSB address code. A 0 selects the 8 LSB data, and a 1 selects the MSB data. Two consecutive memory addresses will then read the entire data word in two bytes. As there are only 12 data bits, zeros are placed on the remaining data lines. For 2s complement binary data coding of ± input analog signals, the 12th bit would be inverted and extended to the remaining data lines so that signals would appear as valid data to the microprocessor.

Total address decode, control, clock, and output drive logic circuitry is contained in six DIP circuits (only one of 24 pins). To this must be added a code-select header, a reference, and 16 converters. Total power required is 4.2 watts for 16 channels of 12-bit data from ±5V analog signals of 10Hz bandwidth (see Table 3). Low Power TTL output drive capability would reduce power drain by 370mW. Total cost of parts (assuming a future price of $25/ADC) would run to about $26 per channel (see Table 4).

Table 3. Power Required, 16-Channel, 12-Bit

		P_D (mW)		
		8080	6800	PACE
16 –	ADC		3200	
1 – LH0071	Reference		45	
1 – DM74LS132	4 x 2-Input NAND Schmidt		60	
1 – DM74L154A	4:16 Decoder		24	
1 – DM8131	6-Bit Comparator		250	
1 – DM8093	4 x Buffer	170		
or 1 – DM8099	6 x NAND Buffer		175	
or 3 – DM8097	6 x Buffer			975
2 – DM8123	4 x 2-Input MUX	400	400	
or 1 – DM86L13	4 x D-Latch			30
		4199	4154	4584

Table 4. Cost of Components, 16-Channel, 12-Bit

		$ (100s)		
		8080	6800	PACE
16 –	ADC		400.00	
1 – LH0071	Reference		5.00	
1 – DM74LS132	4 x 2-Input NAND Schmidt		2.00	
1 – DM74L154A	4:16 Decoder		2.46	
1 – DM8131	6-Bit Comparator		2.56	
1 – DM8098	6 x Inverter	1.65		
or 1 – DM8099	6 x NAND Buffer		1.70	
or 3 – DM8097	6 x Buffer			5.55
2 – DM8123	4 x 2-Input MUX	2.56	2.56	
or 1 – DM86L13	4 x D-Latch			1.28
		416.23	416.28	418.85
			≈ $26/Channel	

6800 Interface

For other μC systems, the logic will change slightly. Figure 9 shows the logic section of the DAU of Figure 7 modified as necessary to interface with the 6800 μC. The 6800 timing and control signals are shown in Figure 10. With the 6800, the address information, the valid memory address VMA signal, and the read/write W/R signal all come up approximately simultaneously and remain for about one clock period of 1μs (min.). The data need not appear on the data bus until 100ns thereafter. The valid address decoding is accomplished by ANDing the VMA and R/W signals together in a TRI-STATE 2-input AND gate. When enabled by the comparator output, this gate returns a READY signal to the μC and enables the output multiplexers. The appropriate data byte is selected by the LSB address bit as with the 8080 system. The necessary 10ns data hold time is provided by the ADC and output multiplexer disable delays. The remainder of the DAU is identical to that of Figure 7. Cost and power required are also similar to those of the 8080 system interface.

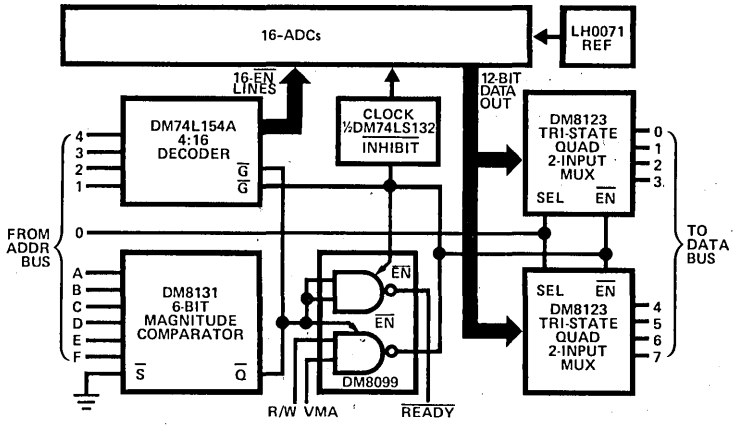


FIGURE 9. 16-Ch, 12-Bit Parallel-Conversion DAU for 6800

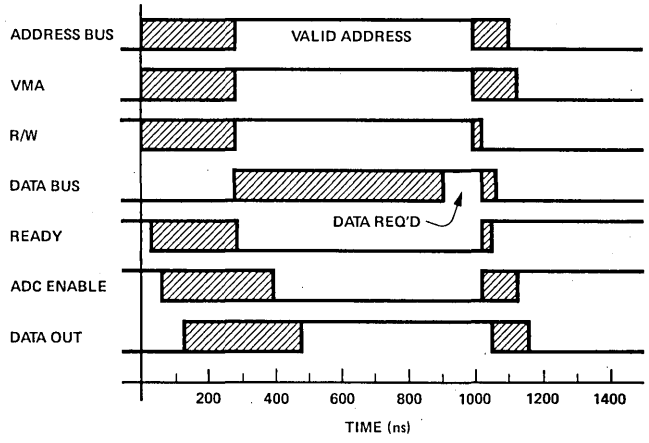


FIGURE 10. Timing and Control for 6800

PACE Interface

Figure 11 shows the logic section of the DAU of Figure 7 modified to interface with a PACE μC. The PACE timing is shown in Figure 12. Since the PACE μC has but a single address/data bus, address latches are required for address decoding. The DM8131 address comparator contains output latches, but the DM74L154A 4:16 decoder does not, so a quad latch is inserted ahead of the 4:16 decoder. The latches all set on the rising edge of the NADS signal provided by PACE during the time that address information is on the bus, and drop out on the next NADS signal. Comparator output applied to gate the 4:16 decoder provides an enable ADC signal lasting until the falling edge of the next NADS pulse. The IDS signal ANDed with the comparator output enables the TRI-STATE output buffers and inhibits the clock. An additional MSB inverter would be needed for ± analog signals in order to provide the 2s complement code. Total address decode, control, clock, and output drive circuitry is contained in seven DIP packages, one more than required for the 8080 system interface. Total power and cost are comparable to those given for the 8080 system interface.

ADC CHARACTERISTICS

The ADC for use on a parallel-conversion DAU must contain TRI-STATE output data latches. Otherwise it may be conventional. The MM5357 was designed for direct connection to a data bus, therefore it contains the necessary output latches. At this writing there are other ADCs with the TRI-STATE output latches appearing on the market, and more can be expected. The MM5357 is nearly ideal for use in an 8-bit parallel-conversion DAU. It would be even more suitable to this use if it were a tracking converter, and the polarity of its enable input and of its data output were of opposite polarity. The data polarity is of lesser importance as the bus drivers probably needed may as well be inverting as non-inverting except for common usage. The enable polarity should match the decoder output to obviate the need for 16 inverters (3 logic packages, though of little cost). See the later discussion of ADC hardware for additional thoughts on this subject.

This parallel-conversion data system has data bandwidth limited to about 10Hz for 8-bit SAR converters, but may be increased to 150-300Hz with 8-bit tracking

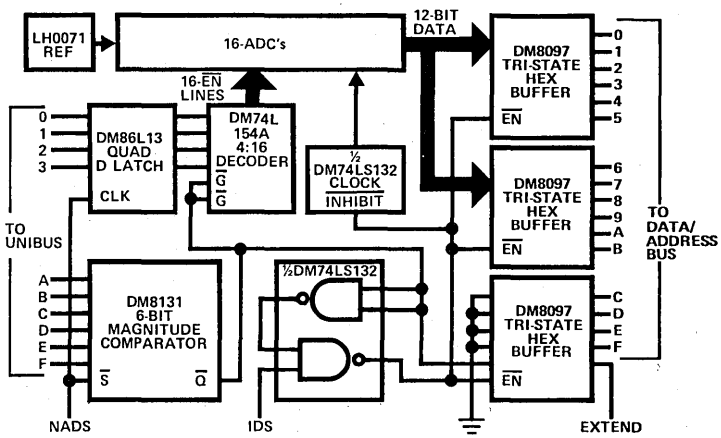


FIGURE 11. 16-Ch, 12-Bit Parallel-Conversion DAU for PACE

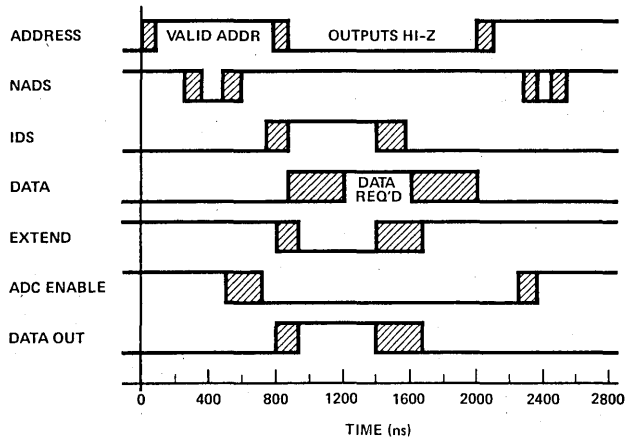


FIGURE 12. Timing and Control for PACE

converters. 12-bit data bandwidth will be 1/16 that of the 8-bit systems. On the other hand, no S&H module is required. Data rates could be considerably increased if S&H modules were added to each channel; however, costs per channel would more than double. For use with S&H modules, SAR logic converters would be faster than tracking types, allowing data bandwidths of over 600Hz/channel for 12-bit data.

MULTIPLEXED DATA ACQUISITION UNIT WITH MEMORY

A multiplexed data acquisition system containing memory is probably the most cost-effective way of providing an immediate data-access interface to processors. The processor may address the peripheral data-acquisition unit to obtain immediate data without entering a wait mode, just as if it were accessing main memory. Latest valid data is always present within the DAU memory which is updated at a rate determined by the channel multiplexer rate and ADC conversion speed. There is no need to write subroutines into processor software or firmware to address and request data from the peripheral, resume its assigned processing task while watching for a flag set by the peripheral indicating that data is ready, and returning to accept data from the peripheral.

The multiplexed DAU with memory shown in Figure 3 takes care of routinely updating its memory by sequentially sampling each data channel, digitizing the channel signals, and writing data into its self-contained memory. When the DAU is interrogated, the sequential process is momentarily interrupted, the RAMs are addressed by the processor, and data is read out to the data bus. The memory can be three each DM8599 16x4-bit RAMs. These have TRI-STATE outputs, so can connect directly to the data bus. Note that the RAM inverts the data bits from the ADC. The RAMs are available in low-power TTL to drive a lightly loaded data bus, or they are available in Schottky versions for driving higher speed systems. In fact, almost the entire logic system could be realized in Schottky circuits, which should allow interfacing even the new fast bipolar μCs without a wait cycle.

The MUX sequencing circuits are shown in Figure 13. When the μC is not accessing memory on the DAU, the 16 data channels are scanned in continuous sequence.

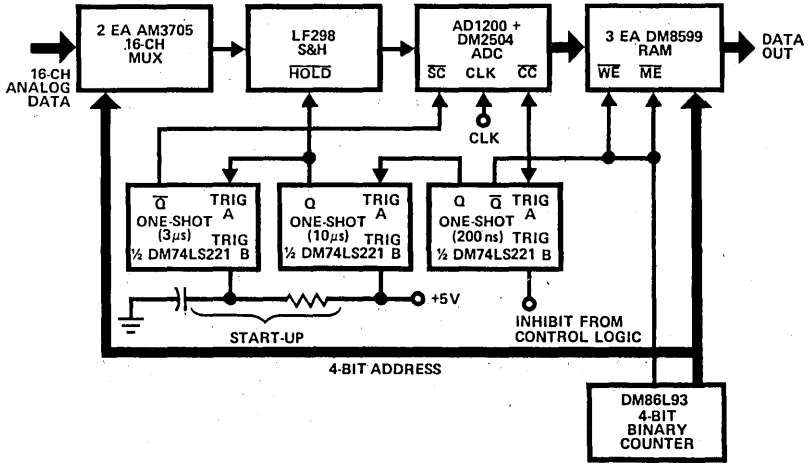


FIGURE 13. Sequencing Logic with OS

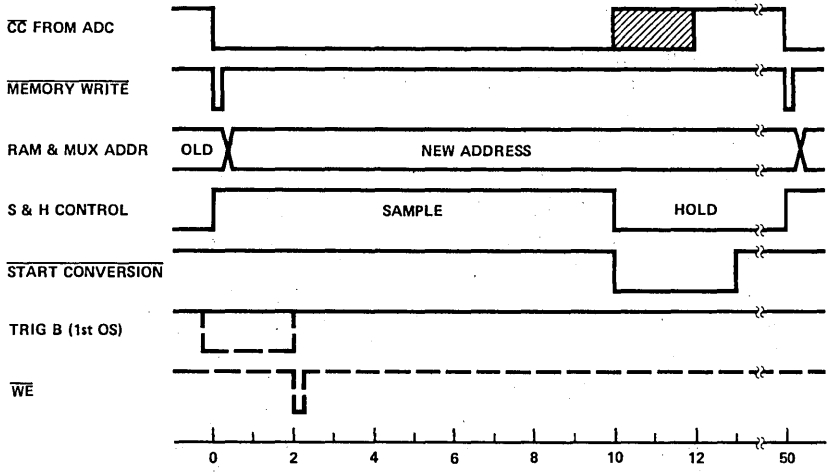


FIGURE 14. Timing for One-Shot Sequencing

Data on each channel is sampled and held in the S&H module while the ADC converts the analog data to digital. At the completion of conversion, the digital output of the ADC is written into the RAMs before the multiplexer selects the next channel. The timing and sequencing of channels is accomplished with a 4-bit binary (÷ 16) counter and three one-shot pulse generators. Where one-shots are undesirable, an alternate approach using shift register timing could provide the same function. A valid address output from the address comparator switches the RAM address input from the ÷16 counter to the address bus input, thereby addressing the RAM to the desired channel for data readout. If the data conversion sequence is in the memory write condition, the gate applied to WE prevents switching the MUX to the address bus or returning an XACK signal until the memory has been loaded. Thereupon, the sequence is interrupted as outlined above. The interruption of the sequence lasts for about 1300ns (8080 system) while the address is valid.

The sequential data conversion cycle is shown in the timing signals of Figure 14. The conversion-complete $\overline{CC}$ output of the ADC triggers a one-shot to generate a 200ns memory write pulse. The trailing edge of this pulse advances the address ÷ 16 counter to the next channel and triggers a second one-shot to produce a 10μs sample period. At the completion of the sample period, the S&H goes into hold mode and a third one-shot generates a 3μs start conversion $\overline{SC}$ pulse. When the DAU is in the command read mode, a 0 appears at B trigger input to the first one-shot. If a $\overline{CC}$ signal occurs during the time the 0 is present on the B input, the one-shot will not be triggered until the B input returns to a 1.

An alternate sequencing circuit without one-shot circuits is shown in Figure 15 with timing relationships in Figure 16. It makes use of a shift register and exclusive-OR gates to generate the gates needed to write into memory, sample and hold, and start conversion. The ADC clock is generated at twice the desired clock frequency and divided by 2 in a D flip-flop. In this manner, the minimum gate width is 1/4 of the ADC clock period (620ns in this example). The $\overline{CC}$ signal is clocked into a D flip-flop with a delay of 620ns. The delayed output clears the shift register (SR) and is clocked into the SR after an additional 620ns delay. An exclusive-OR of the SR input and Q1 output generates a 620ns gate to write data into the RAMs. The trailing edge of this $\overline{WE}$ gate clocks the ÷ 16 counter to advance the MUX and RAM address to the next channel. Exclusive-ORing of SR Q1 and Q7 produces an 8.75μs sample gate. (If the acquisition and settling time of the S&H is greater than 8.75μs, additional circuit complexity is required.) Exclusive-ORing of Q7 and Q8 produces a synchronized 1.25μs gate to start the ADC. This circuit may not be the most versatile or elegant for the purpose. For those applications with longer S&H acquisition times or other requirements, some alternate circuit may be designed if that of Figure 15 is unacceptable.

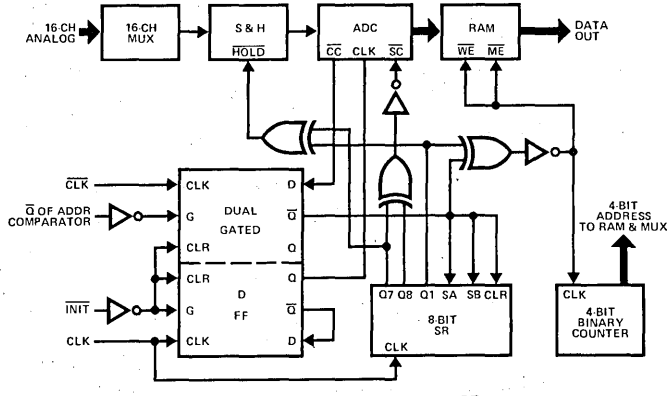


FIGURE 15. Sequencing Logic with SR

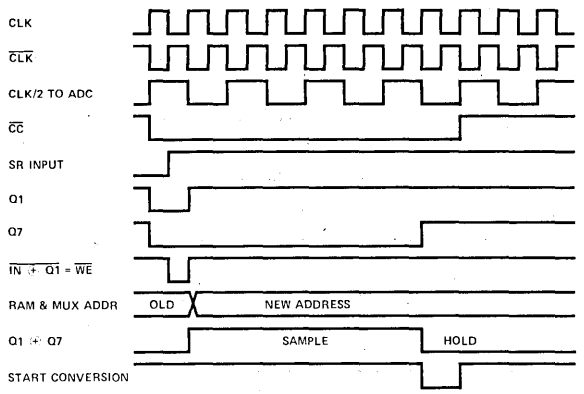


FIGURE 16. Timing for S-R Sequencing

The μ-computer interfaces shown in Figures 17 and 18 are similar to that of Figure 5. The PACE interface is seen to be slightly less complex than that of Figure 17 for 8-bit data-bus machines. A single DAU card with plug-in or strap options could be built to interface any of the three μCs considered. Such a universal circuit is shown in Figure 19. This circuit also includes an option to provide binary output for unipolar analog signals or complementary binary output for ± signals. In the case of binary output, the 13-16th data bits are set to 0. In the case of complementary binary, the sign bit is extended to the 13-16th data bits for valid recognition by the μC.

The total dissipation is 3.5 watts and cost is $11 per channel as shown in Table 5. Both are only slightly greater than those for the conventional DAU.

The ADC desired for this application is similar to the conventional ADC except that the ADC data output should be complementary to compensate for the data inversion within the RAMs. The AD1210 or AD1200 are thus ideal choices for an ADC in the multiplexed DAU with memory.

CONVERTER CHARACTERISTICS

Each approach to the DAU requires different characteristics of the ADC. Table 6 summarizes the requirements for each of the three DAU types. The sequential or addressed DAU types require similar ADCs. If the conventional addressed DAU must utilize bus drivers, the desired ADC characteristics are identical to those for the sequential DAU with memory. Only the parallel-conversion DAU is seen to require buffered TRI-STATE output latches.

By far the most important characteristic of an ADC for use in a parallel-conversion DAU is that it have buffered TRI-STATE output latches. It is desirable that it also have the other characteristics checked in Table 6. Items 1 and 2 are by far the most important of the desired characteristics. The need for item 1 has been discussed. TTL compatible control and data signals are desirable so that TTL-MOS and MOS-TTL interface buffers are not required between the ADC and the rest of the system. Dual output strobing makes it possible to wire-OR interface directly to an 8-bit data bus or to use only an 8-line buffer without the need for the output multi-

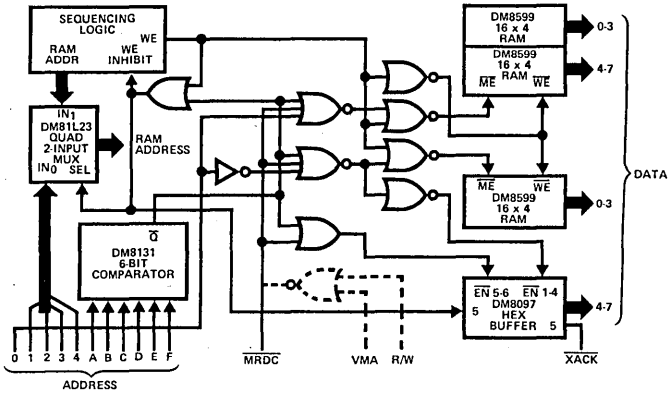


FIGURE 17. Address Comparator and Control for 8080 (6800)

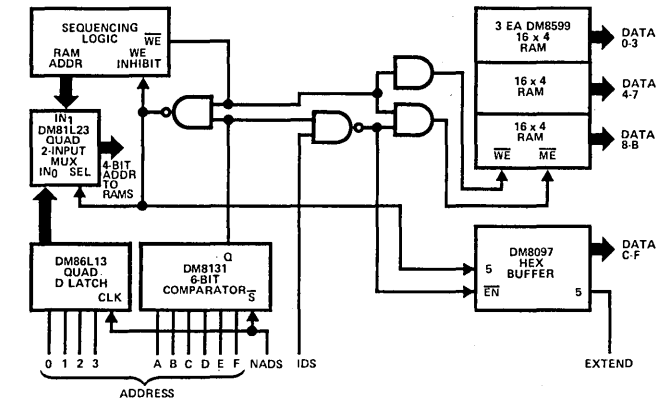


FIGURE 18. Address Comparator & Control for PACE

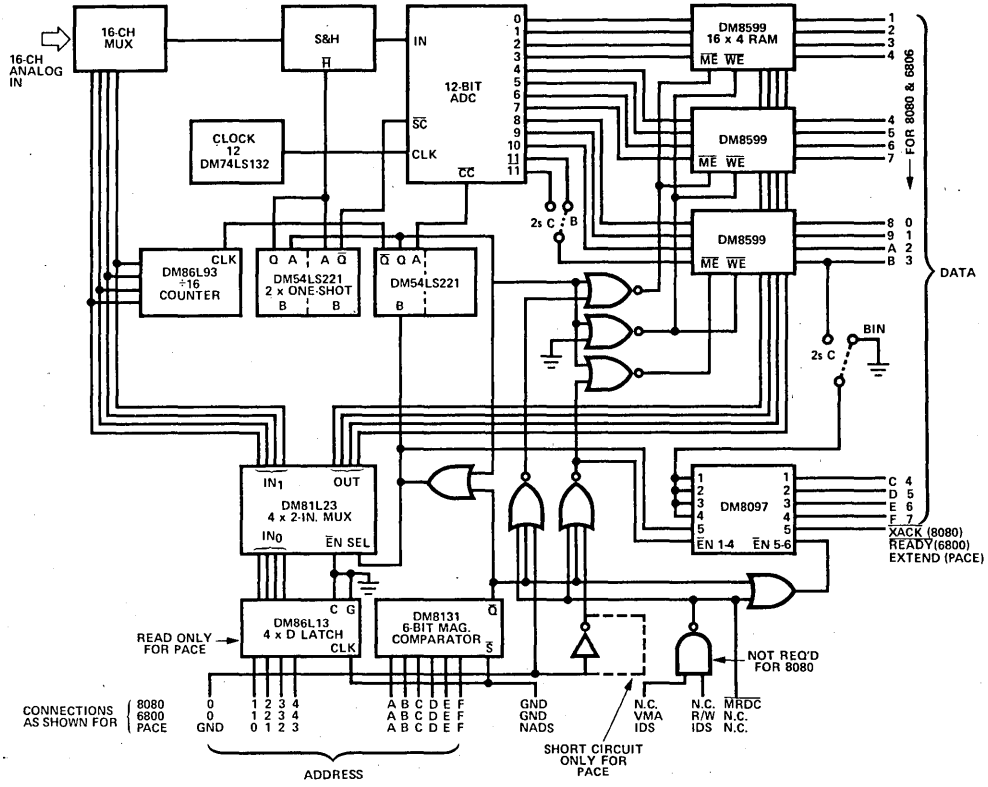


FIGURE 19. Multiplexed Immediate-Data-Access DAU

Table 5. Power & Cost, 16-Channel, 12-Bit Sequential with Memory

		P_D (mW)	$ (100s)
1 –	16-Channel MUX	300	19.55
1 –	S&H	500	74.50
1 –	ADC	600	40.00
1 – LH0070	Reference	45	5.00
3 – DM8599	256-Bit RAM	1200	15.36
1 – DM8097	6 x Buffer	325	1.65
1 – DM8131	6-Bit Comparator	250	2.56
1 – DM81L23	4 x 2-Input MUX	20	2.00
1 – DM74LS27	3 x 3-Input NOR	17	3.00
1 – DM7402	4 x 2-Input NOR	55	.35
1 – DM74L32	4 x 2-Input OR	12	.64
1 – DM86L93	÷16 Counter	25	2.11
2 – DM74LS221	2 x One-Shot	60	6.00
1 – DM74LS132	4 x NAND Schmidt	60	2.00
1 – DM86L13	4 x D-Latch	30	1.28
		3500	176.00
			$11/Channel

plexers shown in Figure 5 et. al., although a separate buffer is required in most systems. Tracking operation provides the higher speed useful in a conversion circuit without an S&H. Inhibiting data transfer to output data latches when the output is enabled prevents changing the output code while data is being read from the data bus. This function can be accomplished with an external gate, but could be convenient if handled within the ADC logic. Straight binary (not complemented) output is desired for all μC interfaces (except the 8080 when operating with Intel system bus drivers and receivers). As it may be necessary to add TRI-STATE line drivers to drive the data bus, data inversion can be handled by inverting buffers when required. The availability of both Q and $\overline{Q}$ outputs on the MSB simplifies data readout as binary or 2s complement without adding an external inverter. Table 6 has been arranged in the approximate order of preference for parallel-conversion DAU use; the preference will be different for multiplexed data.

The National MM5357 is the choice for an 8-bit ADC having buffered TRI-STATE output latches and TTL compatibility when converting ±5 or 0-5V analog inputs. If converting 0-10V inputs, it becomes 10V CMOS compatible. Several monolithic ADCs of 8 to 12 bits have been announced. These monolithic converters and future versions of them promise to bring converter prices down to a level which will make parallel-conversion economically feasible. Several hybrid converters have also been announced with attractive prices; however, it is the monolithics which promise the lowest ultimate cost. Features of several of these new products are compared in Table 7. Although only the MM5357 and the AD7550 are suitable in present form, their prices and characteristics show that the desired attributes are and will be possible at the needed prices.

The future ADC most suited for use in a parallel-conversion DAU might appear as in Figure 20. This

Table 6. Desired A/D Converter Characteristics

	Parallel Conversion	Sequential w/ Memory	Addressed w/o Memory
Buffered TRI-STATE Output Data Latches	x		?
TTL-Compatible Control & Data Signals	x	x	x
Dual Output-Enable (Bits 0-7 & Bits 8-11)	x		x
Counter Logic	UP/DN	SAR	SAR
Internal Comparator	x	x	x
Both Q & $\overline{Q}$ Outputs on MSB	x	x	x
Binary Output Polarity	Data*	$\overline{\text{Data}}$	Data*
Busy Output (TRI-STATE w/ Enable)	?		x
Internal Clock		x	x
Continuous Recycle when CC = SC	x		
Inhibit Data XFR to Latches when Enabled	x		

* Unimportant if Buss drivers used.

Table 7. Low-Cost Monolithic and Hybrid ADCs

	National MM5357	Analog Devices AD7570L	Teledyne 8702	National AD1210 (Hybrid)	Analog Devices AD7550
Number of Bits	8	10	12	12	13
Cost (in 100s)	$7.95	$69.00 (1-49)	$29.50	$24.95	$25.00
Conversion Method	Potentiometric	R-2R	Differential Charge Balancing	R-2R	Integrating
Logic Type	PMOS SAR	CMOS SAR	CMOS Integrating	CMOS SAR	CMOS Quad Slope
Conversion Time	25μs	20μs + Comp. Settling	20ms	130μs	40ms
Logic Interface at 5V Analog Sig. 0-10V	TTL CMOS	TTL TTL/CMOS	TTL TTL	TTL CMOS	TTL TTL/CMOS
External Circuits Required	Ref + Clock	Ref + Comparator	Ref	Ref + Clock	Ref
Output Buffered Latch?	Yes	No	Yes	No	Yes
TRI-STATE Output?	Yes	Yes	No	No	Yes
Separate Output Enables?	NA	Yes	Not Strobed	No	Yes
Output Code	Inverted	Normal	Normal	Inverted	2s Complement
Power Dissipation	170mW Dynamic	10mW Standby + Dynamic + Comparator	20mW Dynamic	140mW Dynamic	10mW Dynamic

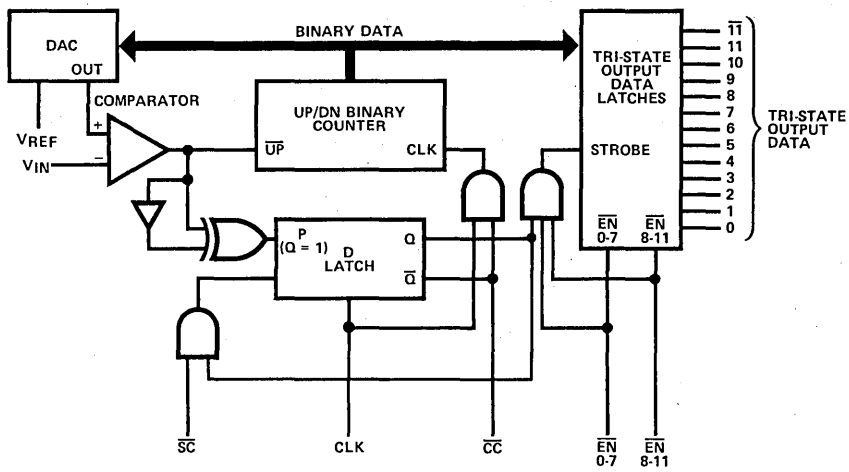


FIGURE 20. Tracking ADC for Parallel-Conversion DAU

design meets all the goals of Table 6. It could run at a clock rate of 0.25-1 MHz (1-4 μs conversion time) because it is a tracking converter, it contains TRI-STATE buffered output data latches, the separate high and low bit-enable lines allow two-byte operation of an 8-bit data bus, the output latches will not change state when the output is enabled, and the $\overline{CC}$ and $\overline{SC}$ terminals may be strapped for continuous conversion without missing a clock period. An 8- or 10-bit converter and possibly a 12-bit converter of this type could be built on a single chip without much difficulty. If not, a hybrid or two-chip design is practical. Where speed is not of importance, monolithic 10- or 12-bit converters can be built with integrating or voltage-to-frequency conversion techniques. The integrating technique possibly allows the greatest accuracy with the least circuitry, and is a prime contender for the application. As the integrating ADC utilizes both linear and digital circuits, it is normally of multi-chip design. However, as technology advances, it will become increasingly practical to produce the low-drift, low-offset amplifiers, integrators, and current sources required of a 12-bit ADC on a single reasonably small chip along with the necessary logic. A two-chip approach would likely be the choice today. We will certainly see some of these desired design features appearing on ADCs in the near future.

As far as ADCs and DACs are concerned, the entire makeup of their internal logic sections is different from that of conventional converters of today (except for the MM5357 and AD7550). Tables 6 and 8 outline the desired characteristics of ADCs and DACs for parallel-conversion and multiplexed systems. Figures 20 and 21 indicate the logic required. The ADC of Figure 20 is suitable for relatively high speed data acquisition without S&H circuits, while that of Figure 21 is suitable for slowly varying data only.

DATA DISTRIBUTION SYSTEMS

Until now, the discussion has centered entirely around the data acquisition end of the system. At first thought, the data distribution may seem almost trivial. However, there is still the address recognition and decoding plus the control functions. The conventional data distribution unit (DDU) has used a single DAC, a multi-channel analog demultiplexer, low-pass filters and possibly S&H

Table 8. Desired D/A Converter Characteristics

	Parallel Conversion	Multiplexed System
Hi-Z Digital Input Circuits	x	x
Strobed Data Input Latches	x	x
Dual Input Data Strobes (Bits 0-7 & Bits 8-11)	x	x
Optional Internal Inversion of MSB	x	x
Internal Output Amp & FB Resistors	x	?
Internal Reference	?	x

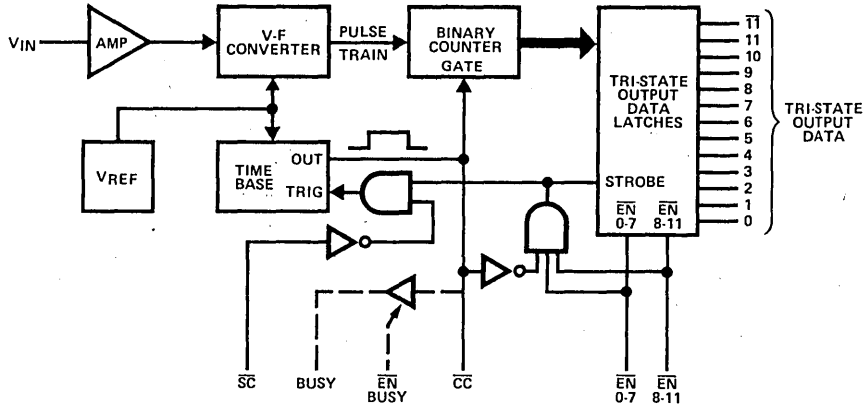


FIGURE 21. V-F ADC for Parallel-Conversion DAU

circuits on each channel reconverted to analog form. Such a system could benefit from a DAC with input data latches and separate (double-byte) input gating or strobing controls while a parallel-conversion DDU has even more need of these input characteristics.

The parallel-conversion DDU shown in Figure 22 would, if constructed with available DACs, require 12-bit input data latches ahead of each DAC. The characteristics desired of a DAC for this use are listed in Table 8. High impedance digital inputs prevent loading the data bus while a strobed input data latch allows entering data only in the addressed DAC and holding it until updated (thus performing the function of DAC and S&H). Separate input data strobes for low and high bits are used for the same reason as with the ADC, for alternate enabling on successive input data bytes. Figure 23 outlines the desired DAC for use in a parallel-conversion DDU.

The DDU address decoding and complexity is similar to that of the DAU. Input data strobing separated as 8 LSB and the remaining MSB is an advantage when used on 8-bit data bus systems. The cost per channel is essentially that of the DAC used. Likewise, for power dissipation. Practicality will be entirely dependent on ultimate cost of the converters. Advantages over a demultiplexed system are that only minimal output filters are required and that an output amplifier per channel is not required (already exists in each DAC).

CONCLUSION

Each type of DAU described exhibits unique advantages as indicated in the comparisons of Table 9.

Further reduction in the costs of monolithic converters will make the parallel-conversion type of DAU attractive where low-speed data is handled. For 8-bit data, this type of DAU is extremely attractive at this time because the DAU cost per channel is essentially that of an ADC which is as low as $8 in lots of 100.

It would seem that the multiplexed DAU with memory exhibits all of the advantages of the conventional random-addressed DAU plus all those of the parallel data conversion DAU except that the data in any specific channel may be older. Offsetting this single comparative disadvantage are significantly lower cost per channel, lower power requirements, and no requirement for special ADCs with buffered output latches. The multiplexed approach with memory is only slightly more complex or costly than a standard DAU, yet it brings the great advantage of high-speed immediate data access with significant cost savings over the parallel conversion technique.

Although the character of an ADC or DAC used in a parallel-conversion data system differs markedly from those used in the usual multiplexed data system, the processor interface requirements are similar or identical. The sense of μC bus control signals is of relatively minor importance so long as they are standardized among the several μC units available. Positive-true data and address signals are possibly a slight advantage over zero-true signals when TRI-STATE circuits are used. For the multiplexed system described, data inversion through the RAM would suggest the advantage of complementary binary output data from an ADC.

Conventional ADCs and DACs available today (except the MM5357 and AD7550) do not have the characteristics needed for parallel-conversion systems. However, this picture is changing as more units are designed for direct data bus interface. Fortunately, however, the multiplexed DAU with memory does not require the bus oriented type of ADC. There is at least one available DAC which includes the dual-strobed input data latches suggested for direct data bus interface; I would expect to see others appearing in future designs, both monolithic and hybrid.

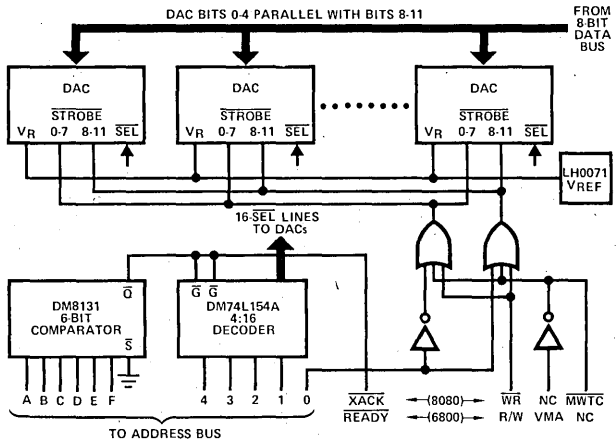


FIGURE 22. Parallel-Conversion DDU for 6800 or 8080

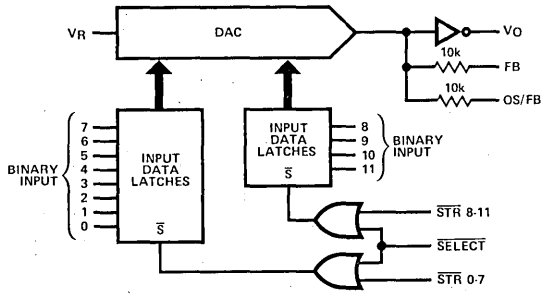


FIGURE 23. DAC for Parallel-Conversion DAU

Table 9. Comparison of Three Types of DAU

Features of DAU 16-Channel, 12-Bit	Conventional Random-Addressed	Parallel-Conversion Without S&H	Multiplexed With Memory
Approx. Component Cost (100s) (based on a $25 ADC)	$9.38	$26	$11
Approx. Power Dissipation	2.8W	4.3W	3.5W
Data Bandwidth/Channel t_{conv} = 50μs t_{acq} (S&H) = 10μs	200Hz	10Hz (tracking: t_{conv} = 4μs)	200Hz
Data Access Time	60μs	< 0.5μs	< 0.5μs
Software	60μs delay or subroutine and return on flag	as memory access	as memory access
Logic Interface Complexity	9 DIP	6 DIP	13 DIP
No. of IC Packages			
ADC Requirement		TRI-STATE buffered output data latches	

RMS Converters and Their Applications

National Semiconductor
Application Note 180
John T. Lee
Hybrid Special Products

Introduction

A true RMS converter is a device which converts a signal (DC, AC, AC+DC) to its equivalent DC heating value. These devices are useful in fundamental measurements of virtually all waveforms.

SOME BASICS ABOUT RMS CONVERTERS

I. What is the RMS Value of a Waveform?

The Root Mean Squared (RMS) value of a waveform is a fundamental measurement of that waveform: it is a measure of the waveform's heating value when applied to a resistor.

A fundamental theory of Fourier Analysis states that any periodic function may be represented in a trigonometric series. This series is a sum of sinusoidal components having different frequencies and amplitudes. These components are all multiples of the fundamental frequency. Thus, for a periodic function, the power content (also its mean-squared value) in the period T is defined to be:

$$\text{mean square value} = \frac{1}{T}\int_{-T/2}^{T/2}[f(t)]^2dt = \sum_{n=-\infty}^{\infty}|Cn|^2$$

where the Cns are the complex Fourier coefficients of the function. It is seen that if $f(t)$ is a voltage or a current waveform, then the mean square value represents the average power delivered by $f(t)$ to a 1 ohm resistor. Summing its discrete components, one can obtain the power content of the signal. A graph of these components vs frequency is known as a power spectral density plot.

The RMS value is defined to be:

$$\text{RMS} = \sqrt{\frac{1}{T}\int_0^T[f(t)]^2dt}$$

Thus, one can see that the RMS value is just the square root of the mean square value.

Since the mean square value of a periodic function is the sum of the mean square value of its discrete harmonics (without regard to their phases) it is seen that any signal with the same mean square value (thus RMS value) will dissipate the same amount of energy, over a period, in a resistor.

Whereas periodic signals may be completely described by their amplitudes, phases, and frequencies, random signals are those where future behavior cannot be predicted. Random signals may only be described by quantities such as the RMS value, power spectral density, and probability distribution. If for a random signal there exists a statistical value such as the RMS that is independent of time, then this signal is said to be stationary. The RMS value of any stationary zero mean random signal is equal to the standard deviation of the signal.

Whereas periodic signals have a discrete power density spectrum, random signals have a continuous spectrum. The RMS value of a random signal may be defined to be:

$$\text{RMS} = \sqrt{\lim_{T\to\infty}\frac{1}{T}\int_0^T f(t)^2dt}$$

For a random signal, then, it is necessary to break the signal up into many narrow bands in order to investigate its power spectral density.

II. Why RMS Converters? Why Not Average Detect?

Since the mean square value (hence RMS) measures the power content of a signal, it provides a universal scale of measurement. An RMS measurement will give the intensity of a random phenomenon when averaged over a time interval. Besides periodic signals, phenomena such as acoustic noise, electrical noise, and mechanical vibration may be characterized. It is seen that instruments that read RMS values would be highly desirable.

Until recently, due to the high cost of RMS converters, most AC voltmeters did not read the RMS value of a waveform. Instead, they were average reading and RMS calibrated. This is done by taking the Mean Averaged Value (MAV) and multiplying by a factor of 1.11. This calibration is accurate only for measuring sinewaves. However, if the signal is not a pure sinewave, this type of instrument could lead to great errors. For example, such meters would read about 11% low on gaussian noise and about 11% high on symmetrical square waves. Note that if one knew beforehand that the waveform to be measured consisted of symmetrical square waves the meter could be calibrated accordingly. However, this meter would hardly be useful for anything else. Also, since many signals may change waveform during measurement, it would be impossible to try to calibrate the meter.

An example of a varying waveform would be the output of a ferroresonant line voltage regulator. The waveform could change from a sinewave to a square wave; when the output is a sinewave the average type meter would read correctly, however when the output is a square wave the meter would read in error of as much as 11%.

Another example would be the voltage from an SCR controlled circuit. An averaging meter would read correctly only during 180° condiction angle; it would read in error of 51% at 45° conduction angle.

Yet another example would be the output of an audio system during intermodulation testing. The true RMS value is insensitive to the ratio of frequencies, while the average value is highly sensitive to this ratio. Table I compares normalized readings between RMS and average detecting type meters. It is seen that whenever a waveform other than sinusoidal is to be measured, an RMS type meter should be used.

Table I

A Comparison of RMS and AVG Detecting Type Meters

Waveform		RMS	AVG
Sine		1	1
SCR Cond ∡	180°	1	1
	90°	0.707	0.5
	45°	0.301	0.15
Gassian Noise		δ*	0.89δ*
Zero Based Pulse Train	10% duty cycle	A/$\sqrt{10}$	A/10
	1% duty cycle	A/10	A/100

* δ = standard deviation = RMS value

TABLE I. A Comparison of RMS & AVG Detecting Type Meters

III. What Kinds of RMS Converters Are There?

There are basically three methods of RMS measurements:

1. **Thermal.** This method is achieved by converting an unknown voltage or current into heat in a known value of resistance.
2. **Direct Computing.** From the definition of RMS,

$$RMS = \sqrt{\frac{1}{T}\int_0^T f(t)^2 dt}$$

we can see that the RMS value may be determined by first squaring the waveform, then averaging it, and then taking the square root. This method is illustrated in Figure 1.

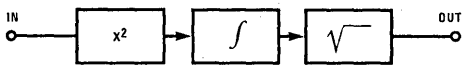


FIGURE 1. Direct Computing Type RMS Converter

3. **Implicit Computing.** This scheme is similar to the second one with the square root performed by feedback and the squaring done by log method. This method is illustrated in Figure 2.

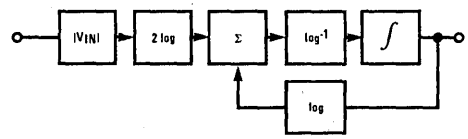


FIGURE 2. Implicit Computing Type RMS Converter

Of the three methods mentioned above, the Implicit Computing method is by far the most desirable – since a converter of this type can achieve great accuracy, wide bandwidth, high dynamic range, and low cost. The LH0091, National Semiconductor's true RMS converter, is such a unit.

SPECIFICATIONS

An ideal RMS converter would have infinite crest factor response, infinite bandwidth, and no errors due to conversion. Since this is not yet an ideal world, the performance of a practical converter will be discussed.

A practical converter should have sufficient bandwidth to respond to the entire spectrum of the measured signal; it should also have adequate crest factor response and accuracy to meet the particular application. Thus, these are important characteristics of an RMS converter.

1. **Crest Factor.** Crest Factor is the peak signal value divided by the RMS value. In general, the higher the crest factor a signal has, the higher the conversion error will be for a converter. This is due to internal circuit limitations. However, most signals encountered in measurement do not have high crest factors. For example, sinewaves have a crest factor of 1.414; triangular waves have CF of 1.73; for an SCR output, the CF varies from 1.414 to 3 as power output varies from 100% to 10%. One of the few waveforms which has high crest factor is noise; however, the crest factor of common noise is 3 or less for 99.7% of the time. The probability of a gaussian noise having a crest factor greater than 4 is 0.01%.

   A zero based pulse train is one of the rare waveforms which can have very high crest factors; such a pulse train with a 1% duty cycle will have a crest factor of ten. Using the high crest factor connection, the LH0091 will respond to signals with crest factor of 10 with typically no more than 0.2% error.
2. **Accuracy.** The accuracy of a converter is in reality its conversion error. Error is the amount by which the actual DC output differs from the theoretical value. It is customary to define error as a sum of a fixed offset term and a percent of reading term. For the LH0091, both the unadjusted and the adjusted total errors are specified; they are 20 mV ± 0.5% and 0.5 mV ± 0.05% respectively.

3. **Frequency Response.** The frequency response of a computing type RMS converter has an upper and a lower bound; on the low frequency end, it depends on the size of averaging capacitor; on the high frequency end, it depends on internal circuitry. Since this type of converter uses an RC filter for averaging, the RC time constant is critical for low frequency response. The RC time constant should be much greater (10 times or more) than the period of the lowest frequency component of the signal. For the LH0091, the RC time constant is simply the product of a 10kΩ resistor and the external capacitor. Low leakage capacitors should be chosen.

4. **Frequency for Specified Adjusted Error.** This is the frequency below which the output will maintain the adjusted accuracy (specified for sinewaves). For the LH0091, the device will maintain the adjusted accuracy to 70kHz, typically, for a 7 Vrms input.

5. **Frequency for 1% Additional Error.** This is the frequency below which the device will have an additional error of less than 1% of the initial reading (midband). This is also specified for sinewaves. This frequency is typically 200kHz for a 7 Vrms input with the LH0091.

APPLICATIONS

RMS converters may be used in measurement of virtually any waveform. The examples below are only a few of the many possible applications.

A. Spectrum Analysis

Spectrum analysis is useful in characterizing random phenomena, identifying sources of mechanical vibration and noise. It is also used in characterizing the energy content of a signal. The RMS converter may be used in such an application.

As shown in Figure 3, the signal is passed through a tunable bandpass filter, and then it is read by the RMS converter. The output from the RMS converter represents the energy content in the narrow band of frequencies. If this procedure were repeated many times (each time changing the center frequency of the filter) we would have the power spectral density of the signal.

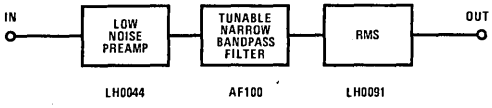


FIGURE 3. Application of the RMS Converter in Spectrum Analysis

B. Total Harmonic Distortion Meter

A simple and low cost total % harmonic distortion meter is shown in Figure 4.

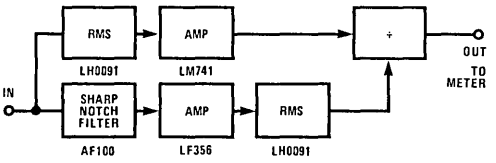


FIGURE 4. Total Distortion Meter

It is seen that the amplitude of the signal from which the fundamental has been rejected is divided by the amplitude of the composite signal; thus the output is a measure of total harmonic distortion.

C. Noise Meter

A complete noise meter is shown in Figure 5. Note that this meter will indicate the total noise within the frequency band of interest. However, if a tunable filter were added, one could plot the noise spectrum of the environment, thus being able to identiry the sources of noise.

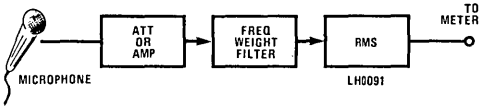


FIGURE 5. Noise Meter

D. Current Measurement

A current meter capable of measuring complex current waveforms is shown in Figure 6. Note that since the RMS converter is used, virtually any current waveform may be measured. Examples of such current waveforms are pulse train, SCR, and noise.

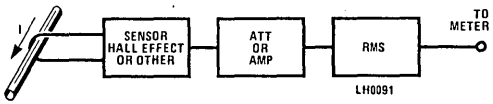


FIGURE 6. Current Meter

E. DVM AC Interface

Another application of the RMS converter would be an AC interface to a DVM. With such an interface, a DVM may be used to measure complex signals. Since most computing type RMS converters have relatively low input impedance, a buffer should be added as shown in Figure 7.

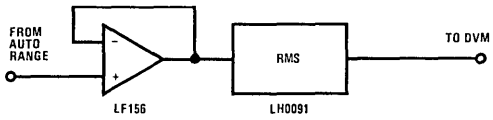


FIGURE 7. DVM AC Interface

F. Random Vibration and Noise

Random phenomena, such as random vibration and electrical noise, may be described only by such quantities as RMS, power spectral density, and probability distribution of magnitudes.

The spectral density of a wide band random signal is defined to be the mean square value of the signal per unit bandwidth. It is seen that we can obtain a kind of spectral density by dividing the RMS value (band limited) by the square root of the noise bandwidth, where:

$$\text{noise} = E/\sqrt{\Delta f} \text{ volts/Hz}^{1/2}$$

The result can be interpreted as simply the RMS noise voltage in 1 Hz of bandwidth. Thus wideband electrical noise may be measured as shown in Figure 8. If the filter in Figure 8 is tunable, then it would be possible to plot the spectral density of the signal.

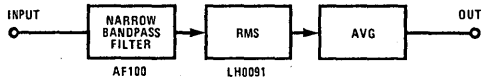


FIGURE 8. Measurement of Noise

For random mechanical vibrations, an accelerometer and a preamp are added to the circuit. This is shown in Figure 9.

FIGURE 9. Application of the RMS Converter in Random Vibration

G. Ball Bearing and Other Vibrational Failure Monitor

A very interesting application of the RMS converter is in the monitoring of ball bearing and other vibrational failure. A discussion is given on the ball bearing, but the principle is applicable to any vibrational monitors.

It has been found* that a knowledge of bearing geometry is sufficient to enable the prediction of frequency of fault-induced vibration. There are natural frequency formulas relating directly to bearing geometry. When vibration is generated by impact due to defects, the impact frequencies are usually much lower than the natural frequency of the outer bearing race. Thus the natural frequencies are brought to life. An example of this would be a bell of 200 Hz natural frequency being struck several times a second: the corresponding plot of the oscillation would tend to exhibit 200 Hz and ignore the striking frequency.

It is possible to monitor the fundamental frequency of the outer race. However, it may be necessary to monitor a band of frequencies, depending on the application. If an RMS reading is taken to detect the normal operation level of a new bearing (after a few hours of operation) a safe level may now be set. Thereafter, if the RMS level exceeds the set safe level, an alarm could be triggered. A circuit for such a function is shown in Figure 10. If the bandpass filter is tunable, diagnosis of the failure can be performed.

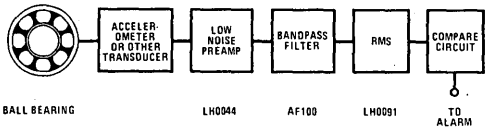


FIGURE 10. Ball Bearing Failure Monitor

*See *Vibration & Acoustic Measurement Handbook*, Blake & Mitchell, Spartan Books, 1972 and "Detection of Ball Bearing Malfunction," *Inst. & Control*, Dec. 1970.

CONCLUSION

In conclusion, it has been found that the RMS converter is a versatile component. Applications range from complex current waveform measurement to ball bearing failure monitor. The examples cited in this note are but a few of the many possible applications.

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Digital Telephony and the Integrated Circuit CODEC

National Semiconductor
Application Note 215
Jim Smith

INTRODUCTION

Before beginning a detailed discussion on PCM CODECs (Pulse Code Modulation COders/DECoders), it is important to consider the nature of voice frequency communication and the digital telephone network. This, of course, is the primary application of any PCM CODEC. Basically, a digital telephone network uses switching and transmission techniques that are generally considered appropriate for a digital computer rather than a telephone communications network. High speed digital logic, arithmetic logic units, extensive use of digital memories, etc., are important aspects of digital telephony. But the success and acceptance of digital techniques for switching and transmitting voice signals depends upon the viability of an efficient and cost effective analog-to-digital and digital-to-analog interface. Without such an interface, the message switching telephone network must remain, at least in part, an analog network.

Although patented in 1937 by Alex H. Reeves, (France), PCM was not used commercially until the 1950's. At that time, the Bell System used PCM in a transmission system designed to increase the message carrying capacity of short-haul cables. In this application, where the performance of FDM was considered inadequate, the voice signals were band-limited to 4 kHz, sampled and coded into digital words. These digital words were then time multiplexed with identical signals from 23 additional channels and transmitted over a single transmission cable pair. At the receiving end, the reverse operation took place and to complete a telephone conversation path, a symmetrical circuit arrangement was provided for voice communication in the opposite direction. This entire system was named channel bank and designated as D1. It used cable facilities designated as T1.

To the end user, the D1 channel bank system is 24 voice channels at either end of a T1 span and little attention to the channel bank system is necessary. No obvious switching functions are involved, and in fact, the telephone subscriber connected to a central office (CO) via a D1 channel bank is usually not aware of any alterations in the normal services from the CO.

The D1 system and its successors (up to D4) are strictly transmission systems that use digital coding and time division multiplexing to increase short-haul cable call handling capacities. For that application, the important advantages of PCM are not exploited. The use of PCM in long-haul transmission for noise-free signal regeneration and in switching systems to eliminate electromechanical circuits has never been fully developed because alternative approaches were usually more economical. The advantages of PCM did not appear to warrant its use when compared to the cost.

The trend, however, is beginning to change. The introduction of the integrated circuit CODEC is only the beginning of the "siliconization" of the digital telephone network line interface circuit. This fact and the inherent advantages of PCM telephony have prompted closer examination of digital telephony for all phases of the telecommunications network.

DIGITAL TELEPHONY

A realizable digital telephone network can be configured in several different ways, but basic to any approach is the need to represent the original signal as discrete time samples, the desire to multiplex many signals together to increase the call capacity of switching and transmission equipment and finally, to digitize the time samples so that degradation of the message signal will be eliminated as it is transmitted and switched through several different systems. Although time sampling and digital encoding are usually only performed once for any particular connection, multiplexing can be performed at several different points in the network. In a shared CODEC system, the first level of multiplexing will be analog, usually a pulse modulation technique like pulse amplitude, pulse width or pulse position modulation (PAM, PWM or PPM). This arrangement is necessary because the shared CODEC must convert the time samples of several different channels into a continuous digital bit stream. The time samples of 24 or 30 channels are multiplexed together onto a single wire or hyway and transmitted to the CODEC for coding. Obviously, the complementary procedure is required for decoding. A single channel CODEC arrangement, however, uses a CODEC at each line interface channel. The voice band-limited signal is time sampled and directly converted to a digital signal prior to digital multiplexing with other similar channels. This arrangement eliminates the often troublesome and noise sensitive pulse modulation multiplexing and allows the flexibility of directly interfacing both voice and data channels with the digital network.

Regardless of the CODEC arrangement desired, the concept of representing the original signal as time samples is fundamental to digital telephony. It is this sampling process that allows a continuous analog signal to be digitally coded and time division multiplexed onto a multi-channel transmission and switching hyway. It is, therefore, relevant to present a brief description of the sampling theorem.

Simply stated, a band-limited analog signal that is time sampled at twice the highest frequency in the band of interest will yield regularly spaced samples that contain all of the information of the original signal. It is important to band-limit the input signal because time sampling will cause aliasing of unwanted high frequencies down into the band of interest. Consider, for example, the Fourier transform of a band-limited signal f(t):

$$f(t) = \int_{-1/2T}^{1/2T} F(f) e^{j2\pi ft} df$$

where the bandwidth in hertz of f(t) is equal to 1/2T and the function F(f) = 0 for $f > 1/2T$ or $f < -1/2T$. Since F(f) is only defined between $-1/2T$ to 1/2T, it can be represented by the Fourier series:

$$F(f) = \sum_{n=-\infty}^{\infty} C_n e^{j2n\pi ft}$$

for $-1/2T < f < 1/2T$. The coefficients in this summation are defined by:

$$C_n = \int_{-1/2T}^{1/2T} TF(f) e^{-j2n\pi fT} df$$

Comparing this to the original Fourier transform for f(t), it is clear that the constant C_n represents the value of f(t), times a constant, at T intervals:

$$C_n = T\, f(-nT)$$

Time samples of f(t), C_n, taken at twice the highest frequency in the passband, will represent the original signal f(t) times a scale factor. Substituting C_n back into previous formulas yields:

$$f(t) = \sum_{n=-\infty}^{\infty} f(nT) \frac{\sin \pi/T\,(t - nT)}{\pi/T\,(t - nT)}$$

The time samples, taken T seconds apart, can be reconstructed into the original function f(t) if they are passed through an ideal low pass filter [impulse response h(t)] with gain T and bandwidth 1/2T hertz.

$$h(t) = \frac{\sin \pi/T\, t}{\pi/T\, t}$$

In telephony, the frequency band of interest is 300 Hz to 3 kHz. To allow worldwide transmission of digital telephone signals, the 8 kHz sample frequency has been established as an international standard. This allows a signal bandwidth of DC to 4 kHz to be represented by time samples taken every 125 μs. Although the time sampled signal could now be multiplexed with other similar signals, it is more appropriate to consider the single CODEC approach of encoding to the digital PCM format before any time division multiplexing (TDM) is performed.

PULSE CODE MODULATION

Standard PCM telephony uses one of two non-linear transfer characteristics to compand the time sampled analog input signal into a compressed range of 8-bit digital output words. The reasons for companding are simple. The amplitude probability distribution of telephone message signals is not uniform. There is a heavy concentration of small amplitude signals where a relatively low distortion level would be required to insure an adequate signal-to-quantizing distortion (S/D) ratio. Secondly, the dynamic range of the signals encountered in a typical telephone message may span 40 dB. A uniform CODEC – one that does not compand input signals into a compressed output range – would experience an S/D ratio degradation of 40 dB for weak signals as compared to strong ones. Since low level signals need low level distortion and high level signals can tolerate higher levels of distortion, it would be desirable to devise a digital coding scheme that provided a constant S/D over a wide dynamic range. PCM is such a scheme.

As mentioned earlier, two coding characteristics are in general use today. The first, named μ-255, is used in North America and parts of the Far East while the second, the so called European A-law, has been adopted by most of the remaining countries in the world. The goal of attaining a constant S/D performance over a wide dynamic range means that distortion levels must be proportional to signal amplitude for all signal levels. This implies the use of a logarithmic compression law modified to overcome the mathematical difficulties of using a true logarithmic transfer function. The μ-law, normalized for a coding range of ±1 is defined as:

$$F(x) = \mathrm{sgn}(x) \frac{\ell n(1 + \mu |x|)}{\ell n(1 + \mu)} \qquad -1 \leq x \leq 1$$

where μ is generally set equal to 255. The A-law characteristic, again normalized for a ±1 coding range, is defined as:

$$F(x) = \mathrm{sgn}(x) \frac{1 + \ell n\, A |x|}{1 + \ell n\, A} \qquad \frac{1}{A} \leq |x| \leq 1$$

$$F(x) = \mathrm{sgn}(x) \frac{A |x|}{1 + \ell n A} \qquad 0 \leq |x| \leq \frac{1}{A}$$

where A is generally set equal to 87.6.

The definitions for the μ and A coding laws define smooth curves. In practice, however, these laws are usually implemented as piecewise linear approximation transfer characteristics. One such approximation for the μ-law characteristic is comprised of 15 linear segments centered about the origin of the transfer curve *(Figure 1)*. The first segment, which passes through the origin, contains 32 uniform steps corresponding to 32 digital code words, 15 positive, 15 negative and two codes for

zero. Here is where a primary difference between the μ and A-laws occurs. While μ-law defines two codes for zero volts and is best described as having a mid-tread zero point, the A-law defines no code for zero, a mid-riser condition *(Figure 2)*. The two zero codes of the μ-law characteristic actually represent one normal step that is divided into two half-steps by the y-axis of the transfer curve. These half-steps represent the lowest resolvable signal of the μ-law characteristic. The next two linear segments, one positive and one negative, each contains 16 uniform steps, but the step size or difference between voltage outputs for each incremental change of the input digital word will represent a two-fold change in output voltage when compared to the same incremental change in the first segment. Thus, the "graininess" of the transfer characteristic has doubled. This process of doubling step size with each higher segment continues until the step size in the final two μ-law segments is 128 times larger than the step size in segment one. This arrangement provides 255 discrete output voltages, 127 positive, 127 negative and zero volts.

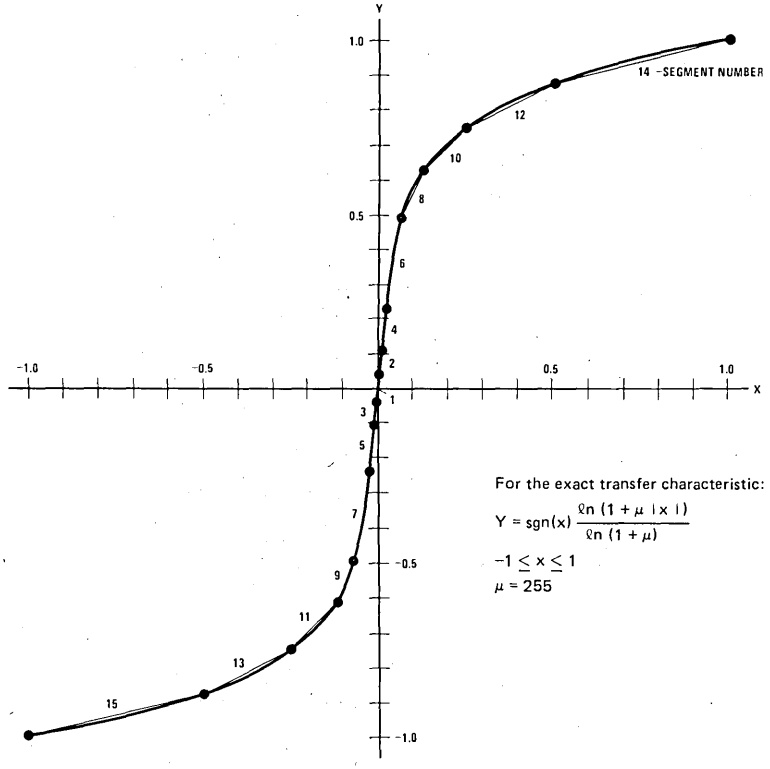


FIGURE 1. μ-Law Transfer Characteristic (Exact and Piecewise Linear Approximation Characteristics)

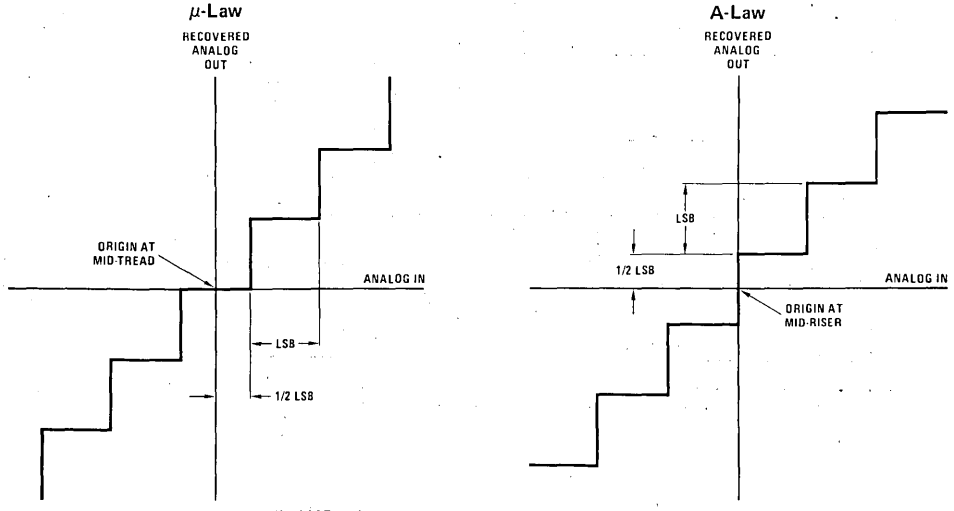


FIGURE 2. Transfer Characteristics Around Zero

If all steps of the piecewise linear approximate μ-law characteristic were normalized to the lowest resolvable step, the first 1/2 step, there would be 8159 positive and 8159 negative normalized steps in the entire transfer curve. This is equivalent to a low level resolution that could only be matched with a 13-bit linear coding characteristic and a dynamic range of approximately 78 dB. Of course, companding will mean a lower resolution at the higher signal levels (only the equivalent of 6 bits in the last segments). However, this μ-law characteristic does yield an S/D ratio that is nearly constant for approximately 40 dB.

The A-law companding characteristic can be approximated in piecewise linear fashion by 13 linear segments centered about the origin of the transfer curve. Again, the first segment is centered on the origin but unlike the μ-law approximation, this first segment contains 64 uniform steps corresponding to 64 digital codes. Thirty-two of the codes represent positive voltage values and 32 represent negative values. No codes, as mentioned above, are reserved for zero volts. As with the 15-segment μ-law characteristic, the step size doubles for each higher linear segment until the step size in the last positive and negative segment is 64 times larger than the step size of the first segment. Normalizing all step sizes to the smallest step would generate a total of 4096 normalized steps, 2048 positive and 2048 negative. This is a low level linear resolution of 11 bits diminishing to 5 bits in the last segments. The approximate dynamic range of the piecewise linear A-law characteristic is 66 dB. S/D ratio is relatively constant for 30 to 35 dB.

PCM transmission speeds are controlled by two variables, the number of transmitted bits per sampling period (called a frame) and the period of the sampling signal. The generally accepted length of a single PCM word is 8 bits. Because sampling is performed at an 8 kHz rate, the period of the sampling signal is 125 μs. A single PCM channel must transmit 8 bits of digital information every 125 μs. This is a transmit (or receive) frequency of 64 kHz. Twenty-four channels would normally require a 24 times increase in the single channel frequency but the Bell System uses a multiplex scheme that combines 24 8-bit PCM words with one framing bit for every 125 μs frame. In one frame, 24 x 8 = 192 + 1 = 193 bits must be transmitted. This is a transmission frequency of 1.544 MHz. A 32-channel system transmit frequency is simply 32 x 64 kHz = 2.048 MHz.

THE TP3000 IC CODEC

Two integrated circuit single channel PCM CODECs have been developed at National Semiconductor. The TP3001 μ-law CODEC and the TP3002 A-law CODEC are each composed of two integrated circuits. The linear functions of input and output sample and hold, autozeroing, successive approximation comparison, DAC voltage reference and reference polarity switching are contained in the 20-pin LF3700 BI-FET™ IC. The digital circuitry-successive approximation register (SAR), non-uniform μ or A-law digital-to-analog converter (DAC), control logic and high speed input and output PCM buffers — are contained in one CMOS package. For a μ-law system, the CMOS part is the 28-pin MM58100, while the A-law system uses the 22-pin CMOS MM58150. A complete μ-law system (TP3001) would use one LF3700 and an MM58100. An A-law system (TP3002) would use the same linear part with the digital MM58150. A block diagram of the TP3001 is shown in *Figure 3*.

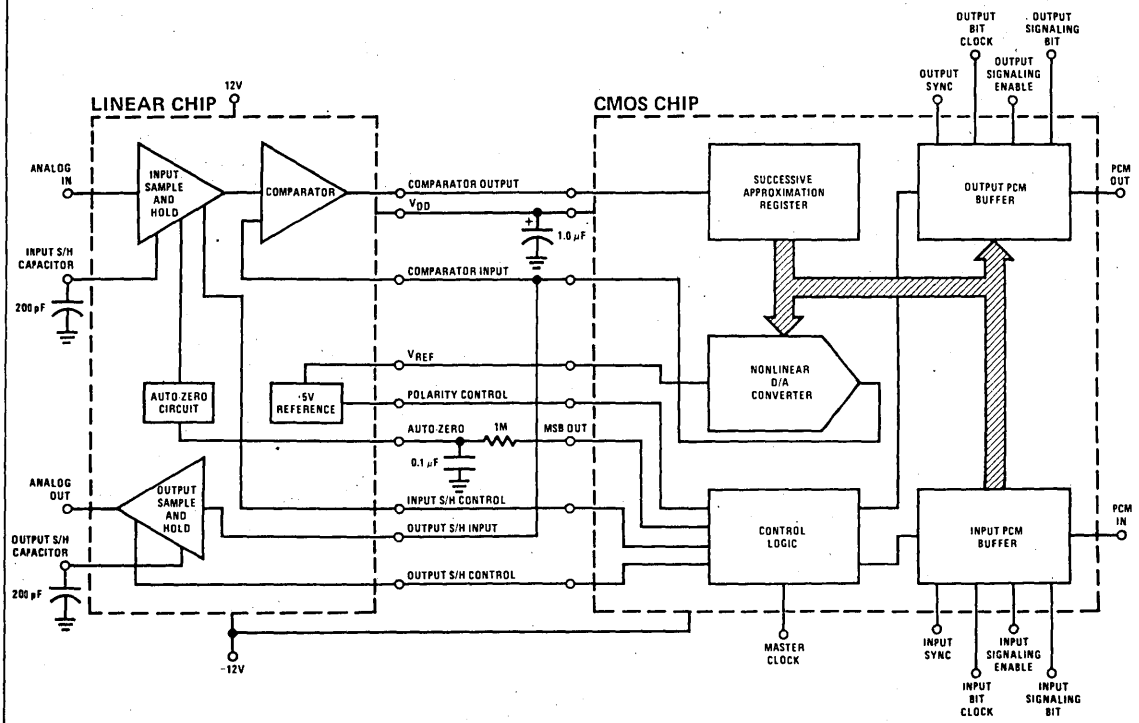


FIGURE 3. TP3001 System Block Diagram

Because sampling will cause aliasing of high frequencies down into the passband, all analog signals applied to the TP3000 must be low pass limited to frequencies below 4 kHz. The NS active filter AF133 is designed for this low pass filter function. Likewise, analog output signals from the TP3000 output will contain sidebands around multiples of the 8 kHz sampling frequency, as well as the sin x/x distortion introduced by the output sample and hold amplifier. A low pass filter with inverse sin x/x correction will restore the TP3000 analog output to its pre-encoding appearance. The NS AF134 is a filter for that function.

Auto-zero circuitry is required for the input sample and hold amplifier to guarantee that the LSB of an idle channel is confined to the first few codes of the transfer characteristic. Without this confinement, idle channel noise, crosstalk enhancement and distortion would increase. Auto-zero for the output sample and hold amplifier is not required since DC voltage offset at the CODEC analog output can be removed by AC coupling the output to the low pass filter.

The auto-zero technique used is a simple time averaging of the PCM code sign bit. By averaging the toggling of this bit over a time constant of approximately 100 to 1000 ms, and adjusting the DC offset control of the input sample and hold to minimize the detected DC component, the PCM output can be forced to contain equal numbers of positive and negative codes over an extended period of time.

The TP3000 voltage reference is a band-gap bipolar reference *(Figure 4)*. The device develops its voltage reference by differencing the voltage drop across two forward biased base emitter transistor junctions. The equation defining this voltage is:

$$V_{REF} = C\frac{kt}{q}\ell n\frac{8A}{A}$$

where C is an amplification constant, k is Boltzmann's constant, q is the electric charge, and A is the emitter junction area. By controlling the area ratio of the two base emitter junctions and compensating for temperature effects with a reverse temperature coefficient introduced via a resistor network, the output voltage of this circuit will be virtually free of significant long term drift.

The DAC used in the TP3000 is a modified grounded ladder R/2R structure *(Figure 5)*. As it turns out, the binary division of a reference voltage afforded by this configuration exactly matches the chord end points of the A-law PCM transfer characteristic. With a slight modification, it will also fit the μ-law characteristic. To achieve the piecewise linear approximation, 16 uniformly spaced taps are brought out from each R resistive element. These taps form the source of an MOS analog switch which is the first level of an all MOS switch tree decoder. Proper decoding of a PCM digital word will select a single DC voltage from the DAC ladder.

The DAC is a grounded ladder structure so that the highest accuracy codes are developed near the ground reference. This configuration will develop positive output voltages with a positive reference applied and negative voltages with a negative reference. The generation of a positive and negative reference voltage is achieved by using a high accuracy polarity switch on the output of the band-gap reference.

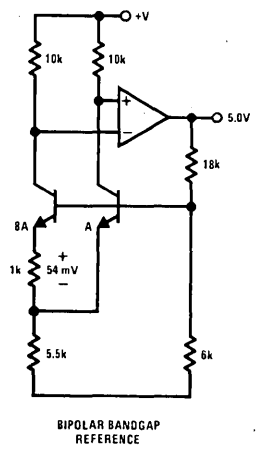
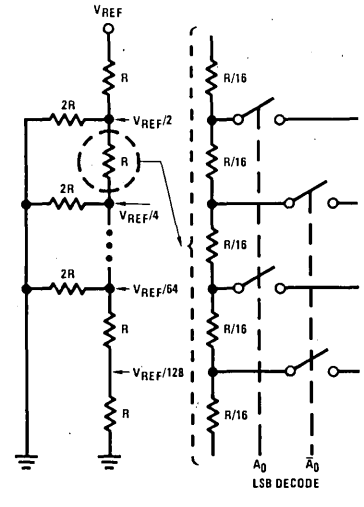


FIGURE 4. The CODEC Voltage Reference



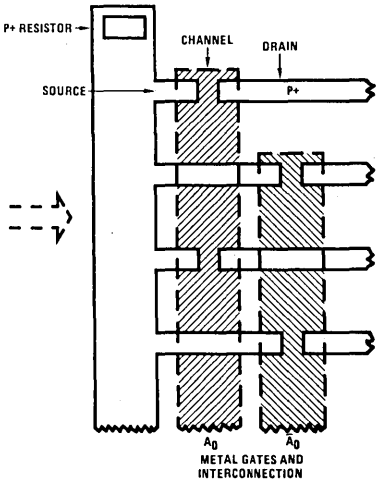


FIGURE 5. MOS DAC for Companding A-Law

The operation of the TP3000 CODEC is clearly described in the data sheet and will only be briefly covered here. For maximum flexibility, the TP3000 is designed with separate clocks and control inputs for PCM transmission, PCM reception and, in the TP3001 μ-law CODEC, signaling control. A master clock input, F_C, is also provided so that internal CODEC timing functions are not dependent upon PCM bit clocks. An asynchronous μ-law system, with signaling, would need direct independent control of all clocks and controls. A synchronous system, with separate signaling arrangements, would combine many of the separate clocks and controls.

PCM data is clocked into the TP3000 with the F_{bi} clock. Clocking occurs on the positive clock edge if F_i is at logic high. Hence, the clocking is enabled by the input word clock F_i. F_{bi} can be any frequency between 64 kHz and 2.048 MHz, but F_i must be 8 kHz. The negative going edge of F_i initiates the decode interrupt cycle of the TP3000.

PCM data is clocked from the TP3000 with clock F_{bo}. Clocking will occur on the negative edge if F_o is at logic high. Like F_{bi}, F_{bo} can be any frequency from 64 kHz to 2.048 MHz, but F_o must be 8 kHz. The positive edge of F_o begins the shifting out of the prior PCM word and begins the encoding of a new analog sample.

APPLICATIONS

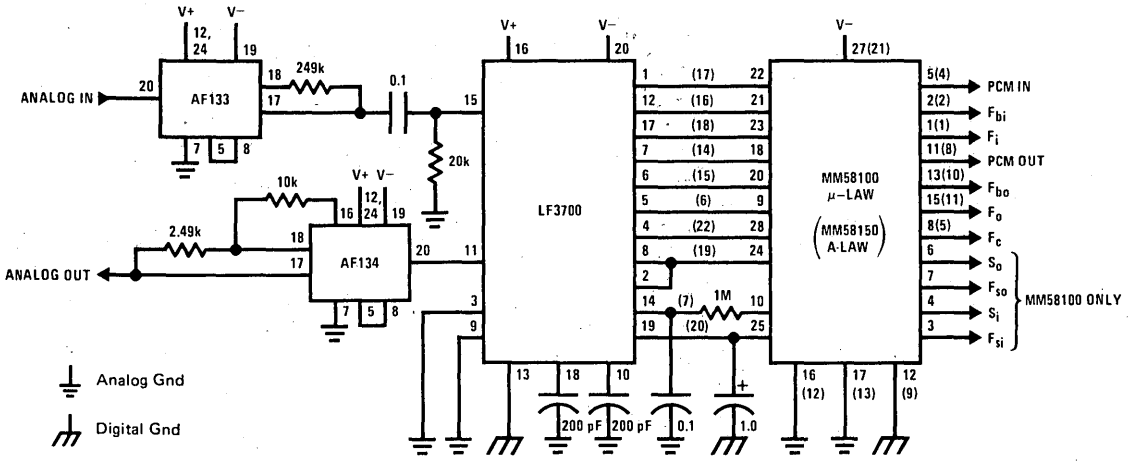
Several applications will be shown starting with 3 simple controller circuits for testing the TP3000 CODECs and finishing with a sophisticated telephone line card for 8 subscribers. While telephone applications are heavily stressed, any voice frequency signal acquisition system can be adapted from the information given here. But, before covering the various applications of the TP3000 CODEC, let's examine a typical system arrangement, *Figure 6*.

The analog input signal is band-limited by the low pass filter AF133 before it is AC coupled to the analog input of the linear CODEC chip. Within the CODEC, the signal is time sampled, held, and converted to a serial PCM bit stream that is available on the PCM OUT pin of the digital CODEC chip. Simultaneously, a serial PCM bit stream can be clocked into the PCM IN pin where it will be converted to an analog voltage, sampled and held. This decoded analog signal is then filtered by low pass filter AF134 and becomes the recovered analog output signal.

For all of the applications covered in this note, the typical system arrangement is required for each CODEC in the application.

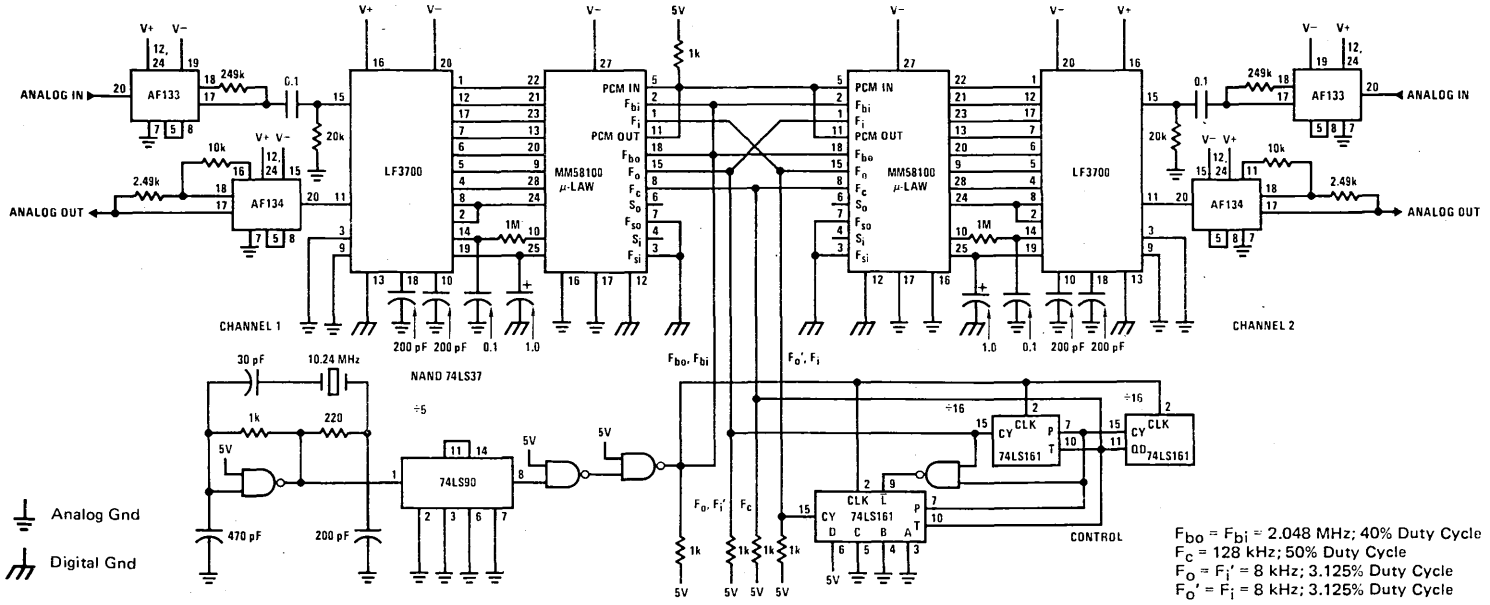
Test Controllers

Figure 7 shows the complete schematic for a two CODEC test controller. The control circuitry derives a 2.048 MHz PCM clock, a 128 kHz master clock (F_C) and two PCM word clocks. The PCM word clocks (F_o/F_i' and F_o'/F_i) are each high for only 8 of 256 clock cycles of the PCM bit clock. These two word clocks are, however, 180 degrees out of phase with each other so as to demonstrate the principle of time slot switching. Although not shown on the schematic, the logic power supply is +5V while CODECs and active filters are powered from ±12V. All supplies should be adequately bypassed.



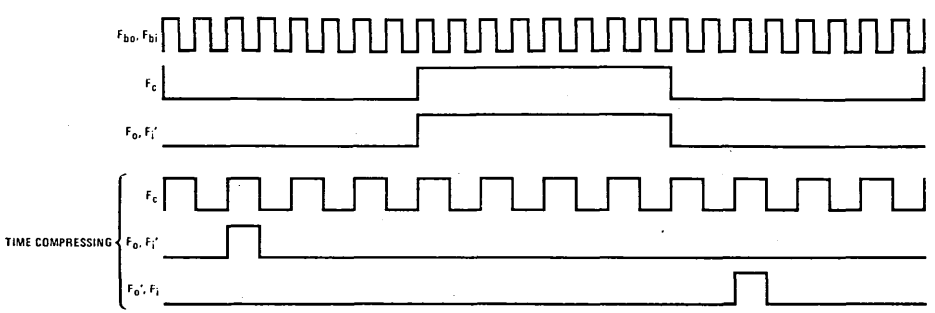
Note: All resistances in Ω and capacitances in μF unless otherwise noted.

FIGURE 6. Typical System Arrangement



Schematic Diagram

Note: All resistances in Ω and capacitances in μF unless otherwise noted.



Timing Diagram

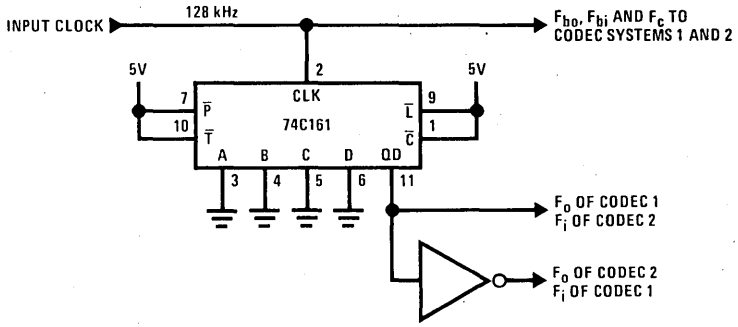
FIGURE 7. CODEC Test Controller(μ or A-Law — 2.048 MHz Clock)

Figure 8 utilizes the PCM bit clock flexibility of the TP3000 to greatly simplify the control of two CODECs. A single 4-stage CMOS counter (74C161) uses the 128 kHz master clock and PCM bit clock to derive the 8 kHz PCM word clocks. In operation, the first CODEC system will transmit to the second for 8 cycles of the 128 kHz, then the second CODEC transmits to the first for the next 8 cycles of the 128 kHz. The simplicity of this test controller will be exploited later for a full duplex system application.

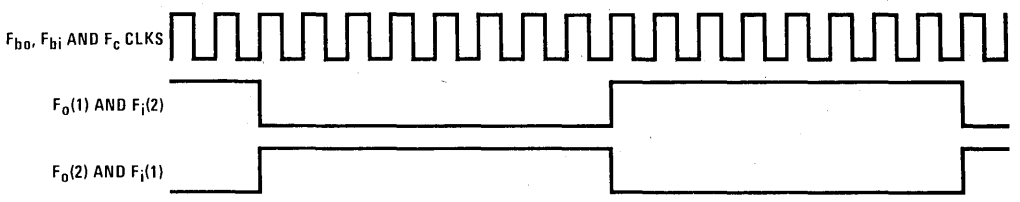
The TP3001 CODEC system has as a necessary feature the ability to "rob" the LSB of a PCM word for the purpose of transmitting digital data information. The Bell System format for this operation is to rob this bit for 1 frame of every 6 frames. During this signaling frame, PCM data is encoded and decoded in a 7-bit format. To further expand the digital data base, alternate signaling frames are used to transmit either an A signal bit per channel or a B signal bit per channel. In this way, not only does a channel carry voice information, but also 4 states of digital information. The TP3002 system does not include this auxiliary operating mode because A-law systems reserve 2 channels out of 32 per frame for digital data information.

The controller of *Figure 8* has been expanded in *Figure 9* to include a divide-by-12 counter (74LS92). This counter, plus additional logic and latches will determine signaling frames and appropriately insert or extract the LSB data during these frames.

The frame input control is normally tied to logic high. A low on this line would synchronously cause a controller reset. This line can be used to synchronize multiple controller circuits.

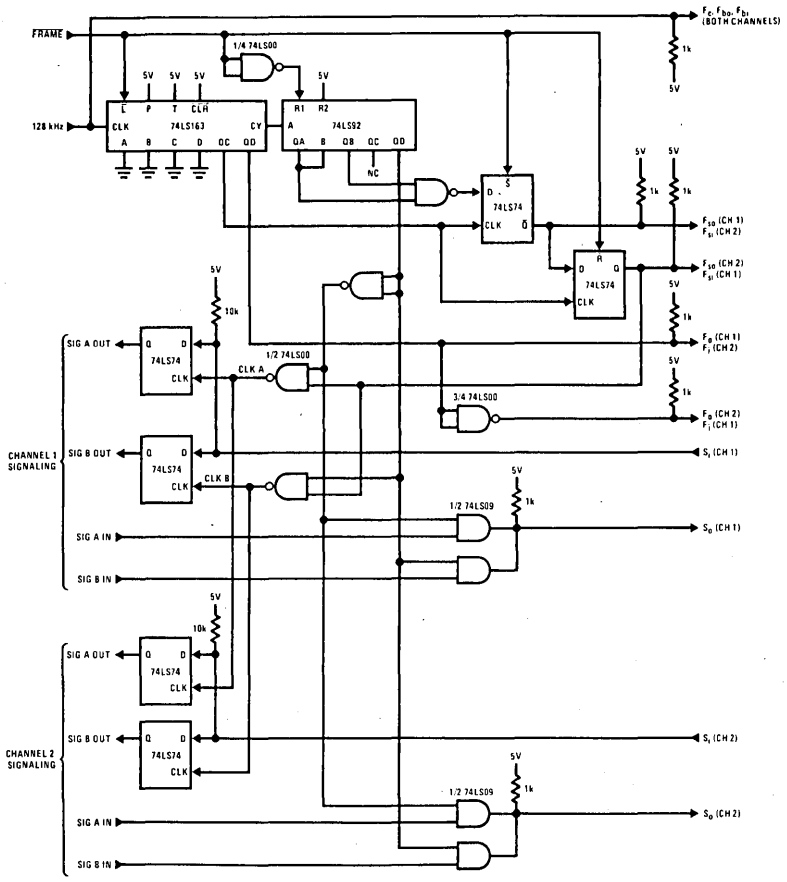


Schematic Diagram

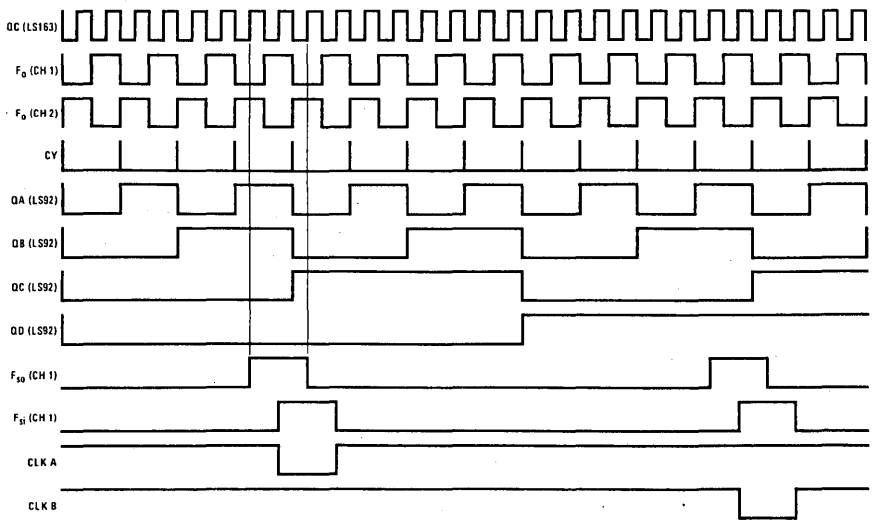


Timing Diagram

FIGURE 8. Single Channel – Full Duplex Test Controller (128 kHz)



Schematic Diagram



Timing Diagram

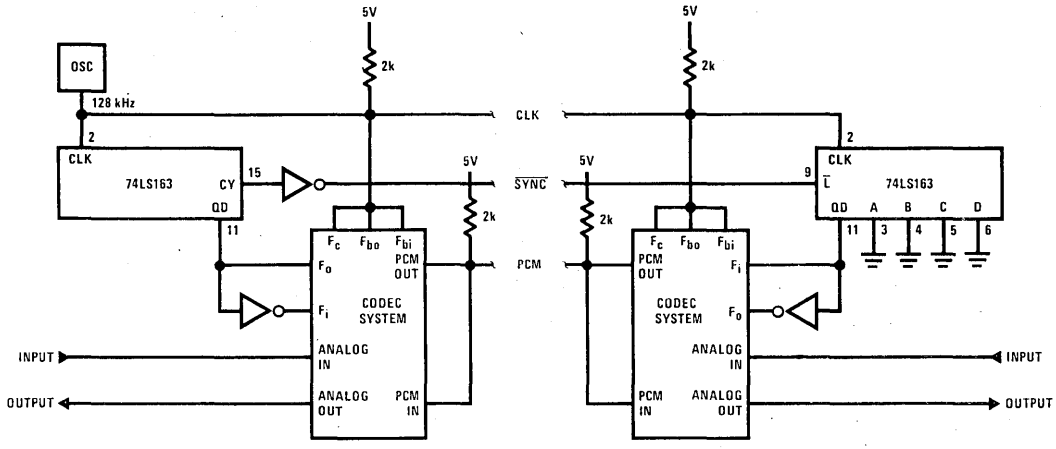
FIGURE 9. TP3001 CODEC Test Controller for μ-Law CODECs with Signaling (128 kHz Clock)

Transmission Applications

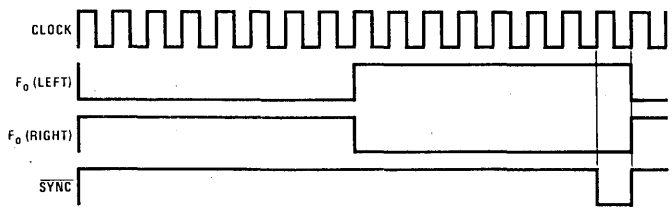
In *Figure 10*, two independent CODEC systems communicate to each other with only three interconnection signals. PCM data is clocked at 128 kHz with the CODECs taking alternating turns at transmitting and receiving PCM data. Sync and clock signals are self-explanatory.

Although not shown in *Figure 10*, some additional circuitry could be added to reduce the interconnect wiring. For instance, the clock and sync signal could be combined by using phase or voltage level modulation. Likewise, PCM information plus the clock and sync could be encoded onto a single line by using two or more modulation schemes. The end result would be a complete two way digital voice communications channel over a single twisted cable pair.

While the circuit of *Figure 10* will control either the TP3001 or TP3002 based system, *Figure 11a* is a control circuit which utilizes the signal frame capability of the TP3001. During 1 frame out of every 6, the PCM data transmitted between the two CODEC systems will be 7-bit PCM format with the LSB carrying signal A or B data. A sync signal occurs every 12 frames, with A signaling information being transmitted from CODEC system 1 four frames after sync and B information ten frames after sync. Signaling frames for CODEC system 2 are five and eleven frames after sync for A and B signaling respectively *(Figure 11b)*. The A/B signal inputs for system 1 controls the A/B outputs of system 2 and vice versa. The interconnection requirements, like *Figure 10*, can be reduced to a single wire pair with the inclusion of an appropriate modem circuit.

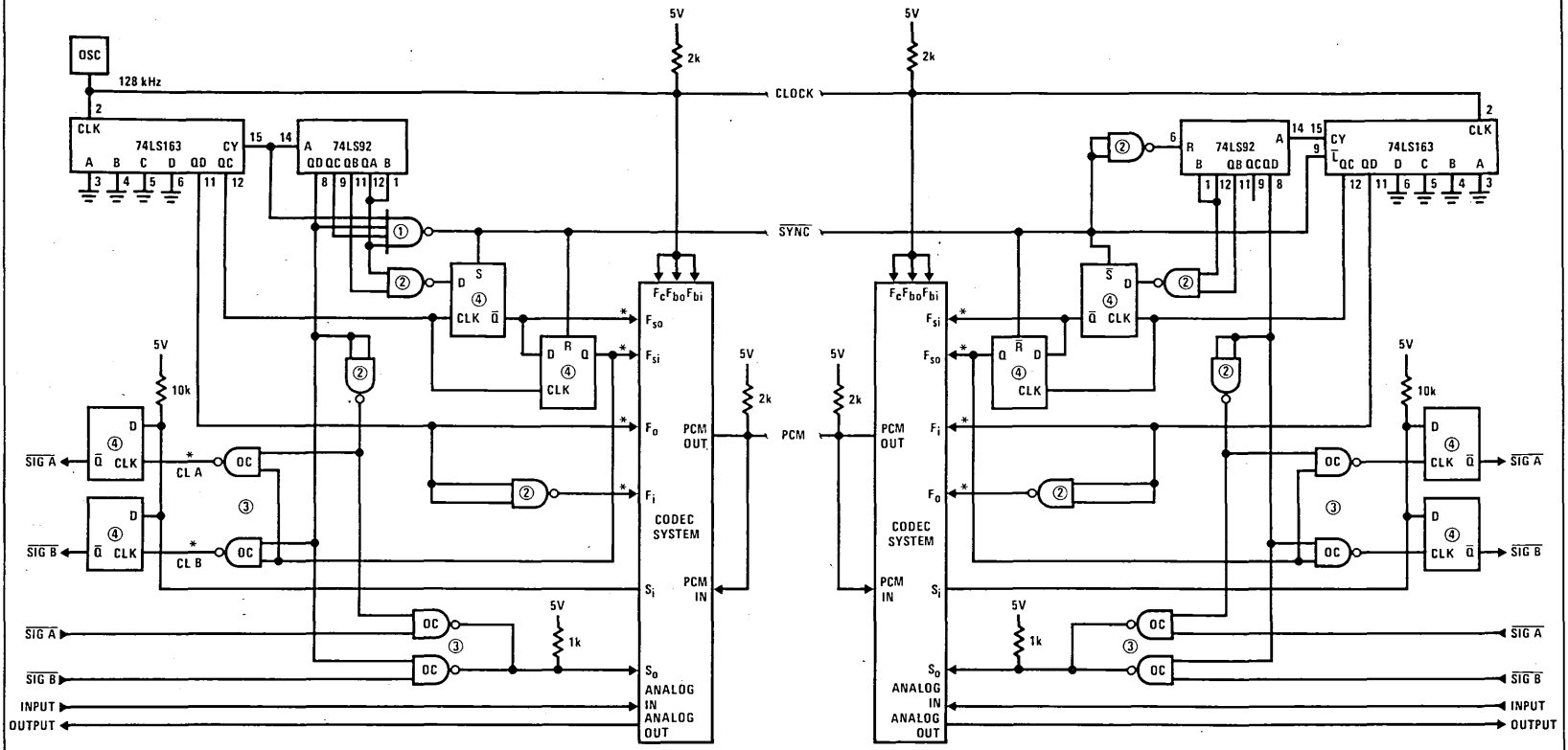


Schematic Diagram



Timing Diagram

FIGURE 10. Full Duplex Single Channel CODEC System for μ or A-Law



Note ① Dual 4 Input NAND: 74LS20
Note ② Quad 2 Input NAND: 74LS00
Note ③ Quad 2 Input NAND O.C.: 74LS03
Note ④ Dual D Latch: 74LS74
*1kΩ pull-ups to 5V required.

FIGURE 11a. TP3001 Full Duplex Single Channel CODEC System for μ-Law (with Signaling)

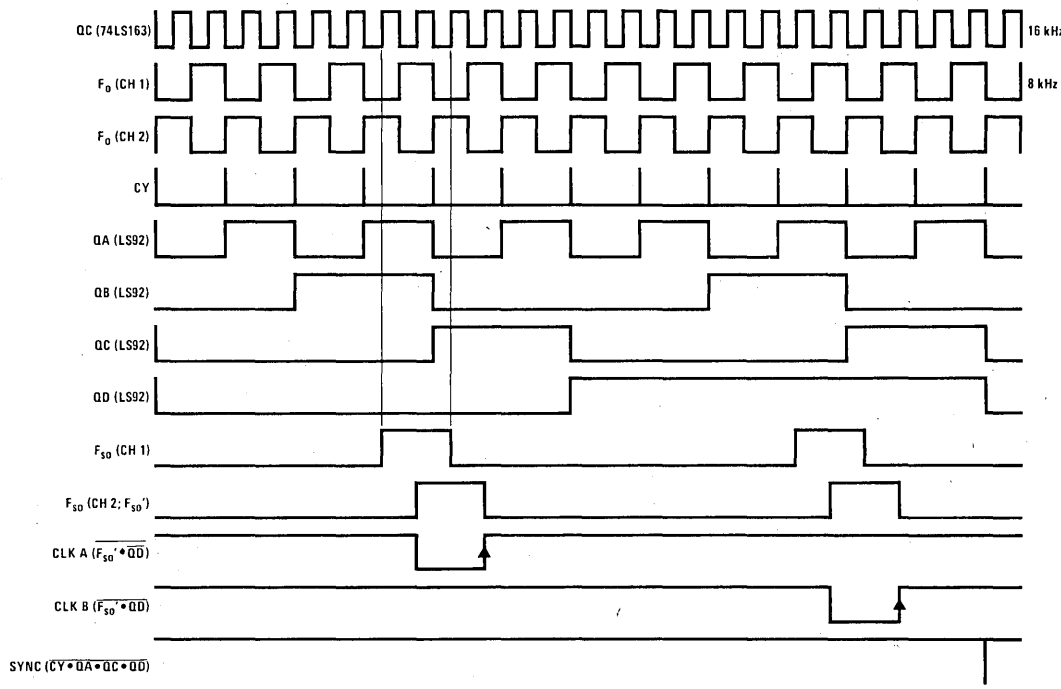


FIGURE 11b. Timing Diagram for Duplex TP3001 Controller

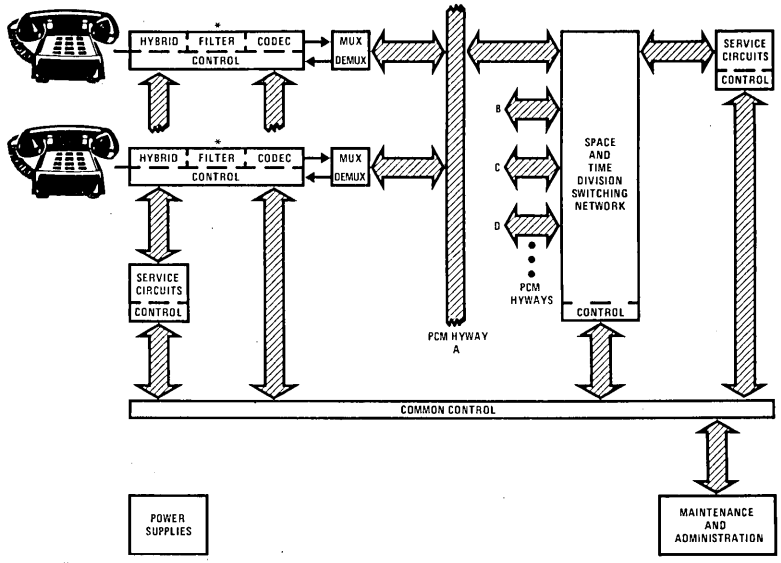
Switching Applications

As stated in the beginning of this application note, a primary application of the TP3000 PCM CODEC is the telephone line interface circuit of a digital switching network. *Figure 12a* is a block diagram of a non-toll switching network with a more detailed diagram of the actual line interface circuit shown in *Figure 12b*. Each telephone line is connected to the switching network via an interface port circuit that consists of the transmission hybrid, active filters, CODEC and control. This circuit is the system to telephone set interface which allows the completely digital switching network to control and process the various power, voice and signaling signals that are required to operate a telephone set. In a typical switching system a single circuit card would contain 4 identical line interface circuits with a single board controller. Examples of this line card arrangement will follow.

Basic to the understanding of time division switching is the concept of line concentration and time slot assignment to effect the switching of digital message signals in a time domain. For example, consider the arrangement of *Figure 12a*. Assume PCM highway A is a single bus hyway (as opposed to the special case dual bus hyway) and that 24 8-bit PCM words can be transmitted over this bus in one 125 μs frame. Also assume that 96 TP3000 CODECs operate from this bus. Because a conversation over any telephone line that is served from this PCM hyway will require two time slots for the data exchange, a transmit and receive time slot, the 24 slot bus can, at most, handle 12 completed switching paths. For 12 conversations between parties that are all served from hyway A, 24 lines of the total 96 would have obtained the requested service. All TDM switching in this case is contained to the first time switch level or PCM hyway A. If, however, the 12 conversations were between parties of PCM hyway A and other PCM hyways, then only 12 of the total 96 lines of hyway A would have obtained the desired service. The concentration of the total number of lines to the number of lines served, in this example, ranges from 8:1 down to 4:1.

Time division switching, as handled at the first switching level (hyway A), can be explained by considering a conversation between two parties served by hyway A. The system controllers may assign the call originator time slots 1 and 2 for the transmit and receive connections respectively. The space and time division switching network will transmit dial tone to this party by transmitting 8-bit samples of digital dial tone onto hyway A during time slot 2. Common control equipment, then, will collect dialed number information and process the information so as to ring the line of the called party. Of course, the common control may be required to transmit other call progress tones (busy tone, reorder, etc.) from the service circuits to the call originator via the space and time division switching network but, for this example, let's assume the call is completed. The called party, being served from PCM hyway A, will receive time slot assignments 2 and 1 for the transmit and receive connections. This is the opposite assignment made to the call originator. The result is PCM data being transmitted from originating to receiving party during time slot 1 and the reverse during time slot 2. A complete conversation path has been established.

This brief explanation of a very complex system is, at most, cursory. Concepts like time slot interchange, conferencing, digital gain control, etc. are beyond the scope of this application note. Hopefully, the concepts presented here will help the reader to reach an appreciation for the details of the following applications.



* Detailed schematic of the Hybrid, Filter, CODEC, Control block is shown in *Figure 12b*.

FIGURE 12a. Typical TDM Non-Toll Switching Network Block Diagram

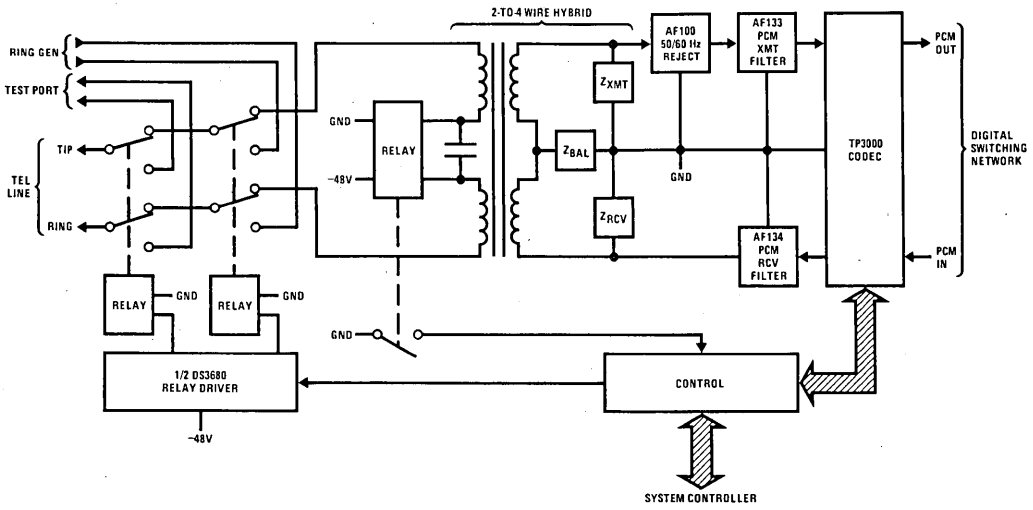


FIGURE 12b. Typical Telephone Line Interface Circuit for a Digital Central Office

Digital Line Cards

Figure 13 is a representation of a possible configuration for a switching system quad line card. The 4 CODECs controlled by the COP420 controller would interface 4 telephone subscribers to a PCM hyway of 32 time slots. The COP420 acts as the interface between the common system control and board level circuitry. This interface is shown as the MICROBUS™, but could easily be configured through a UART for serial communications. The board level control functions consist of monitoring the status of the 4 lines (hook switch inputs), assigning time slots, controlling the line test and ring relays and deactivating unused lines. Also under the direct control of the COP420 is the assignment of call originator or call receiver status. This last control is important to consider because time slots are assigned as a pair at a time. Depending on the latched state of bit D0, a particular CODEC may transmit PCM before receiving or receive before transmitting.

The operation of the quad card is based on a controller selected 74LS169 counter being synchronously preset during system frame sync (the beginning of time slot zero) to an assigned time slot number. From that point on in time it will begin to down count to zero and generate a time slot enable signal (if the power down line is low). Its associated CODEC is now enabled to communicate over the PCM hyway. The 74LS169 counter will continue to down count by wrapping around and will again enable the CODEC 32 time slots later. This operation continues until the COP420 either sends a power down command or a new time slot assignment to this channel.

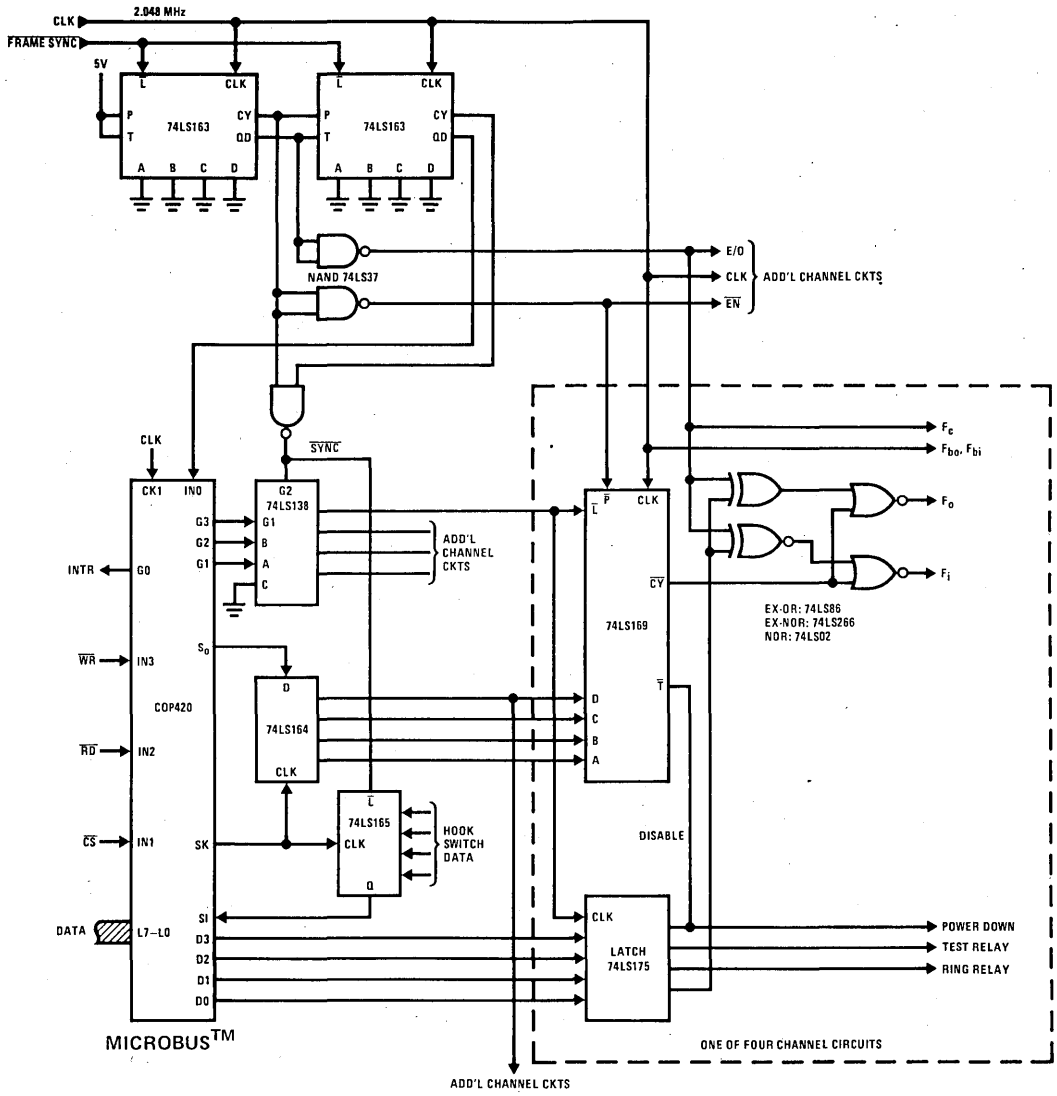


FIGURE 13. Quad Line Card – 32 Time Slot System

The octal line card of *Figure 14* is very similar to the previous example. As before, a synchronous counter, the 74LS169, is preset to a time slot number at the beginning of time slot zero. The counter then down counts to zero at which time a CODEC enable signal is generated. The significant difference here, however, is that the 74LS169 will be preset at the beginning of each frame. The individual time slot assignments have been latched on a per line basis. This scheme allows time slot counts that are not necessarily a power of 2. The 74LS169 counters, in this case, do not have to continuously wrap around to insure proper card operation. The result is a line card that can, with simple modification, operate on any time slot count from 1 to 32.

Figures 15 and *16* show the nature of the modifications required to alter the 24 time slot octal line card to 32 time slot operation *(Figure 15)*, and to provide the capability of assigning time slots on a non-paired basis *(Figure 16)*.

Note that in all of the line card examples, a minimum of interface is required between the line card and the main system. The PCM bit clock and in certain cases a 128 kHz master clock plus the frame sync signal are the only non-bus oriented signals that must be distributed. This simple board level interface coupled with the use of a flexible yet standard line control element (the COP420) makes these line card examples very sensible approaches for the digital switching network line interface card.

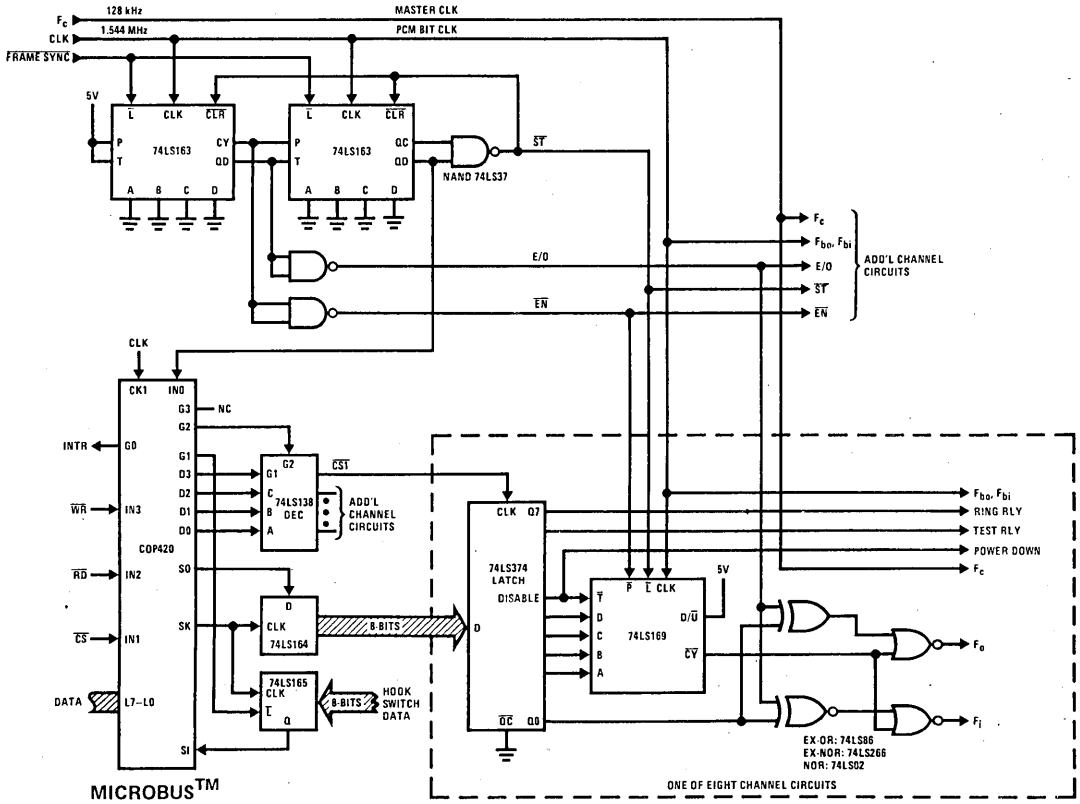


FIGURE 14. Octal Line Card – 24 Time Slot System

SUMMARY

While the intended purpose of this document is to introduce the telephony novice to the often complex structure of digital telephone networks, it is quite possible that the scope of the material covered may also be of interest to individuals with experience in the field. As for those readers with little or no interest in telephony, it is hoped that a basic understanding of the PCM CODEC in its natural environment will help the reader to develop applications in other areas.

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5. J. Cecil, E. Chow, J. Flink, J. Solomon, C.G. Svala and T. Svenson, "A Two-Chip PCM CODEC for Per-Channel Applications", *International Solid-State Circuits Conference Digest*, Feb. 1978.

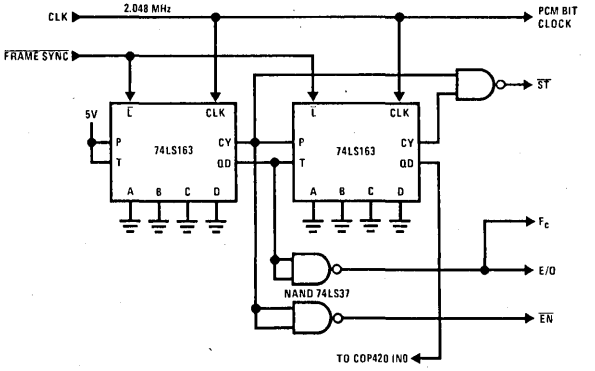
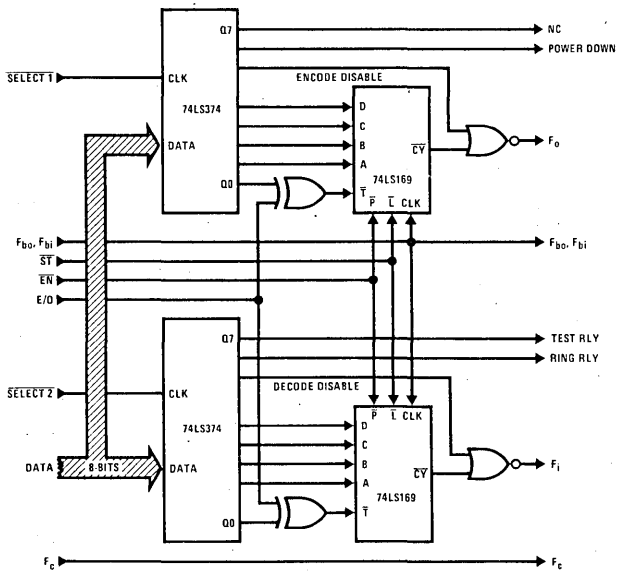


FIGURE 15. Octal Line Card Strobe Decoding Modification for a 32 Time Slot System



Note: When using this channel circuit for 8 lines, replace decoder 74LS138 with 74LS154 and use all 4 lines of port D for input code. G2 will still act as enable line.

FIGURE 16. Channel Circuit for Independent Time Slot Assignment

Gain Measurements in a CODEC System

National Semiconductor
Application Note 219
Jim Smith

INTRODUCTION

For many engineers, designers and technicians, the integrated circuit CODEC will be their first introduction to the transmission measurement and specification techniques of the telephone industry. A quick glance at the National Semiconductor TP3000 CODEC data sheet will reveal specification units that are not common in the general analog equipment world. To initiate the non-telcom designer, this application note will attempt to explain both the obvious and the obscure aspects of telecommunication transmission measurement techniques and units as they apply to the single channel CODEC system.

DEFINITIONS

The primary unit of measure in the telephone industry is the decibel. Used to denote absolute or relative voltage or power levels, ratios of voltage or power levels and even to calibrate between systems of nonmatching impedances, the decibel is a flexible measurement unit. Let's review the various forms of this unit of measure.

1. Decibel, dB: A unit of measure used to express the ratio between two power levels, P1 and P2. It is numerically defined as:

$$dB = 10 \log (P1/P2) \qquad (1)$$

By the application of Ohm's law and proper substitution, the dB can also represent the ratio between two voltage or current levels, at a constant impedance. For example, P1 can be expressed as $V1^2/Z1$ and P2 as $V2^2/Z2$. By substitution,

$$dB = 10 \log (V1^2/Z1)/(V2^2/Z2)$$

if Z1 = Z2, this reduces to,

$$dB = 10 \log V1^2/V2^2$$
$$dB = 10 \log (V1/V2)^2$$
$$dB = 20 \log V1/V2$$

2. dBr or TLP: This is the power relative to a reference point. In the United States, the term Transmission Level Point (TLP) is applied in place of dBr. 0dBr or 0TLP refers to a system point of zero relative transmission level.

3. dBm: This is the absolute power level referenced to 1 mW. It is numerically defined by equation (1) when P2 is set equal to 1 mW,

$$dBm = 10 \log \frac{P1 \text{ (in watts)}}{10^{-3}}$$

For a constant impedance of 600 Ω, the dBm is also defined as,

$$dBm = 10 \log \frac{V^2/600}{10^{-3}} = 10 \log \frac{V^2}{0.6}$$

To find the 0dBm voltage for an impedance of 600 Ω,

$$0dBm = 10 \log \frac{V^2}{0.6}$$

$$\frac{0}{10} = \log \frac{V^2}{0.6}$$

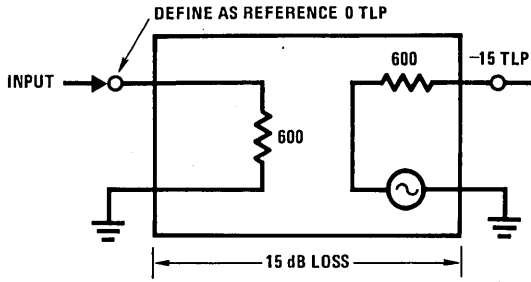
$$\log^{-1} 0 = \frac{V^2}{0.6} = 1$$

$$V^2 = 0.6$$
$$V = 0.775 \text{ Vrms}$$

4. dBm0: This is the power level (expressed in dBm) referred to a transmission level of 0TLP. In all cases, the following equation applies,

$$\text{ABS PWR (dBm)} = \text{REL PWR (dBm0)} + \text{REF PWR (dBr or TLP)} \qquad (2)$$

Figure 1 is an example of how this equation is applied.



At the input, −10 dBm = −10 dBm0
At the output, −25 dBm = −10 dBm0 + (−15 TLP)
therefore, the output level for a −10 dBm0 input is −10 dBm0 or −25 dBm.

FIGURE 1. Blackbox Gain Considerations

5. dBmp: This is the absolute power level as measured after a filter which compensates for the characteristics of the human ear. The weighting curve is shown in *Figure 2*. The psophometric filter is normally used for A-law systems only.

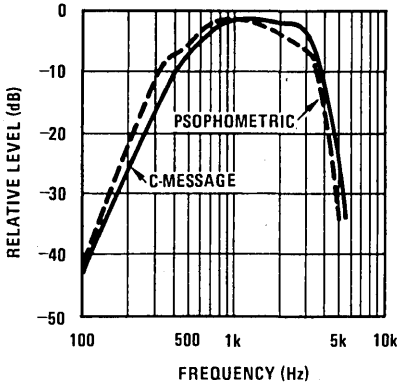


FIGURE 2. C-Message and Psophometric Filter Characteristics (from AT&T "Notes on Distance Dialing")

6. dBrnc: In the USA, the dB is often modified with the suffix rnc. The rn stands for reference noise while the c signifies that the measurement is through a C-message filter *(Figure 2)*. By definition,

   0dBrn = −90 dBm and of course, 0dBrnc = −90 dBmc.

Any of the absolute power levels can easily be expressed "referred to the 0TLP" by simply adding a 0 to the unit of measure and adjusting the numerical value accordingly.

CODEC MEASUREMENTS

Figure 3 is a block diagram of a typical CODEC set-up for making end-to-end analog measurements. In this arrangement, the CODECs are assumed to have identical encode and decode characteristics and all filters are arranged for unity passband gains. Of course, this situation is seldom attained, but gain adjustment considerations will be covered later in this note.

Before end-to-end analog measurements can be made using the *Figure 3* schematic, the relative power levels of the input and output, referenced to a zero transmission level point, must be calculated. These dBr or TLP values will then be used to calculate the dBm0 levels used for testing and measurement purposes.

As previously stated in equation (2),

ABS PWR (dBm) = REL PWR (dBm0) + REF PWR (dBr or TLP)

All that is necessary is to calculate the appropriate TLP numbers. For an example, assume the TP3000 CODEC is to be tested per *Figure 3*. The nominal 0dBm0 decoder output level for this CODEC is 2.70 Vrms which is directly related to the internal reference voltage (5.5V). The ratio of this relative voltage level to the voltage level at 0dBm (600 Ω) will yield the approximate TLP value for the TP3000 CODEC analog input or output.

$$20 \log \frac{2.70 \text{ Vrms}}{0.775 \text{ Vrms}} = 10.84 \text{ TLP} \qquad (3)$$

This means that to encode a 0dBm0 passband signal with the TP3000 CODEC, an absolute signal level of 10.84 dBm must be applied to the unity gain transmit filter's input,

REL PWR (0dBm0) + 10.85 TLP = ABS PWR (10.84 dBm)

Also, the output of the TP3000 decoder, under 0dBm0 signal conditions, will appear as a 10.84 dBm signal at the output of the unity gain receive filter. Measurement adjustments, to compensate for this 10.84 TLP value, would be required when testing the TP3000 CODEC per the *Figure 3* set-up.

The circuit shown in *Figure 4* is basically the *Figure 3* arrangement with transmit and receive gain adjustments shown. Again the TP3000 is the assumed CODEC and all filters are set for unity passband gains. By adjusting the transmit and receive gains accordingly, the 10.84 TLP value can be cancelled so as to allow direct measurement of absolute input and output signal levels. Normal application of any CODEC system would require a configuration similar to *Figure 4*.

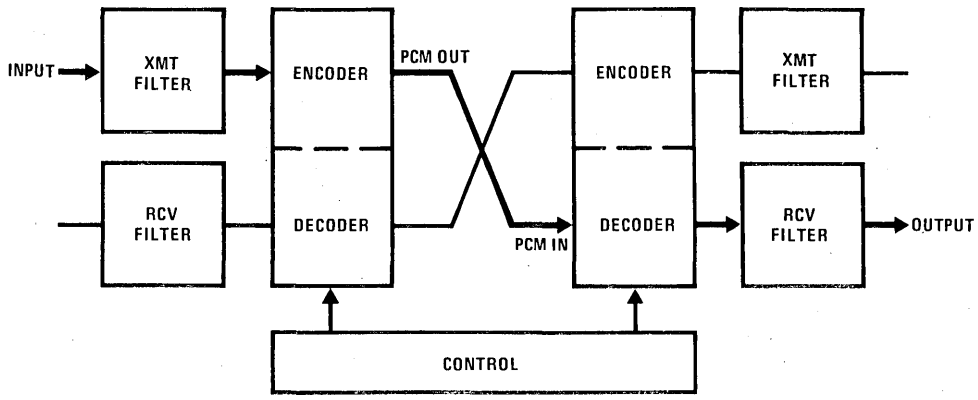


FIGURE 3. Typical Analog End-to-End Measurement

The gain adjustments for *Figure 4* can be computed as follows,

$$\text{XMT GAIN ADJUST} = \log^{-1}\frac{10.84\ \text{TLP}}{20} = 3.484 \quad (4)$$

$$\text{RCV GAIN ADJUST} = \log^{-1}\frac{(-10.84\ \text{TLP})}{20} = 0.287 \quad (5)$$

These adjustments would approximately set 0dBm equal to 0dBm0 for the TP3000 CODEC. This gain adjustment can usually be accommodated in the transmit and receive filters. The National Semiconductor AF133 filter, for instance, provides a single resistor adjustment for transmit gain while the AF134 filter provides a single resistor adjustment for receive attenuation.

THE DIGITAL MILLIWATT

While the gain calibrations detailed above are simple and straightforward, they do rely on knowing the value of the CODEC system input and output TLP. A preferred method of adjusting filter gains to achieve a particular TLP value (e.g. 0TLP) at the CODEC system's input or output is shown in *Figure 5*.

The arrangement of *Figure 5* utilizes a digital tone source to uniquely define a μ or A-law digital milliwatt. This signal source outputs a digital data stream that represents a 1 kHz sinewave of 0dBm0 signal level. When switch S1 is in position A, the receive gain is adjusted until the analog output level is at the proper level (usually 0dBm). Switching S1 to position B, and applying a known absolute signal level to the analog input line (usually 0dBm) will allow the transmit gain to be adjusted for the correct analog output level (e.g. 0dBm). By using this approach to calibrate each CODEC channel in a system, any combination of channel to channel interconnection will result in similar end-to-end gain characteristics.

A schematic of the *Figure 5* block diagram is shown in *Figure 6*. Transmit gain adjustment is controlled by the AF133 filter using resistor R1. Receive filter (AF134) attenuation adjustment is controlled by resistors R2 and R3. V_{IN} is supplied from a 0dBm, 1 kHz sinewave generator and V_{OUT} is measured via an rms voltmeter calibrated for dBm (600 Ω). A 128 kHz 5V clock source (square wave) plus a 74LS161 counter is the only control circuit needed for the CODEC and digital signal source.

The digital signal source is clocked from the CODEC PCM bit clock. One of the 4 PROM output lines (output 1) is a source for μ or A-law digital idle code; a signal that toggles between the lowest positive and negative code words at a 4 kHz rate. PROM output 2 is a source for μ or A-law digital milliwatt code as defined by the CCITT and tabulated in the TP3000 data sheet on page 3. PROM outputs 3 and 4 are unused in the basic digital signal source configuration. The user of this circuit can program these outputs for up to 128 bits of μ and A-law digital signals per output. One application of the unused PROM outputs may be the programming of a steady idle code signal (all ones for μ-law and alternating zero/one for A-law) and a 1 kHz,

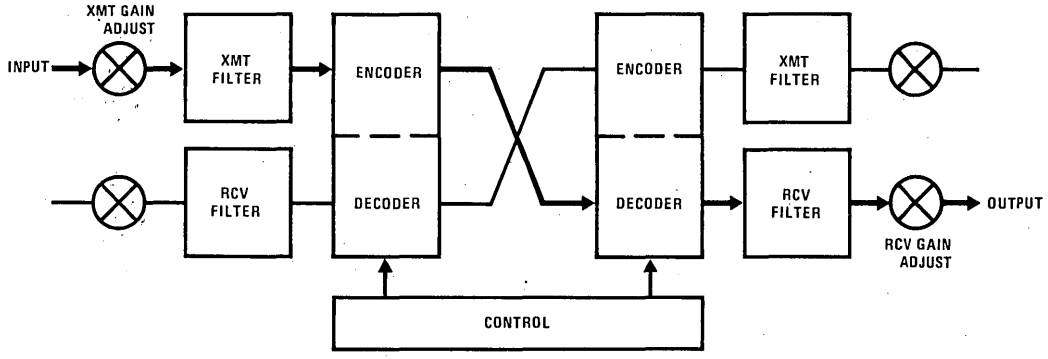


FIGURE 4. Gain Adjustments in the End-to-End Arrangement

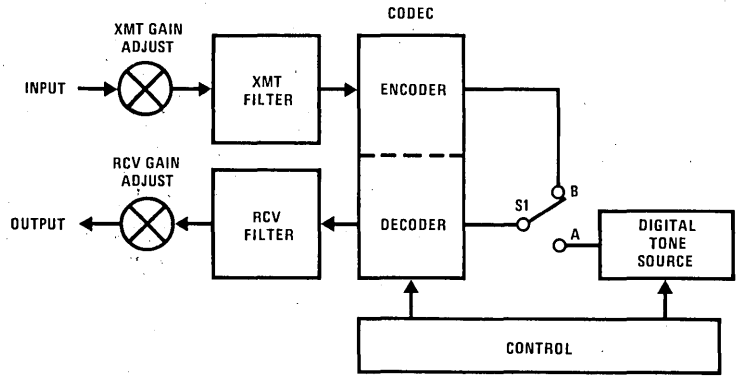
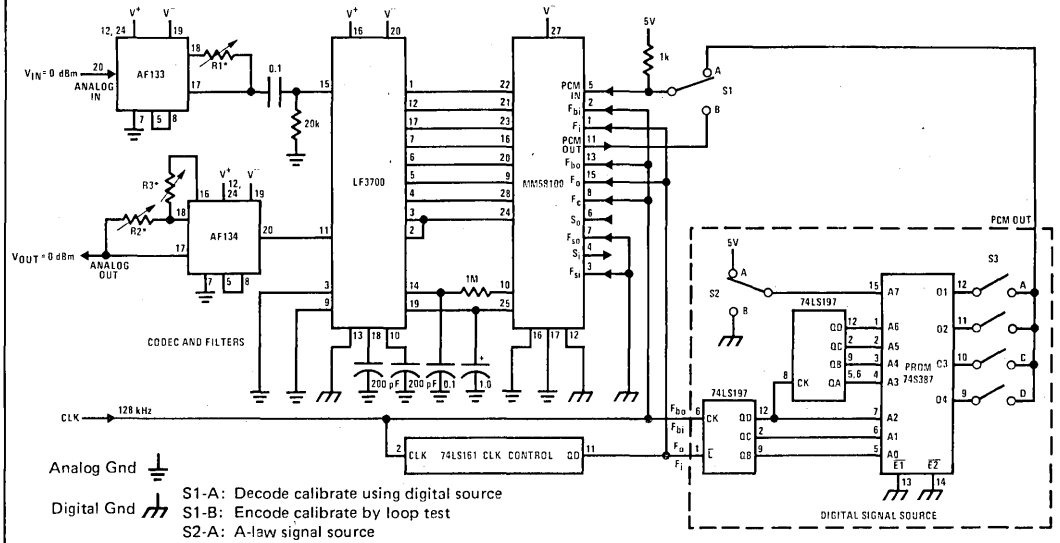


FIGURE 5. Single Channel CODEC Calibration Arrangement

−10 dBm0 signal source. Table I is a listing of the code required to program the 74S387 PROM for the basic digital signal source requirements.

CONCLUSION

What has been presented in this application note is a basic tutorial in analog gain adjustments for CODEC systems. A basic understanding of the terms and units of measure in the telephone industry plus the concept of transmission level point (TLP) should help the reader understand the techniques used to specify the various analog parameters of the NS TP3000 CODEC system. Finally, the concept of the digital milliwatt was introduced to provide a standard calibration technique for CODEC systems.



S1-A: Decode calibrate using digital source
S1-B: Encode calibrate by loop test
S2-A: A-law signal source
S2-B: μ-law signal source
S3-A: Idle code
S3-B: Digital mW
S3-C: Not used
S3-D: Not used

*Transmit gain adjust: R1 ≅ 249 kΩ
Receive gain adjust: R2/R3
where R2 ≅ 2.49 kΩ
R3 ≅ 10.0 kΩ

Note: Resistors in Ω and capacitors in μF unless noted otherwise.

FIGURE 6. Circuit Schematic for Single Channel CODEC Transmission Calibration

TABLE I. DIGITAL SIGNAL SOURCE CODING TABLE (74S387)

A7–A4 \ A3–A0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	0	1	1	3	3	3	3	1	1	1	1	1	3	1	3	3	
1	0	1	1	1	3	1	3	3	1	1	1	3	3	3	3	1	
2	2	1	1	3	3	3	3	1	3	1	1	1	3	1	3	3	
3	2	1	1	1	3	1	3	3	3	1	1	3	3	3	3	1	μ-LAW
4	0	1	1	3	3	3	3	1	1	1	1	1	3	1	3	3	SIGNALS
5	0	1	1	1	3	1	3	3	1	1	1	3	3	3	3	1	
6	2	1	1	3	3	3	3	1	3	1	1	1	3	1	3	3	
7	2	1	1	1	3	1	3	3	3	1	1	3	3	3	3	1	
8	0	1	2	3	0	3	0	1	1	1	2	1	0	1	0	3	
9	0	1	2	1	0	1	0	3	1	1	2	3	0	3	0	1	
A	2	1	2	3	0	3	0	1	3	1	2	1	0	1	0	3	
B	2	1	2	1	0	1	0	3	3	1	2	3	0	3	0	1	A-LAW
C	0	1	2	3	0	3	0	1	1	1	2	1	0	1	0	3	SIGNALS
D	0	1	2	1	0	1	0	3	1	1	2	3	0	3	0	1	
E	2	1	2	3	0	3	0	1	3	1	2	1	0	1	0	3	
F	2	1	2	1	0	1	0	3	3	1	2	3	0	3	0	1	

Note: Code inputs and addressing shown as hex numbers. 74S387 outputs O1 and O2 programmed as shown above, but O3 and O4 outputs are unused. User may program unique signals (e.g. steady state idle code, other output levels or frequencies) into the O3 and O4 outputs.

Applications of Hybrid Active Filters to Telecommunication Systems

National Semiconductor
Application Note AN-221
George H. Warren

ABSTRACT

Active filters are finding greater use in telecommunication systems because of their small size and compatibility with integrated circuits. Thick film hybrid active filters have many advantages in these applications. They are smaller than discrete circuit designs and they can be pretuned by the supplier. Other advantages include better stability due to component tracking and matching. The filters used in PCM systems and DTMF (Touch Tone®) signaling systems are well defined and are used in large quantities. This makes them attractive as thick film hybrid active filters. Transmit and receive filters in 8 kHz sample rate PCM systems such as D3 channel bank and band splitting filters for DTMF receivers are described, and their application to these systems is discussed.

INTRODUCTION

Active filters are being used in telecommunications systems because of their smaller size and compatibility with integrated circuits. The thick film hybrid active filter and other thick film circuits have many advantages in these applications. Hybrid circuits are smaller than discrete circuits and they can provide a complete accurately tuned function in a single package. Another advantage is better stability due to tracking and matching of components.

In PCM systems filters are required to limit the bandwidth of the voice or data analog signal to prevent aliasing and to reject noise and line frequency interference at the input to the transmitter. The receiver output signal must be filtered to smooth the sampler signal and to correct the amplitude for the distortion introduced by the sample and hold circuit. These filters have very stringent specifications because the system must be able to operate without introducing distortion or noise that would degrade the telephone system. In some systems a signal may be converted from analog to digital and back to analog many times. If similar equipment is used each time, signal distortion could build up and degrade a signal to a point where it would be unintelligible. Using thick film hybrid technology and active laser trimming, filters can be built which meet all these requirements.

In recent years digital integrated circuits have become available to receive DTMF signals. These receivers require that the input signal be conditioned before the receiver can decode them. The input signal must be filtered to remove the dial tone signal, if present, and then split into two bands – a high band passing signal between 1209 and 1477 or 1633 Hz and a low band passing signal between 697 and 941 Hz. A valid input signal contains one and only one signal in the high and low bands which are present simultaneously. For the receiver to properly decode the signal extraneous signals must be filtered out and the two valid tones must be separated and coupled to the receiver separately. In addition, the two tones usually are gain adjusted to eliminate twist (difference in tone amplitude). They are also limited to provide a logic level signal to the input of the receiver detector.

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PCM FILTERS

PCM systems are used to digitize analog signals for low noise transmission and reception. In telephone applications 24 to 32 PCM signals are multiplexed together to form a signaling channel and are then transmitted as a single signal. *Figure 1* is the block diagram of the analog-to-digital and digital-to-analog circuit used in telephone PCM systems. The filter in the transmit channel is required to prevent aliasing. Aliasing is the error caused by frequencies greater than one-half the sampling frequency being sampled in the CODEC. These frequencies appear at the output of the receiver as erroneous signals. A signal at 4.1 kHz sampled at 8 kHz will appear at the output as a 3.9 kHz signal added to any signal which originally appeared at the input at 3.9 kHz. Obviously this will reduce the quality of the transmission system.

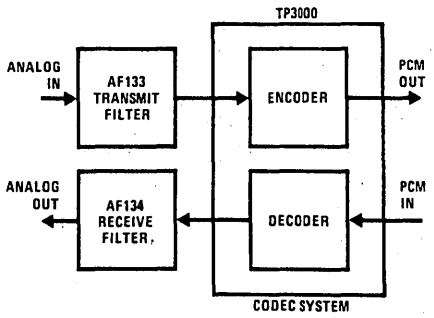


FIGURE 1. A/D-D/A Circuit Block Diagram

The requirements for a filter which will give maximum bandwidth for information with minimum signal distortion has been defined in the Western Electric specifications for the D3-channel bank. *Figure 2* is a graphical amplitude specification which meets the Western Electric and CCITT requirements for PCM systems. Filters that meet these specifications meet all amplitude requirements for high quality central office PCM transmission systems. The tight amplitude specifications are required because a signal may be converted from analog to digital to analog many times before a signal completes a telephone connection. If this were not the case the filter requirements could be relaxed.

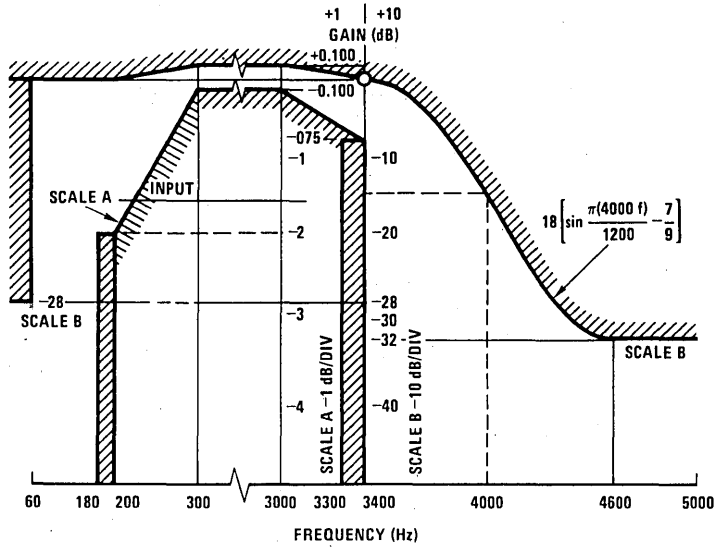


FIGURE 2. Transmit Filter Gain Relative to Gain at 1000 Hz

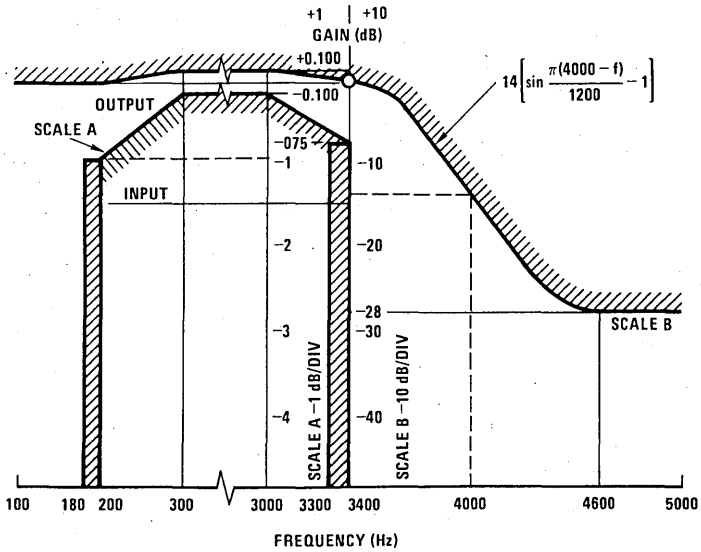


FIGURE 3. Receive Filter Gain Relative to Gain at 1000 Hz

The receive filter at the output of the decoder has two functions. One function is to attenuate all frequencies above the usable voice band and the other function is to correct the amplitude response for the distortion introduced by the output sample and hold circuit. The amplitude of the receive signal is modified by the function:

$$A = \frac{\sin(\pi \cdot f/8000)}{(\pi \cdot f/8000)}$$

The receiver response is usually specified with a sin(x)/x input signal (where $x = \pi \cdot f/8000$). *Figure 3* is a graphical amplitude specification for a PCM receive filter with sin(x)/x input that meets the Western Electric and CCITT requirements for PCM systems.

Another consideration which must be taken into account in a PCM system is the group delay distortion in the channel. The two most common ways of specifying the limits are differential delay between two frequencies and deviation from linear phase. These specifications are usually given as a system requirement which includes all circuits in the system from input to output. In a PCM channel almost all delay distortion is caused by the filters, so in practice the maximum distortion allowable per filter is slightly less than half of the total system specification. The typical specifications for either the transmit or receive filter are:

Differential Delay 1000 Hz to 2600 Hz $< 90\ \mu s$

Differential Delay 600 Hz to 2800 Hz $< 150\ \mu s$

Figure 4 is the channel specification in terms of deviation from linear phase as defined by Western Electric for the D3 channel bank.

The National Semiconductor AF133 and AF134 are a pair of filters specifically designed for PCM applications. They are 5th order elliptic low pass filters which approximate the requirements of *Figures 2, 3* and *4* for use in high quality telephone PCM systems.

The AF133 transmit filter is a low pass filter that has maximum ripple of ±0.125 dB in the band from 300 to 3000 Hz and a minimum of 32 dB attenuation above 4600 Hz. This filter typically meets all specifications of *Figure 2* above 300 Hz, but does not provide the attenuation at 60 Hz. The 60 Hz attenuation is required in two-wire systems such as those coupled to subscriber lines but not in four-wire systems used between central offices. Where 60 Hz rejection is required an additional high pass filter must be provided. A 3rd order high pass elliptic filter tuned at 240 Hz with 0.01 dB ripple and a shape factor of 3.87 will meet the requirement for 28 dB attenuation below 60 Hz.

The AF133 requires one external resistor to set the gain of the filter which can also be used to set the transmit channel gain. By varying the gain resistor from approximately 450 kΩ to 40 kΩ the gain will vary from +10 dB to −10 dB.

The AF134 receive filter is a modified low pass filter which has an amplitude response such that when a signal with sin(x)/x amplitude characteristic is inputted the output will approximate the response of *Figure 3*. The maximum ripple from 300 to 3000 Hz is ±0.125 dB and the minimum attenuation above 4600 Hz is 28 dB. The typical response meets all requirements of *Figure 3*.

The input amplitude to the filter is not usually the amplitude required to the line, but by adding an external resistor to the filter the gain can be varied over a ±20 dB range. An 11 kΩ resistor connected from output to pin 17 will decrease the gain by 20 dB and an 11 kΩ resistor from pin 16 to pin 18 will increase the gain by 20 dB.

The AF133 and AF134 filters are designed for use in systems which require tight tolerance on the quality of the signal transmission. Systems used for central office equipment and systems used to handle data as well as voice transmission require these filters. In applications where a single conversion from analog to digital to analog and only voice signals are handled, a simpler filter can be used. This type of system can be a local concentrator which combines a group of voice telephone lines for transmission over two pairs of digital lines instead of using a large number of analog lines. The AF132 Dual PCM Filter provides a transmit and receive filter in one package. Although the filters do not equal the performance of the AF133 and AF134, they provide enough filtering and amplitude correction to be used in single conversion voice-only systems. The advantages in using the AF132 are that it only requires half the power that two more complicated filters require, it requires only half the space, and it is lower in cost.

DUAL TONE MULTI-FREQUENCY FILTERS

The DTMF receivers used to detect signals from push-button telephones require at least two filters. In recent years single chip integrated circuits have been designed to detect the signaling tones and perform the logic functions required in DTMF receivers. These receivers still require input band splitting filters to separate the two input tones. Two such detectors are the Rockwell CRC8030 and the Mostek MK5102. The National Semiconductor AF121 and AF122 are bandpass filters which provide 40 dB separation between the bands. The AF121 and AF122 filters are 6th order elliptic bandpass filters. Each filter has 0 dB ± 0.5 dB gain at the center of the passband with a maximum ripple of ±2 dB peak-to-peak. The stop band rejection is greater than 40 dB. *Figure 5* shows the typical amplitude response of the two filters.

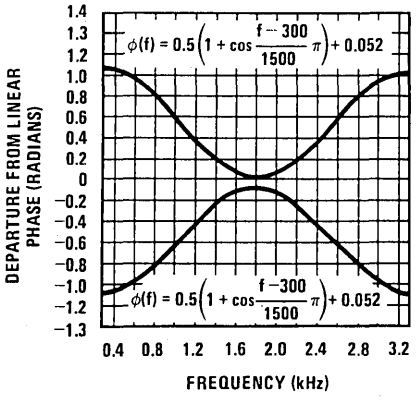


FIGURE 4. Phase Bounds

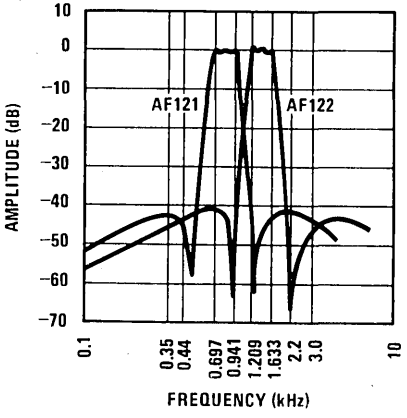


FIGURE 5. Typical Amplitude Response

Figure 6 is the block diagram of a tone receiver using the AF121 and AF122 to split the input signal into a low group and a high group signal. The signals are next passed through AGC (automatic gain control) circuits which provide amplitude correction to equalize the signal level in the two channels and to provide a known level to the limiters. The limiters have a threshold setting circuit so signals which exceed the threshold will appear at the inputs of the digital tone detector.

The input bandpass filters reject the dial tone signals, when present, and provide enough rejection to noise and extraneous signals to assure a low error rate system. The AGC amplifiers equalize the tone levels in each band, which allows the detection of signals with large twists. The AGC amplifiers also provide up to 24 dB gain to the tone signal, allowing operation over a wide range of input levels.

The National Semiconductor AF104 AGC amplifier is a linear fixed gain device with an input attenuator which is controlled by the average output amplitude. Additional circuitry provides fast recovery when a burst of signal is applied to the input. The typical recovery time of the circuit is one half cycle of the input frequency.

The limiters can be built of discrete components using a comparator such as the National Semiconductor LM339. The limiter threshold can be set by using the internal reference of the AF104, which is a +5 volt regulator. This provides a stable threshold which is independent of the system power supply. Since none of the analog circuits are dependent on the power supply for a reference and all the circuits have good common-mode rejection, a simple power supply is all that is required so long as the supply voltages remain greater than 9 volts.

CONCLUSION

Thick film hybrid circuits are being used in telecommunications systems to provide filtering and other system functions because of their small size. In PCM systems the precision required for the transmit and receive filters can be provided by actively trimmed hybrid circuits. Hybrid circuits such as active filters and AGC amplifiers can provide the signal processing required for digital tone detectives. By using active filters with good rejection to out-of-band signals, low error rate systems can be built using digital tone detectors.

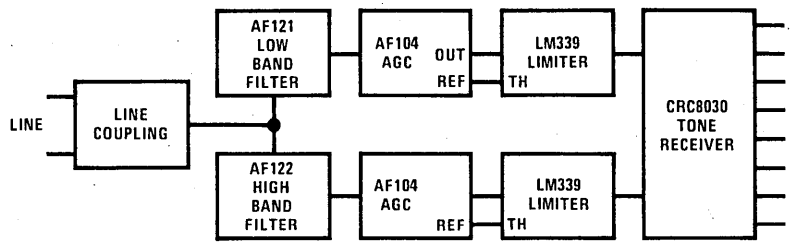


FIGURE 6. Tone Receiver Block Diagram

Applications of Wide-Band Buffer Amplifiers

National Semiconductor
Application Note 227
James Wong
Jim Sherwin

INTRODUCTION

The LH0002, LH0033 and LH0063 are wide-band, high current, unity gain buffer amplifiers. They are intended for use alone or in closed-loop combination with op amps to drive co-axial cables and capacitive or other high-current loads. Features and characteristics of these buffers are summarized in Table I. All are active trimmed for low unadjusted output offset voltage and uniform performance. Good thermal coupling between dice is achieved by hybrid thick-film construction on ceramic substrates.

Part I analyzes the AC and DC equivalent circuits.

Part II is a comprehensive guide to applications techniques and shows how to get optimum performance under a variety of circumstances.

Finally, Part III illustrates these techniques in some specific applications including drivers, sample-and-hold amplifiers and active filters.

I. CIRCUIT DESCRIPTIONS

General

The three buffer amplifiers share a similar class AB emitter-follower output stage as shown in *Figure 1*. The symmetrical class AB amplifier output provides current sourcing or sinking and relatively constant low impedance to the load during positive and negative output swing. The input stage of the LH0002 consists of a complementary bipolar emitter-follower. The LH0033 and LH0063 employ junction FETs configured as source-followers, thereby achieving several orders of magnitude improvement in DC input resistance over the LH0002. In each case, the output stage collectors are uncommitted to allow the use of current limiting resistors in series with either or both output collectors.

LH0002 Low Frequency Operation

The LH0002 circuit shown in *Figure 2* is a compound emitter-follower with small-signal current gain of approximately 40,000 (product of first and second stage betas).

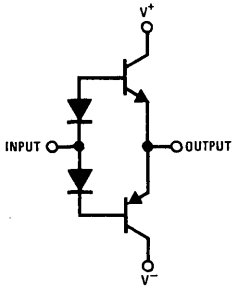


FIGURE 1. LH0002 Simplified Output Stage

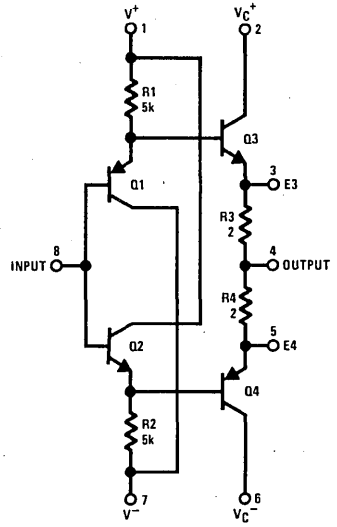


FIGURE 2. LH0002 Schematic Diagram

TABLE I. BUFFER AMPLIFIER TYPICAL CHARACTERISTICS

Parameter	Conditions	LH0002	LH0033	LH0063	Units
DC Output Current Continuous		± 100	± 100	± 250	mA
Peak Output Current		± 200	± 250	± 500	mA
Slew Rate	$R_L = 1\ k\Omega$, $R_S = 50\Omega$	200	1500	6000	V/μs
Bandwidth, 3 dB		50	100	180	MHz
Voltage Gain	$V_{IN} = 1V @ 1kHz$, $R_L = 1k$	0.97	0.98	0.98	V/V
Output Offset Voltage	$T_C = 25°C$, $R_S = 100\ k\Omega$ ($R_S = 300\Omega$ for LH0002)	± 10	± 5	± 10	mV
Input Bias Current	$T_C = 25°C$	6 μA	50 pA	100 pA	
Output Resistance		6	6	1	Ω

Operation is symmetrical, and the circuit may be analyzed by considering only the upper or the lower half of the circuit as redrawn in *Figure 3.* Input stage operating current is determined by R1 in conjunction with supply and input voltages. For $V_{IN} = 0$ and $V_S = \pm 15V$, first stage quiescent current is typically:

$$I_C = \frac{V_S - V_{BE} - V_{IN}}{R1} = \frac{15 - 0.63 - 0}{5000\Omega} = 2.88\ mA \qquad (1)$$

The normal production variation of I_C is $\pm 5\%$.

The emitter-base junctions of the first and second stages appear in series between input and output terminals, therefore the output offset voltage for $V_{IN} = 0$ is the difference in base-emitter junction voltages of a PNP and an NPN transistor. This is true for both upper and lower halves of the circuit, so there is no conflict between the two circuit halves. Output stage quiescent current will equal that of the input stage if the transistors are matched and at equal temperatures. This establishes a class AB bias in the output stage so there is no class B crossover distortion in the output. Resistors R3 and R4 inserted in the output emitter circuits minimize the effect of unmatched upper and lower circuit halves and limit the potential for thermal runaway due to input and output stage temperature differences. There is no thermal runaway if operation is confined within data sheet limits.

Maximum output current is dependent on the supply voltage, R1, Q3 current gain, and the output voltage. Maximum current is available when V_{IN} rises sufficiently above V_{OUT} that Q1 is cut off. Under this condition, the 5k resistor supplies base current to Q3, and the maximum output current is:

$$I_{O(MAX)} = \frac{V_S - V_{BE3} - I_O R3 - V_O}{R1/\beta_3}$$

$$= \frac{V_S - V_{BE3}}{R1/\beta_3 + R3 + R_L} \cong \frac{V_S - 0.7}{30 + R_L} \qquad (2)$$

where $\beta_3 \cong 200$.

If $V_S = \pm 15V$, the LH0002 can theoretically deliver about 500 mA peak into a shorted load (in practice, only 400 mA peak can be realized, for the current density in the output transistors limits the beta to about 150) or 180 mA peak into 50Ω. Current limiting may be employed for short circuit protection (see section on Current Limiting).

The voltage gain of the LH0002 is slightly less than unity and is a function of load as with any emitter-follower. It is dominated by the finite output resistance of the output stage. Hence, the gain analysis for all three buffers can utilize the hybrid π model as shown in *Figure 4.* Note that r_{e3} is the emitter dynamic resistance of Q3 and is load-current dependent. The gain expression written as a function of load resistance and input voltage is:

$$A_V \cong \frac{R_L}{R_L + R3 + r_{e3}} = \frac{R_L}{R3 + R_L\left(1 + \dfrac{0.026}{V_O + 0.003R_L}\right)}$$

$$= \left.\frac{R_L}{R3 + R_L\left(1 + \dfrac{0.026}{V_{IN}}\right)}\right|_{V_{IN} > 0.1V} \qquad (3)$$

Voltage gain could range from 0.996 for $R_L = 1\ k\Omega$ to 0.978 for $R_L = 100\Omega$ at 10V input. In contrast, the same loads would yield gains of 0.973 to 0.956, respectively, for an input of 1V because r_{e3} would be somewhat larger.

Because of the inherent current-mode feedback, initial offset error is typically 10 mV with a finite (300Ω) series input resistance. Even with unsymmetrical supplies, V_{OS} increases only an additional 3 mV per volt of supply differential. Usually this error component may be ignored as it is relatively small compared to the large-signal error predicted by equation (3) when driving heavy loads.

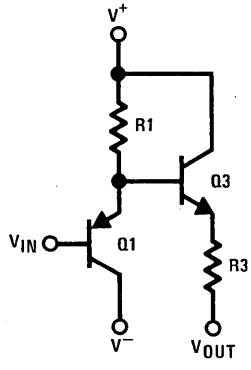
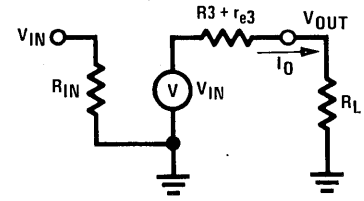


FIGURE 3. LH0002 Half Circuit



Where: $r_{e3} = 0.026/I_O$

FIGURE 4. Equivalent Model of LH0002

LH0002 High Frequency Operation

The high frequency response is limited primarily by internal circuit capacitances; most significant are the junction capacitances shown in *Figure 5*.

Since the base-emitter junction capacitances of emitter-followers see little effective junction voltage change, they may be neglected in the following first-order analysis. For the transistors used we may also assume that the transistor delay and transit time effects are overshadowed by the RC effect. We can then simplify the half-circuit to that of *Figure 6*: a single transistor emitter-follower plus an equivalent load reflected from the output stage.

Evaluation of the transfer function of equation (4) as derived from *Figure 6b* indicates that the input pole dominates for finite source resistance.

$$\frac{e_o(s)}{e_{in}(s)} = \frac{\left(\frac{R2}{R2+R_S}\right)\left(\frac{\beta_3 R_L}{\beta_3 R_L + r_{out}}\right)}{[1+s\,(R2\|R_S)\,C'_{CB1}]\,[1+s\,(r_{out}\|\beta_3 R_L)\,C_{CB3}]} \quad (4)$$

$$\cong \frac{A_V\ (\text{low frequency})}{(1+s\,R_S C_{CB1})\,(1+s\,r_{e1}\,C_{CB3})}$$

To illustrate, for $R_S = 300\Omega$, the primary pole is predicted to occur at about 60 MHz, a close correlation to the real value, while the output pole is well beyond 1 GHz. The implication of this analysis is quite significant—the fundamental bandwidth of the LH0002 is a function of the input source resistance within a reasonable range of 50Ω to 300Ω. For the case of $R_S = 50\Omega$, the resulting bandwidth is well above 100 MHz.

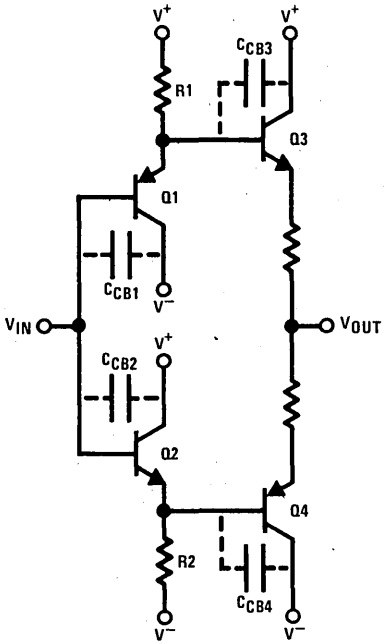


FIGURE 5. LH0002 High Frequency Circuit

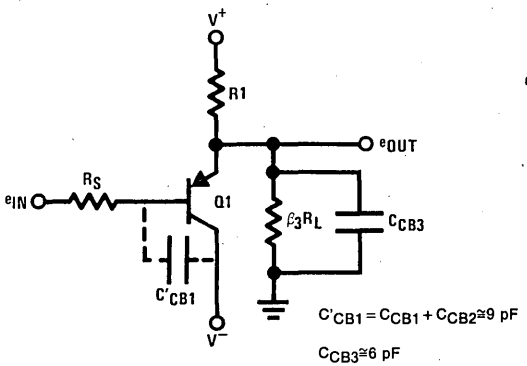


FIGURE 6a. LH0002 Simplified Mirror-Half Input Stage

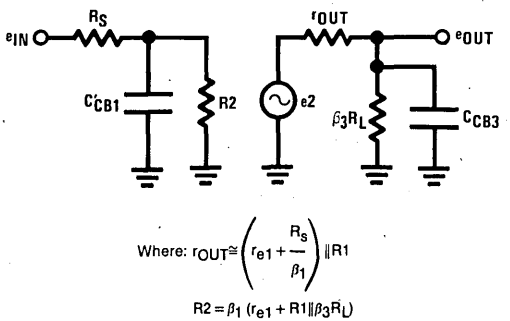


FIGURE 6b. Hybrid π Model

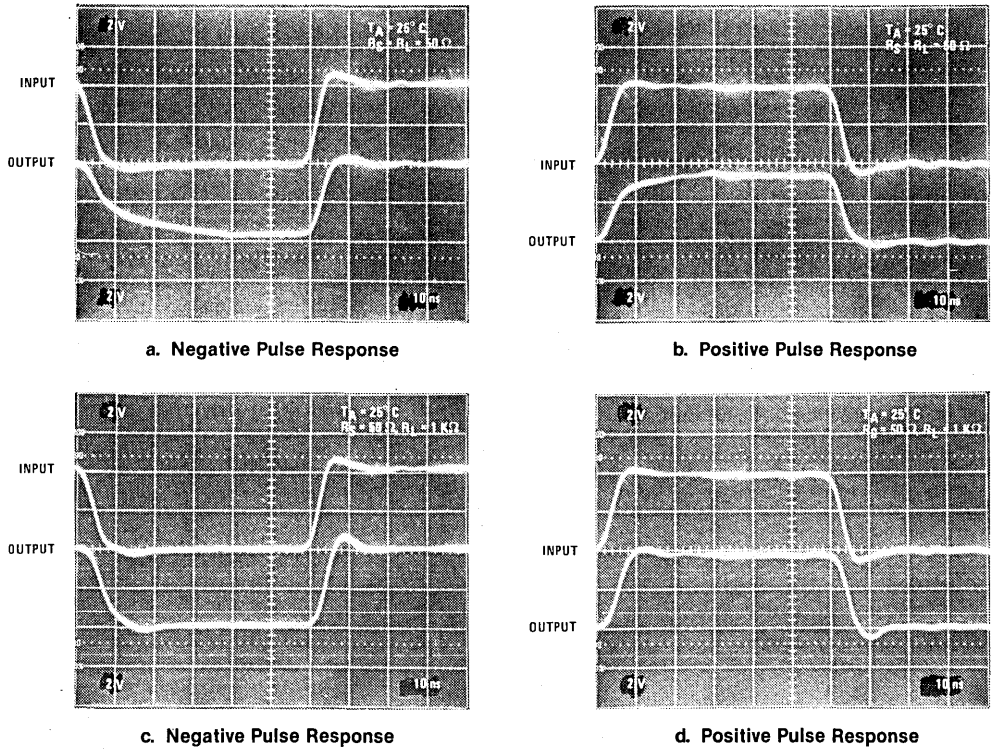


FIGURE 7. LH0002 Pulse Response

LH0002 Large Signal Pulse Response

Figure 7 shows the typical large signal pulse response of the LH0002.

LH0033 Low Frequency Operation

The LH0033 circuit can be described in simplified form, *Figure 8*, as a source-follower plus a balanced emitter-follower. The complete circuit is shown in *Figure 9*.

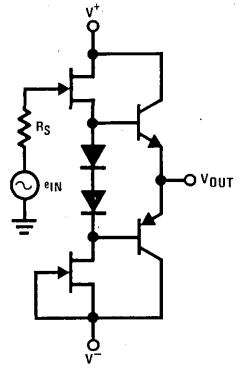


FIGURE 8. LH0033 Simplified Circuit

When Q1 and Q2 are well matched, offset voltage and drift will be low because the gate-source voltage of Q2, V_{GS2}, is set $\cong 2\ V_{BE}$, thus forcing $V_{GS1} = V_{GS2}$ due to the matching when operating at equal currents. However, as load current is drawn from the output, Q1 and Q2 will drift at slightly different rates as I_{D1} will no longer equal I_{D2} by the difference in output stage base current. Resistor R2 is trimmed to establish the drain current of current-source transistor Q2 at 10 mA, and R1 is trimmed for zero offset.

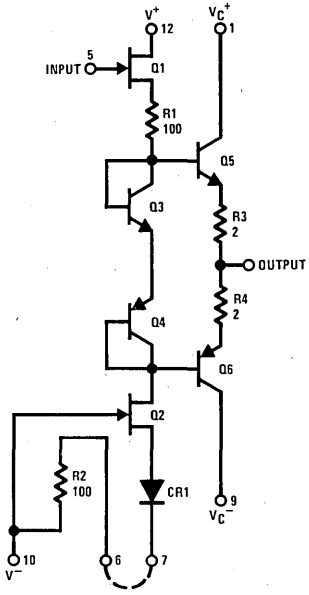


FIGURE 9. Complete LH0033 Schematic Diagram

The same current flowing through Q2 also flows through Q1 and R1, causing a gate-source voltage of approximately 1.6V. The 10 mA flowing through R1 plus Q3's V_{BE} of 0.6V causes $V_{OUT} = 0$ for $V_{IN} = 0$. The output stage current is established to be approximately equal to that of the input stage by Q3 and Q4.

Voltage gain of the LH0033 is the product of the 1st and 2nd stage gains taken independently. The analysis of each is shown in *Figure 10*. We can write the total amplifier gain expression as:

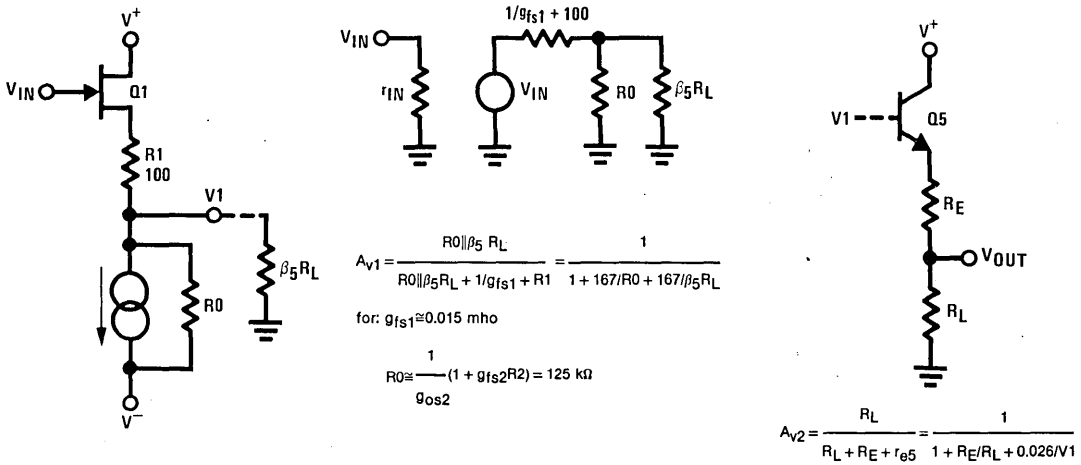
$$A_V = \frac{1}{1 + 2/R_L + 167/\beta_5 R_L + .026/V_{IN}} \qquad (5)$$

where $\beta_5 \cong 200$.

Voltage gain is predicted to be 0.995 for a 1 kΩ load, and 0.95 for a 50Ω load at 10V output.

LH0033 High Frequency Operation

Low frequency performance is modified at high frequencies by the increasing effect of transistor junction capacitance. Transistors Q3, Q4 and the output emitter-follower pair contribute only minor incremental effect on the first-order high frequency equivalent circuit so they may be omitted to yield the simplified model appearing in *Figure 11*. Modeling of transistor Q1 reduces the circuit to that of *Figure 12*.



a. Hybrid π Model of FET Source-Follower Including Effect of Output Load

b. Output Stage Gain with the Effect of Emitter Dynamic Resistance

FIGURE 10. Voltage Gain Analysis of the LH0033

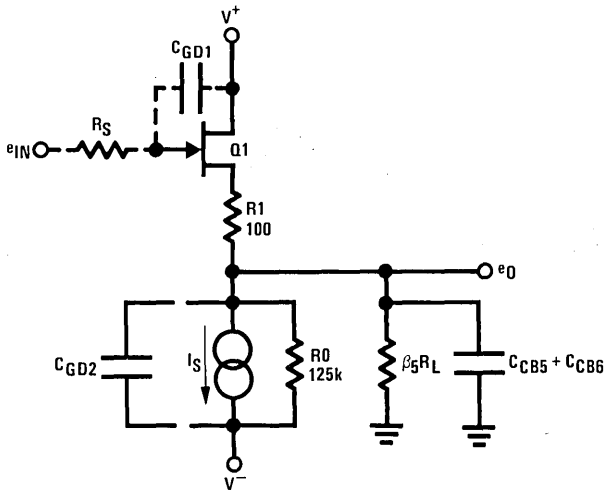


FIGURE 11. LH0033 Simplified Circuit

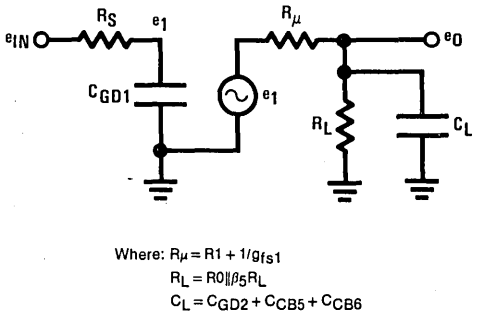


FIGURE 12. LH0033 High Frequency Circuit Model

Capacitors C_{CB5} and C_{CB6} are collector-base junction capacitances of Q5 and Q6, typically 3 pF each. C_{GD1} and C_{GD2} are the gate-drain capacitances of the FETs, typically 3.5 pF each. The frequency-dependent transfer function of the circuit is:

$$\frac{e_0(s)}{e_{in}(s)} = \frac{R_L/(R_L + R1)}{[1 + s\,R_S C_{GD1}][1 + s(R_\mu \| R_L)\,C_L]} \qquad (6)$$

Notice that unlike the LH0002, the output pole ($s = -1/R_\mu C_L$) dominates the primary frequency response roll-off occurring at about 100 MHz with an input source resistance $R_S = 50\Omega$. The user is cautioned that as R_S increases, the secondary (input) pole will begin to take effect. To illustrate, for $R_S = 300\Omega$, the secondary pole will have moved from 900 MHz at $R_S = 50\Omega$ to about 150 MHz.

LH0033 Slew Rate

The slew rate of the buffer is predicted by equation (7),

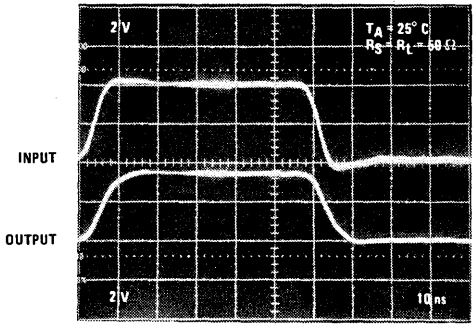
$$\frac{dv}{dt} = \frac{I}{C_L} \qquad (7)$$

where I is the input stage current available to charge the circuit capacitance C_L.

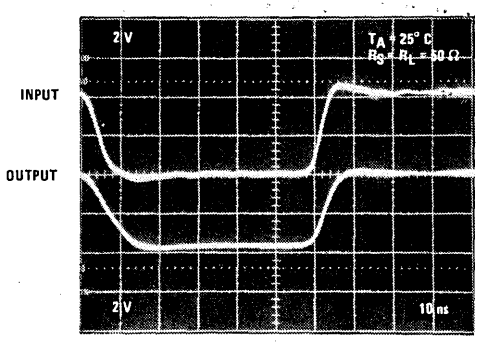
With the LH0033, the positive slew is 2-3 times greater than the negative slew. The pulse response in *Figure 13* illustrates this. The reason is that during positive slew, the peak charging current is limited by the value of R1 plus R_S when the FET gate-source junction is forward biased. This could be 30 mA- 40 mA peak, allowing a typical slew rate of 3,000 V/μs.

The LH0033 negative-going slew is limited by its input stage quiescent current of 10 mA established by the FET current source. As the input transistor tends to shut off, the circuit capacitance discharges into the current source (sink) at a rate of 10 mA. Therefore, the slew rate is computed to be:

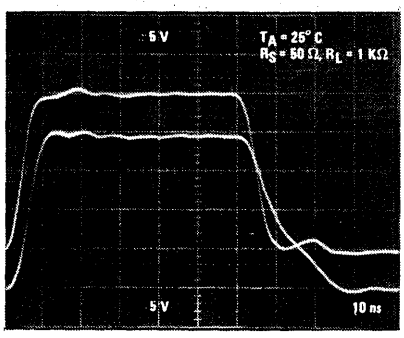
$$\frac{dv}{dt} = \frac{10\text{ mA}}{9.5\text{ pF}} = 1{,}050\text{ V}/\mu\text{s}$$



a. Positive Pulse Response



b. Negative Pulse Response



c. ±10V Pulse Response

FIGURE 13. LH0033 Large Signal Pulse Response

LH0063 Low Frequency Operation

The LH0063 exhibits several times the slew rate and bandwidth of the LH0033 due to a higher input stage operating current. The push-pull design of the first stage also allows the input FETs to be forward biased for either positive or negative-going input signals. The schematic diagram of *Figure 14* shows a pair of complementary FETs at the input stage. Transistor Q1 is biased by the current source Q4. Resistor R1 is trimmed for a 30 mA input stage operating current. Similarly, Q2 is biased to 30 mA by the current source Q3 and R2. Transistor Q5 and resistors R3 and R4 establish a $2V_{BE}$ forward diode equivalent between the Q6 and Q7 bases. These resistors are trimmed such that the output stage operates at a quiescent current of about 1 mA. Each FET gate-source voltage cancels each output transistor V_{BE} drop. Hence, the output of the buffer sits at 0V for an input 0V. The zero-offset voltage-follower action holds for any input voltage within the buffer operating voltage range.

Because of the high current drive capability, multiple output transistors are employed to limit output transistor current density. Four output degeneration resistors of 1Ω each help to prevent thermal runaway.

The DC voltage gain equation is similar to that of the LH0033. Equation (5) may be used without introducing significant error. It needs modification only because of the multiple transistor output stage. Therefore, the LH0063 voltage gain equation is approximately:

$$A_V \cong \frac{1}{1 + 0.5/R_L + 1/g_{fs1}\beta_6 R_L + 0.026/2V_{IN}} \quad (8)$$

where: $\beta_6 \cong 200$, $g_{fs1} \cong 0.010$ mho.

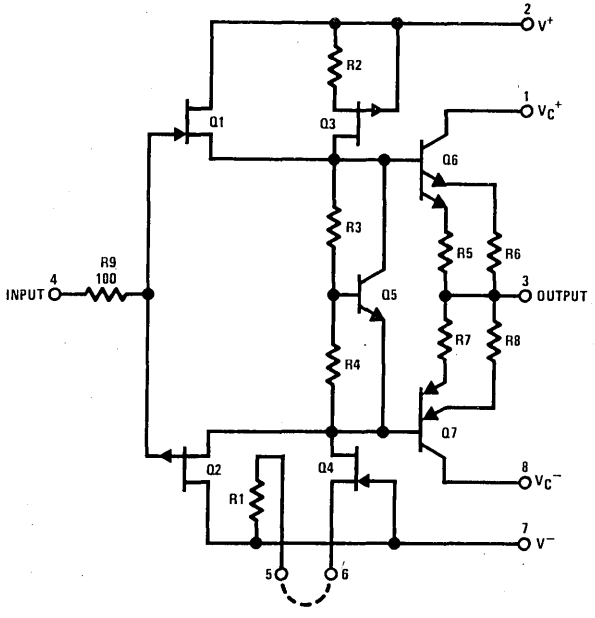


FIGURE 14. Complete LH0063 Schematic Diagram

LH0063 High Frequency Operation

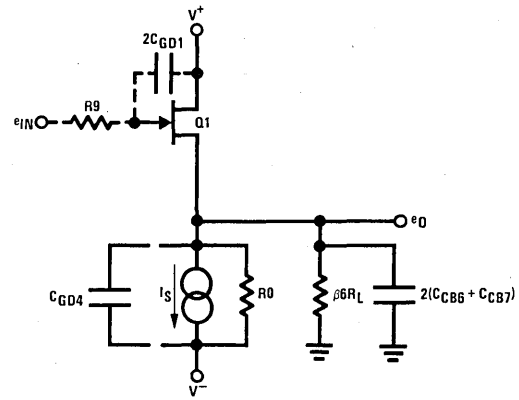
The high frequency equivalent circuit may omit the output stage, including only its load effect. The two mirrored half-circuits, consisting of a pair of complementary junction FETs and their respective current sources, can be reduced to a single half-circuit with the combined effect of both as shown in *Figure 15*.

The frequency-dependent transfer function of the LH0063 as derived from *Figure 15b* is:

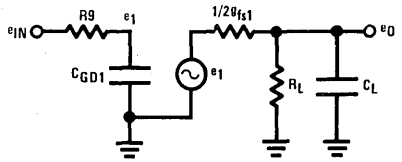
$$\frac{e_o(s)}{e_{IN}(s)} = \frac{R_L/(R_L + 1/2g_{fs1})}{[1 + s2R_9 C_{GD1}][1 + s\left(\frac{1}{2g_{fs1}} \parallel R_L\right) C_L]}$$

$$= \frac{A_v\,(\text{low freq.})}{[1 + s2R_9 C_{GD1}][1 + s\left(\frac{1}{2g_{fs1}}\right) C_L]} \quad (9)$$

Similar to the LH0033, equation (9) indicates that the device output pole ($s = -2g_{fs1}/C_L$) dominates for small value input source resistance (R9 = 100Ω). Using the parameter values given in Figure 15b, equation (9) predicts the primary pole to occur at about 190 MHz, and the secondary (input) pole at beyond 300 MHz.



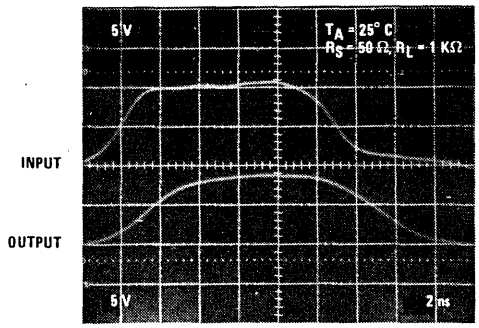
a. Lumping the Combined Effects of Two Complementary Input Stages



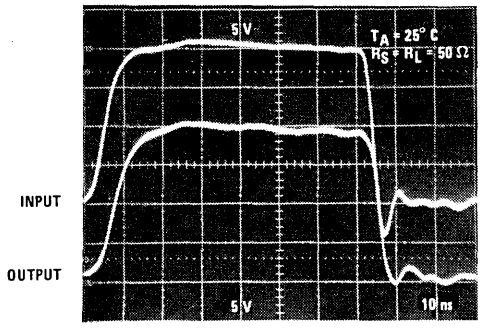
$g_{fs1} \cong 0.010$ mho, $R_L = R0 \| \beta_6 R_L$
$C_L = 2(C_{CB6} + C_{CB7}) + C_{GD4}$
$C_{CB6} \cong C_{CB7} = 3$ pF
$C_{GD1} \cong C_{GD4} = 3.5$ pF

b. Hybrid π Model of the Source Follower Substituted in the Composite Model

FIGURE 15. LH0063 Simplified High Frequency Circuit Model



a. Positive Pulse Response



b. ±10V Pulse Response

FIGURE 16. LH0063 Large Signal Pulse Response

LH0063 Large Signal Pulse Response

Figure 16 demonstrates the large signal pulse response capability of the LH0063 under different load conditions. Note the higher positive as well as negative-going slew rate achieved with the complementary FET input stage operating at higher current, a response superior to that of the LH0033.

II. APPLICATIONS INFORMATION

Circuit Layout Considerations

Circuit layout is one of the most important areas of high frequency circuit design. A sound design may yield only marginal performance when insufficient attention is given to circuit layout. This will be particularly important when the buffers are used with an op amp in a closed loop or when using very high frequency devices. The full performance capability of this family of buffers may be realized by following a few basic rules on circuit layout.

Good high frequency layout practice requires use of a ground plane wherever possible. A ground plane provides shielding (isolation) as well as a low-resistance, low-inductance circuit path to reduce undesirable high frequency coupling. In some cases, signal paths should be shielded by a surrounding ground plane to minimize stray signal pick-up; however, this shielding can cause increased stray capacitance which may be harmful at high impedance points in the circuit. Some care and judgement must be exercised in the amount and spacing of shielding ground plane areas. IC sockets should be avoided if possible because the increased inter-lead capacitance may degrade bandwidth or increase feedback capacitance in gain stages. Input and output connections should be kept short for compact physical layout and minimum coupling. When used with an op amp, layout should minimize capacitance from output to feedback point and from feedback summing junction to ground. Supply and output signal traces should be as wide as practical for these high-current devices.

Power Supply Decoupling

The positive and negative power supply terminals of the devices must be bypassed to ground with one or two 0.1 μF monolithic ceramic capacitors. They should be placed no more than 1/4 to 1/2 inch from the device pins. In difficult cases with the LH0033 and in all cases with the LH0063, a 4.7 μF solid tantalum bypass should also be added at both the plus and minus supplies. The circuit board trace between capacitor ground points should be short and of low inductance.

Compensation

The three buffer amplifiers are inherently stable in applications with resistive loads and adequate supply bypassing. However, oscillation may occur in cases where a capacitive load of 100 pF or more is present. A series input resistance of 50Ω-300Ω will prevent this oscillation by compensating the negative input-resistance seen as a result of the reflected capacitive load. All source, cathode, or emitter-followers are subject to this phenomenon which is a result of transit time through the active region of the devices.

When these buffer amplifiers are placed within the feedback loop of a high-gain op amp, the phase margin of the operational amplifier is reduced by an additional amount equal to the phase lag of the buffer. Readjustment of circuit compensation may be required to insure stability. For additional information see the section on Closed-Loop Feedback Applications.

Power Dissipation and Device Rating

Each data sheet specifies the conditions for safe operating power dissipation. These limits must be observed for both continuous and pulsed conditions. *Figure 17* shows the power dissipation limits versus temperature for each device, both with and without heat sinks. To compute total power dissipation, the standby power must be added to the load-related power.

The standby power drain is computed from the device DC operating current and its operating voltage:

$$P_{standby} = (V_S^+ - V_S^-)\, I_S \qquad (10)$$

The load-related power is the average power dissipated in the output stage. It may be estimated as the product of average current delivered to the load and the average voltage across the output stage. Because of the high-current capability of the buffers, it is essential to observe the device dissipation limits. Safe operating areas for each buffer are presented in *Figure 18*. A note of caution: these plots are valid only for 25°C ambient. Additional power derating based on the power derating curves of *Figure 17* is mandatory for operation at higher ambient temperature.

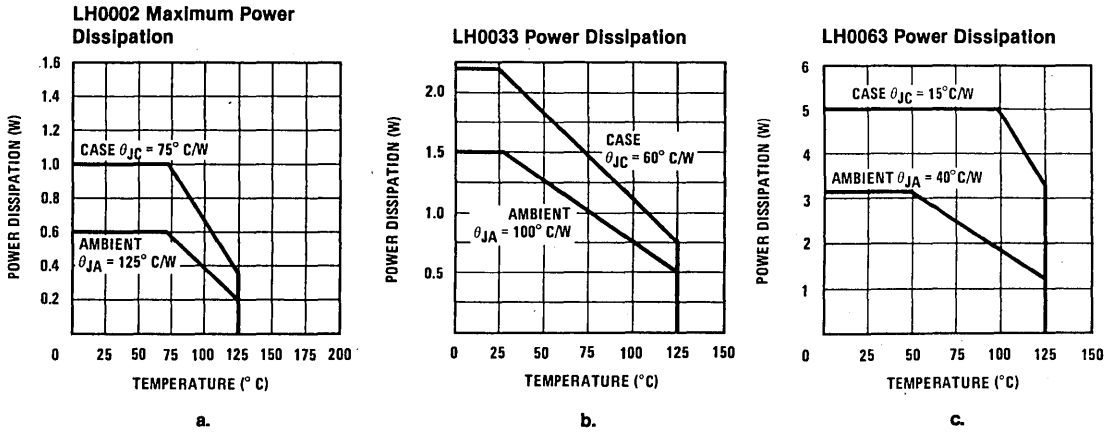


FIGURE 17. Device Power Dissipation

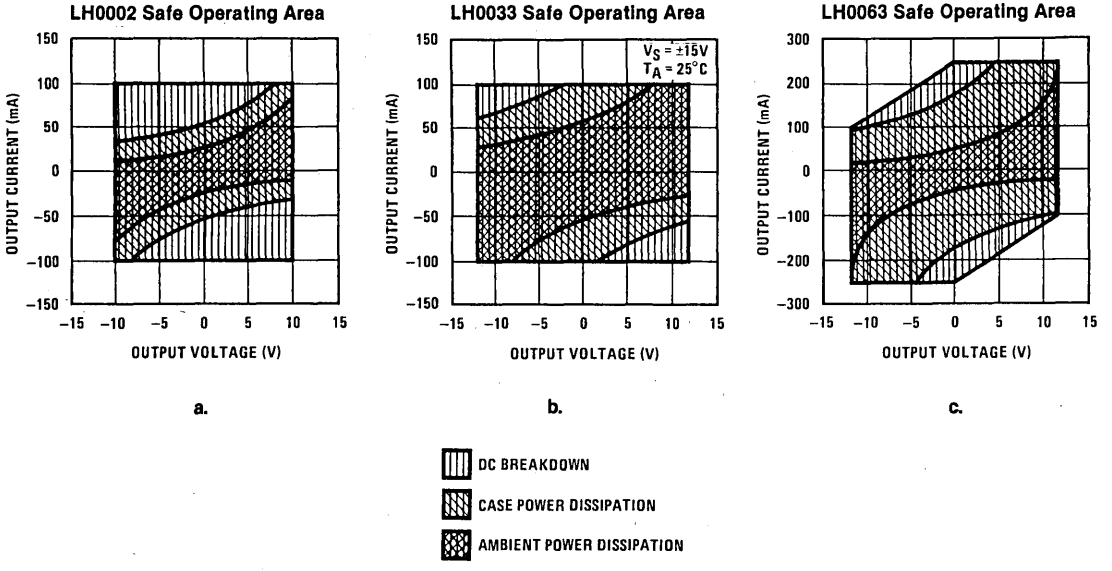


FIGURE 18. Safe Operating Areas at 25°C and V_S = ±15V

Peak Power Dissipation

An often overlooked power dissipation factor exists when driving a reactive load. Consider the LH0002 with a possible 400 mA peak current drive capability when driving 10V square pulses into 1000 pF. At the rising edge, the upper drive transistor charges the capacitor at its limiting current. The charging waveform is not linear, in fact it approaches a logarithmic curve because the resistor R1/β3 appears as the principal value of charging resistance [see equation (2)]. The instantaneous power dissipation is simply the product of V^+ and $I_{O(MAX)}$, or 6W, with occurrences at the positive and negative leading edges. Once the load capacitor is charged, the negative leading edge instantaneous peak power is somewhat greater because the power dissipated in the lower output transistor is $(V_O - V^-)\, I_O = 25 I_O$. The PNP pull-down transistor has slightly lower β, limiting peak current to less than 400 mA, therefore the peak negative edge power is just under 10W in this instance.

Figure 19 indicates the output voltage and current relationships as well as the power dissipation versus time for the pulse waveform into a capacitive load.

Obviously, the average power dissipation under peak current drive conditions is dependent upon the pulse repetition frequency, and becomes increasingly dominant as the PRF increases.

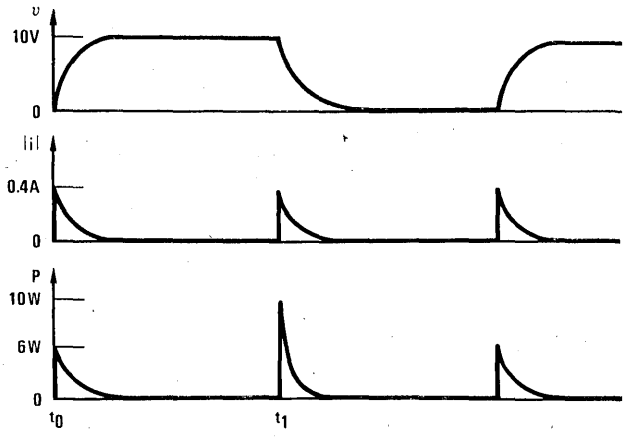
Because each of the buffer amplifiers may be operated on dissimilar supply voltages for input and output stages, device power dissipation is reduced by lowering the output stage supply voltages while retaining the input stage supplies at a higher level for best current driving capability. The limiting factor is, of course, a reduced output voltage swing.

Current Limiting

Current limiting may be provided in either of two ways: by adding series resistors at the collectors of the output stage, or by a single series resistor at the buffer output. The first method (*Figure 20*) is preferred as there is little effect on output resistance and peak current drive. However, the output voltage swing is reduced by the voltage drop across these resistors. Their value is determined as follows:

$$R_{LIM} = \frac{V^+}{I_{SC}^+}\ ,\ \frac{V^-}{I_{SC}^-} \qquad (11)$$

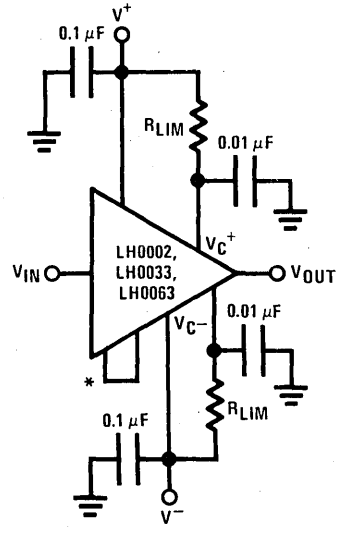
where $I_{SC} = 100$ mA for LH0002 and LH0033, and 250 mA for LH0063.



PEAK POWER

$P_{t_0} = (15V - 0V)\,(0.4A)$
$= 6\ W_{PEAK}$
$P_{t_1} = [10V - (-15V)]\,(0.4A)$
$= 10\ W_{PEAK}$

FIGURE 19. Peak Power Dissipation Into Pure Capacitive Load



*LH0033 and LH0063 only

FIGURE 20. Current Limiting using Collector Resistors

The output collectors should be bypassed with 0.01 μF capacitors in addition to the normal supply bypassing, as shown in *Figure 20*. The 0.01 μF capacitors will allow full output voltage and current on an instantaneous basis for transient pulses yet at the same time prevent output stage resonant oscillation.

Alternate active current limit techniques that retain almost the full DC output swing are shown in *Figure 21*. In these circuits, the current sources are saturated during normal operation and thus apply nearly full supply voltage to the load. Under fault conditions, the voltage decreases as determined by the overload.

For *Figure 21a*, the limit-set resistor is set for 60 mA.

$$R_{LIM} = V_{BE}/I_{SC} = 0.6V/0.06A = 10\Omega$$

In *Figure 21b*, the current limit has been set to 200 mA.

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{0.2A} = 3.0\Omega$$

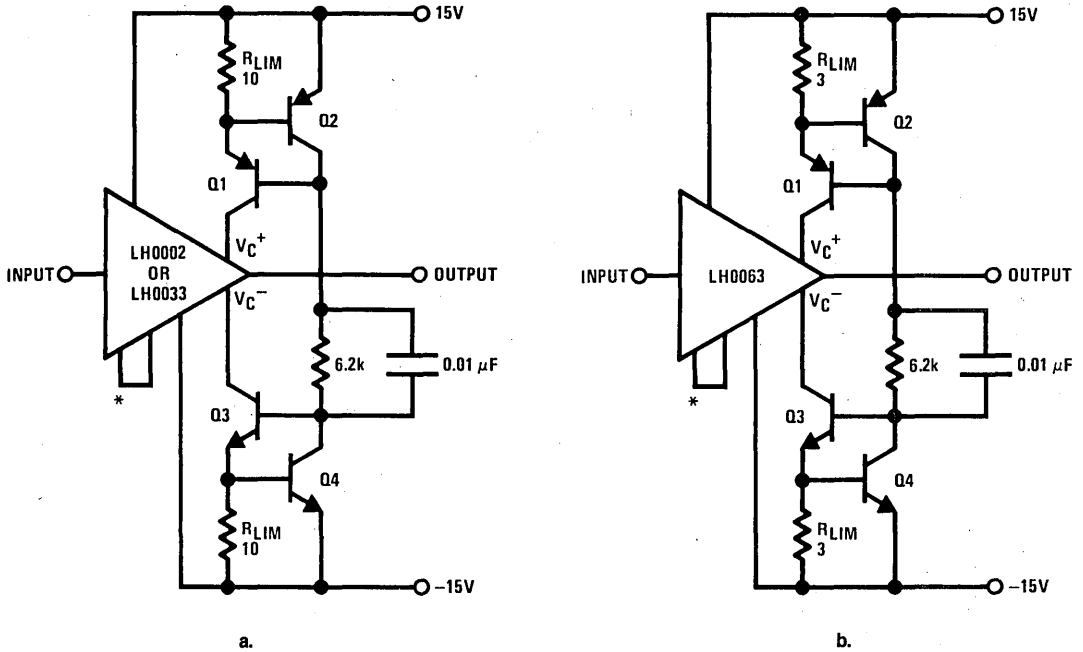
For applications where the buffers are inside the feedback loop of an op amp such as LH0032, LH0024, LH0062, or LM118, a single current limiting resistor may be placed inside the feedback loop at the buffer output as shown in *Figure 22*. Its value is also computed as $R_{LIM} = V^+/I_{SC}$.

Heat Sinking

In order to utilize the full drive capabilities of these devices, low thermal resistance heat sinks should be used. The cases of all three devices are isolated from the circuit and may be connected to system ground or to the buffer output as desired. The following list gives thermal resistance of various heat sinks available for the buffers.

TABLE II. HEAT SINKS FOR LH0033 AND LH0063

LH0033	LH0063
Thermalloy 2240A, 33 °C/W	Thermalloy 6002B-19, 6 °C/W
Wakefield 215CB, 30 °C/W	IERC LAIC3B4BC
IERC UP-TO8-48CB, 15 °C/W	IERC HP1-TO3-33CB 7 °C/W



*LH0033 and LH0063 only

FIGURE 21. Current Limiting using Current Sources

Capacitive Loads

All three devices are capable of driving relatively high capacitive loads. Because capacitive loads on emitter-followers are reflected to the input as negative resistances, it is necessary to add some series compensating positive real resistance; 50Ω-300Ω is usually sufficient. An alternative is to insert the current limiting resistor at the output as shown in *Figure 22*. This will isolate the capacitive load from the buffer.

Any of the buffers can drive twisted pair, shielded or coaxial cables, or other reactive loads. For all practical purposes, an unterminated coaxial cable presents a capacitive load to the driver. On the other hand, terminated coaxial cables appear as resistive loads, and therefore may not require the compensation for capacitive loads. Don't forget consideration of peak power dissipation when driving cable loads, since they may represent capacitive loads (see section on Peak Power Dissipation).

Offset Voltage and Adjustment

Offset voltage is measured with $V_{IN} = 0$. As V_{IN} and I_L are increased, the apparent offset voltage will change. This is due primarily to a gain which is less than unity (inherent in an emitter-follower). The effect of this is discussed in detail in the section on Circuit Description. Both the LH0033 and LH0063 have provisions for offset voltage adjustment. When not required, the OFFSET ADJUST pins of these two devices should be shorted. When adjustment is desired, they should be open-circuited, and the external adjustment is accomplished with a 200Ω variable resistor inserted between V^- and pin 7 of the LH0033 or pin 6 of the LH0063. It is good practice to insert a 20Ω resistor in series with the variable resistor to limit excessive power dissipation at the input stage when the pot is at minimum value. The offset adjustment range is typically ±400 mV.

When a buffer amplifier is used as a current booster in conjunction with an operational amplifier, as in *Figure 22*, there is usually no need for output offset adjustment, since the offset is reduced by the open-loop to closed-loop gain ratio.

The total offset of the closed-loop circuit is:

$$V_{OS(TOTAL)} = V_{IOS} \pm V_{OOS} \frac{A_{CL}}{A_{OL}} \quad (12)$$

where: V_{IOS} = input offset voltage,
V_{OOS} = buffer offset voltage.

Slew Rate

Slew rate is the rate of change of output voltage for large-signal step input changes. For resistive load, slew rate is limited by internal circuit capacitance and operating current. *Figure 23* shows the slew capabilities of the buffers under large-signal input conditions.

However, when driving capacitive load, the slew rate may be limited by available peak output current according to the following expression.

$$dv/dt = I_{pk}/C_L \quad (13)$$

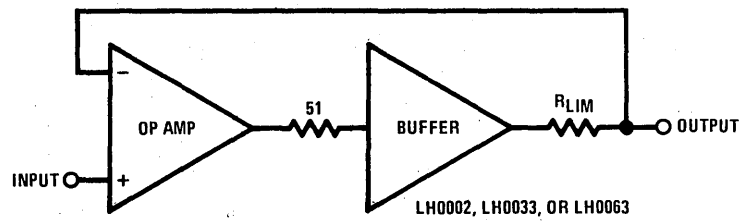
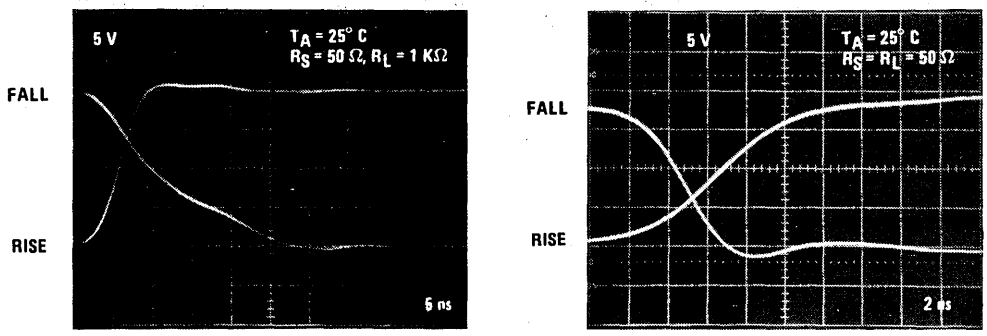


FIGURE 22. Current Limiting Inside an Amplifier/Buffer Loop



a. LH0033 Slew Response **b. LH0063 Slew Response**

FIGURE 23. Positive and Negative Slew of Each Buffer

Note that the peak current available to the load decreases as C_L charges [see equation (2)]. *Figure 24* illustrates the effect of the load capacitance on slew rate for the three buffers. Slew rate tests are specified for resistance and/or very small capacitance load, otherwise the slew rate test would be a measure of the available output current. For highest slew rate, it is obvious that stray load capacitance should be minimized.

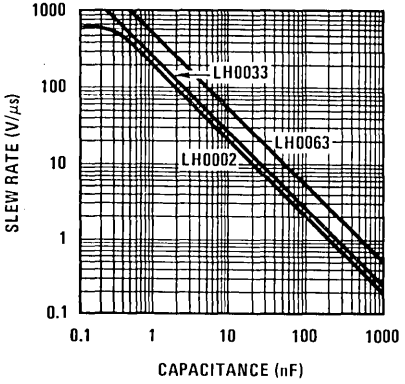


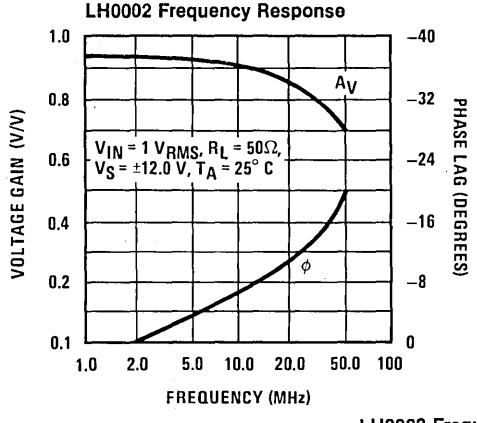
FIGURE 24. Slew Rate vs Load Capacitance

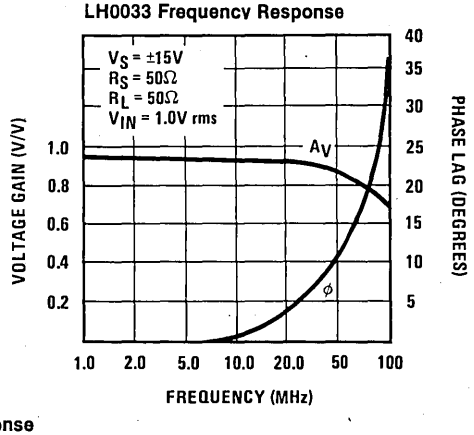
Distortion

The output stage of the three buffer amplifiers are biased at 1 mA to 10 mA to remove any possibility of crossover distortion. The LH0063 may exhibit a small amount of crossover distortion in some circumstances due to the relatively low 1 mA output stage bias. The heavy local feedback inherent in emitter-follower or source-follower operation provides a very low distortion output. The remaining distortion (<0.1%) is primarily due to the modulation effect of non-constant V_{CE} as the output voltage changes.

Closed-Loop Feedback Operation

Any of the buffer amplifiers may be used inside an op amp feedback loop. When this is done, the additional phase lag introduced by the buffer must be included in loop stability consideration. With most op amps, the bandwidth of these buffers is so great that the op amp totally controls the loop stability. However, when using very wide-band op amps such as the LH0024, LH0032, and LH0062, the small additional phase lag of the buffers should be taken into consideration. *Figure 25* presents the Bode plots of gain and phase for the three buffers. The phase margin and open loop frequency response is altered by the additional pole(s) contributed by the buffer. The buffer phase shift is algebraically summed with the op amp phase shift, and may cause a stable op amp loop to become marginally stable depending upon the relative positions of the op amp and buffer poles. In general, the buffer bandwidth should significantly exceed that of the op amp, so that the loop performance will be determined solely by the op amp.





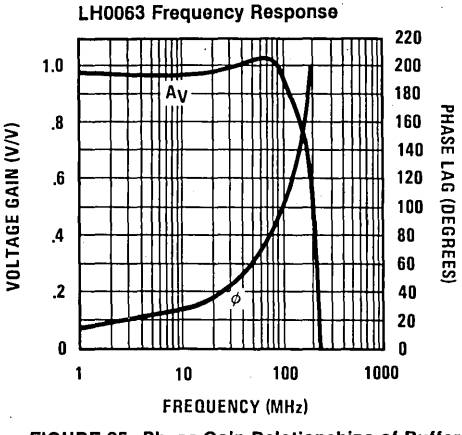
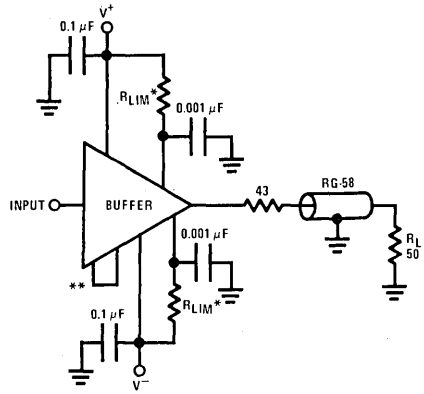


FIGURE 25. Phase-Gain Relationships of Buffers

III. APPLICATIONS CIRCUITS

Because of their high current drive capability, the LH0002, LH0033 and LH0063 buffer amplifiers are suitable for driving terminated or unterminated coaxial cables, and high current or reactive loads. Current limiting resistors should be used to protect the device from excessive peak load currents or accidental short circuit. There is no current limiting built into the devices other than that imposed by the limited beta of the output transistors. *Figure 26* shows a coaxial cable drive circuit. The 43Ω resistor matches the driving source to the cable; however, its inclusion will rarely result in visible improvement in pulse response into a terminated cable. If the 43Ω resistor is included, the output voltage to the load is about half what it would be without the near end termination.

The LH0033 and LH0063 are useful in high speed sample-and-hold or peak detector circuits because of their very high speed and low-bias-current FET input stages. The high speed peak detector circuit shown in *Figure 27* could be changed to a sample-and-hold circuit simply by removing the detector diode and the reset circuitry. For best accuracy, the circuit offset may be trimmed with the 10 kΩ offset adjustment pot shown. The circuit has a typical acquisition time of 900 ns, to 0.1% of final value for 10V input step signal, and a droop rate of 100 μV/ms. Even faster acquisition time can be achieved by reducing the hold capacitor value.



* For: LH0002, $R_{LIM} = 100\Omega$, 1W
LH0033, $R_{LIM} = 100\Omega$, 1W
LH0063, $R_{LIM} = 60\Omega$, 5W
* *Jumper for LH0033 and LH0063 only.

FIGURE 26. Coaxial Cable Drive Circuit

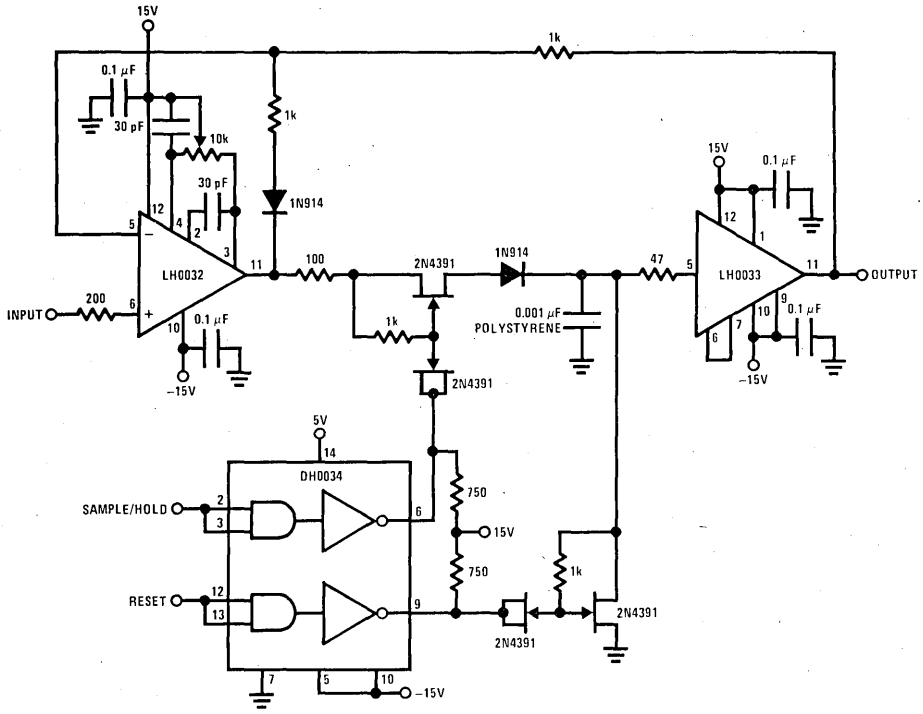


FIGURE 27. High Speed Peak Detector with Hold and Reset Controls

The LH0033 may be used as a cable-shield driver as shown in *Figure 28*. The advantage is that the source driver is not required to charge the line capacitance of the unterminated coaxial cable, and indeed does not need to match its line impedance; therefore, high speed data transmission is permitted.

The buffers may be used with a single supply without special considerations. A typical application is shown in *Figure 29*. The input is DC biased to mid-operating point and is AC coupled. Its input impedance is approximately 500 kΩ at low frequencies. Note that for DC loads referenced to ground, the quiescent current is increased by the load current set at the input DC bias voltage.

The high input impedance of the LH0033 and LH0063 are suitable for active filter applications. A basic two pole, high pass filter is diagrammed in *Figure 30* using the LH0033. The circuit provides a 10 MHz cutoff frequency. One consideration of the filter is its apparent gain change due to the finite output impedance of the amplifier, which affects the overall gain and the damping factor of the filter stage. Resistor R3 ensures that the input capacitance of the amplifier does not interact with the filter response at the frequency of interest.

An equivalent low pass filter is similarly obtained by capacitance and resistance transformation.

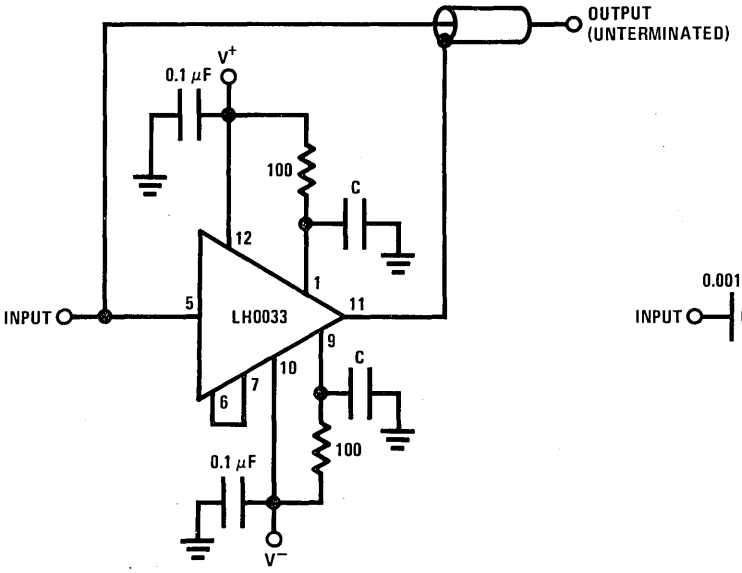


FIGURE 28. High Speed Shield/Line Driver

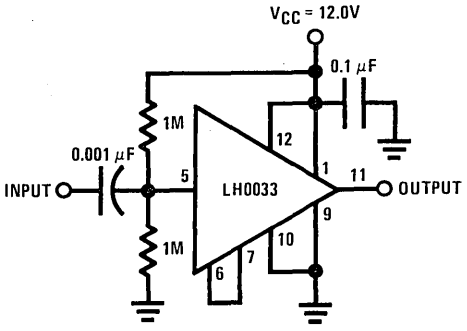


FIGURE 29. Single Supply AC Buffer Amplifier

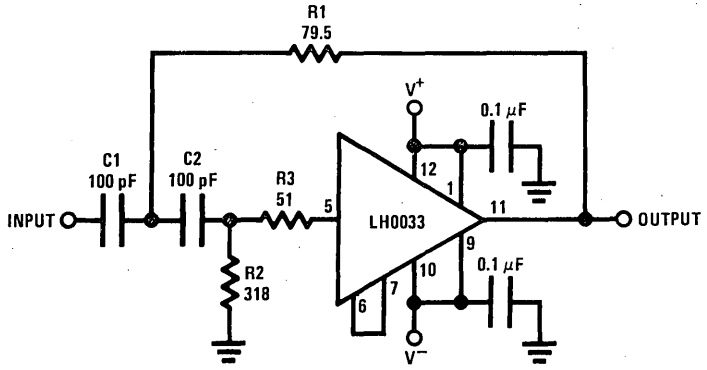


FIGURE 30. Wide Band Two Pole High Pass Filter

Another filter application is that of a high frequency notch filter, as shown in *Figure 31*. It takes advantage of the buffer's very high slewing capability. Component value sensitivity is extremely critical, as are temperature coefficients and matching of the components. Best performance is attained with perfectly matched components and when the gain of the amplifier is unity. To illustrate, the quality factor Q is very high as amplifier gain approaches 1 with all components matched (in fact, theoretically it approaches ∞) but decreases to about 12.5 with the amplifier gain at 0.98.

The most common use of the buffers is inside an op amp feedback loop as shown in *Figure 32*. The chart in the figure shows the ideal match of the buffer family to most popular operational amplifiers.

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"Application of the LH0002 Current Amplifier," National Semiconductor Corporation, AN-13, September 1968.

B. Siegel and L. Van Der Gaag, "Applications For a New Ultra-High Speed Buffer," National Semiconductor Corporation, AN-48, August 1971.

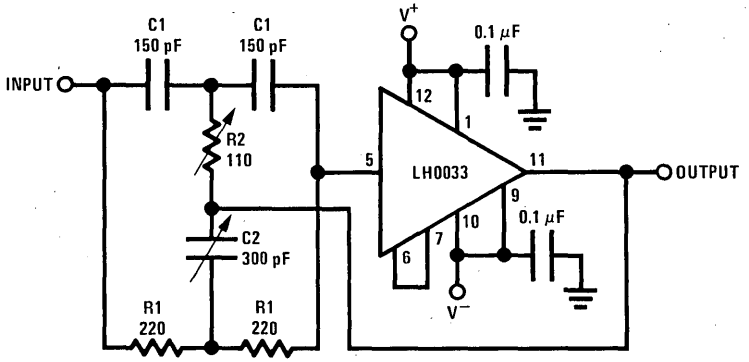
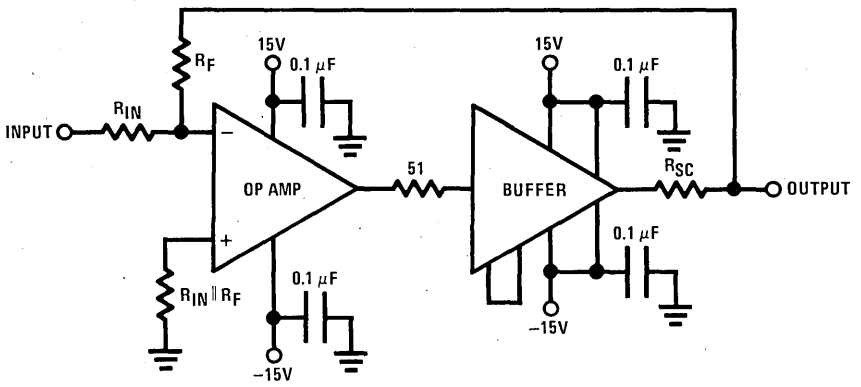


FIGURE 31. 4.5 MHz Notch Filter



Op Amp	Recommended Buffer	
LM101, LM108, LM741, LF151 LH0022, LH0042, LH0052	LH0002	
LF155, LF156, LF157, LH0024, LH0032	LH0033	$R_{SC} = \frac{V_S}{I_{SC}}$
LH0024, LH0032	LH0063	

FIGURE 32. Using Voltage Follower as Output Buffer

Introduction to Practical Fiber Optics

National Semiconductor
Application Note 244
Eric Miller

Introduction

We have all heard a great deal about fiber optics in the past number of years. Unfortunately, most of the discussion is about very high performance communications links. 200 Mbit, 20 Kilometer repeater-less links, jeweled connectors, solid state cooled lasers for transmission, and avalanche photodiodes for reception seem to be the rule. There is another side to fiber optics which is usually neglected, and that is the under-a-kilometer, less-than-50-Mbit fiber optic links. It is the purpose of this application note to de-mystify fiber optics in general, and to bring it into the designer's arsenal of problem-solving tools. We will primarily discuss fiber optic communications from a digital standpoint, but touch on a few analog applications. Fiber optic cable and connectors will be presented, followed by output transducers and transmitter circuitry, and finally input transducers and receiver circuitry.

First, however, we should review the fundamental advantages that fiber optics can bring. Superb electrical isolation can be obtained which also eliminates many grounding and safety-related problems. Fiber optic cable at this time is cost competitive with coax, and prices will drop dramatically as volume increases due to improved production techniques and abundant raw material (sand), its small size, light weight, and ruggedness surpass copper wire in every respect. Compared to coaxial cable, fiber optic cable significantly reduces signal attenuation while providing a much wider bandwidth. Crosstalk between adjacent pairs of optical fibers is eliminated by simply inserting each fiber in an opaque sheath. Fiber optic cable is EMI and RFI immune; neither is it susceptible to nor does it emit electromagnetic radiation.

Figure 1 shows a simplified diagram of a fiber optic link. An analog or digital input is conditioned by the transmitter circuitry and drives either an LED or semiconductor laser diode. This modulated light is launched into a fiber optic cable, terminated with the desired connectors on both ends. At the receiving end, a PIN photodiode or avalanche photodiode converts the incident light to a low level current which is processed by the receiver circuitry to provide a useful analog or digital output. Full duplex operation would require two such links.

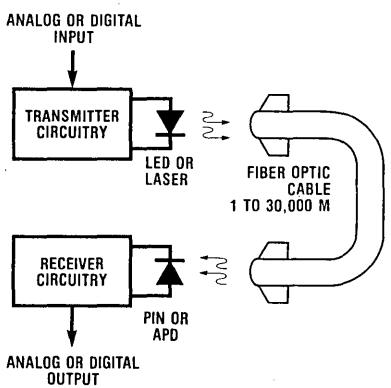


Figure 1: Simple Fiber Optic Data Link

Fiber Optic Cable

An end view and a cutaway view of a single stepped index optical fiber is shown in Figure 2. A stepped index fiber refers to the abrupt change in the index of refraction between the core and the cladding. All transmission of light occurs within the core. Given a core index of refraction n_1 and a cladding index of refraction of n_2, there will be a critical angle such that any light ray entering the core at less than that critical angle will be totally reflected. It is in this manner that light will propagate down the length of the optical fiber. This mechanism also gives rise to the term numerical aperture. The numerical aperture is defined as the Sine of the aforementioned critical angle, as shown in Figure 3. The numerical aperture defines a cone in which incident light may be launched into the cable, and in which light will emerge from the cable. The smaller the given numerical aperture, the more difficult it is to launch light into the fiber.

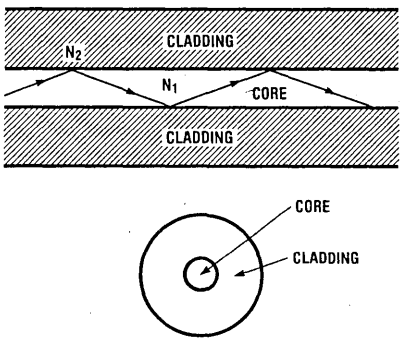


Figure 2: Stepped Index Fiber Cross Section

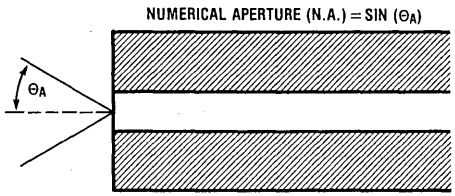


Figure 3: Numerical Aperture

Fiber Attenuation

The most important fiber specification is usually its attenuation characteristics. Specified at a given wavelength, the attenuation is measured in decibels per kilometer. Optical fibers are available whose attenuation can range from 0.2dB/km to 10,000dB/km. Figure 4 shows a simple example. We will suppose that we have an optical fiber whose attenuation at the wavelength of interest is 10dB/km. Light levels are measured in terms of power, and often expressed as dBm, i.e., referenced to 1mW. Therefore, if we launch 100μW of light into the cable (−10dBm) and the cable is 1km long, the light power at the receiving end will be 10μW or −20dBm. As previously mentioned, we must know the wavelength at which we are going to operate. Most red LED's emit light at 660nM, yellow at 585nM, green at 565nM and infrared (IR) at 900nM. Figure 5 shows a typical fiber's attenuation versus wavelength characteristics. Note that the attenuation can vary widely depending upon the chosen wavelength. A green LED would be attenuated by 18dB/km, a red LED 11dB/km. An IR LED would be significantly attenuated by 90dB/km. Figure 6 shows a somewhat better behaved wavelength-attenuation graph. This happens to be for a graded index fiber. Graded index refers to the index of refraction gradually decreasing as the distance away from the center of the cable. Note that there is no single wavelength that is optimum for all fibers. Careful consideration must be given to selecting the appropriate cable for use with the chosen emitter wavelength.

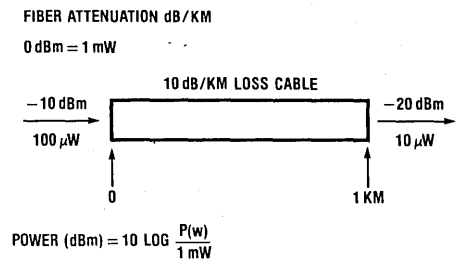


Figure 4: Fiber Attenuation (dB/km)

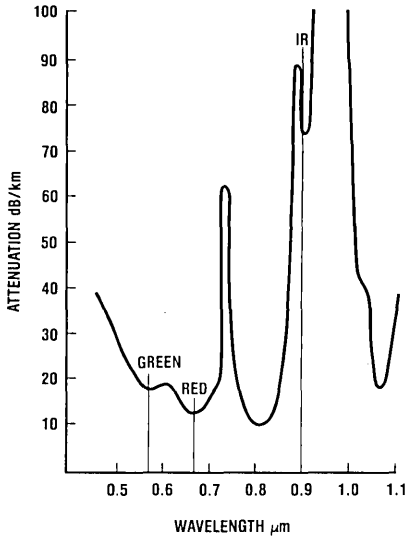


Figure 5: Typical Fiber Attenuation versus Wavelength (Step Index)

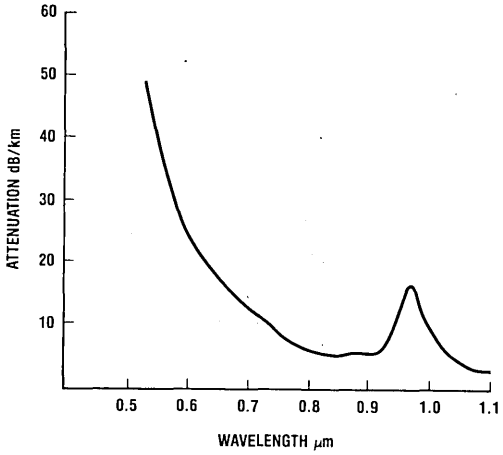


Figure 6: Typical Fiber Attenuation versus Wavelength (Graded Index)

Numerical Aperture

Each fiber has a characteristic numerical aperture which is usually between 0.2 and 0.4. This corresponds to light entry half angles of 11 to 24 degrees respectively. Large bandwidth low attenuation cables typically exhibit smaller numerical apertures. The core index of refraction is usually given in a data sheet; we can then calculate the propagation delay down a given length of cable. The propagation speed is simply the speed of light divided by the core index of refraction. For example, if a fiber's core index of refraction is 1.5, then the speed at which light will travel down the fiber is $2X10^8$ meters per second. Thus it will take 500 nanoseconds for light to travel to the end of a 100 meter cable.

Bandwidth

We also need to know the bandwidth of the cable chosen. This specification may be given as MHz/km or as a more obtuse spec; −3dB intermodal dispersal expressed in ns/km. A 200 MHz/km cable will exhibit an attenuation of −3dB at 200MHz at the end of a 1-km long cable. To calculate the bandwidth constraint from the intermodal dispersion expressed in ns/km, simply divide 0.35 by the given specification. Thus, if a fiber is characterized by a 3ns/km −3dB intermodal dispersion, this is equivalent to 116 MHz/km. In simpler terms, when the dispersion is given in ns/km, this indicates the increase in signal rise time per a given length of fiber.

Fiber core diameter can vary from less than 10μM to more than 1500μM. In general, high bandwidth, low attenuation fibers are available in small diameter fiber cores and small numerical apertures. Figure 7 gives a list of a few cable and fiber manufacturers. Cables are available with one fiber per cable to upwards of twenty.

EXAMPLES OF CABLE AND FIBER MANUFACTURERS
BELDEN
CANSTAR
CORNING
DUPONT
GALILEO
ITT
OPTELCOM
QUARTZ PRODUCTS
SIECOR
TIMES WIRE AND CABLE
VALTEC

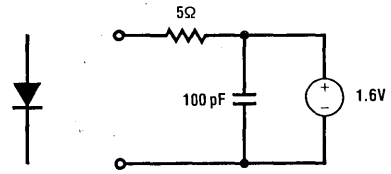
Figure 7: Cable and Fiber Manufacturers

Connectors

Although there is no standard cable connector, the AMP and SMA type connectors are the most popular. Figure 8 gives a representative list of connector manufacturers. In general, inexpensive plastic type connectors are capable of less than 3dB of insertion loss on fibers as small as 125μM. Smaller fibers, or lower insertion loss, require the use of metal connectors at increased cost. Connectors are available in single or multiple fiber versions, and one can obtain connectors where the user may mix conventional wire conductors with optical fibers in the same connector.

PARTIAL LIST OF CONNECTOR MANUFACTURERS
AMP
AMPHENOL
AUGAT
BELDEN
BENDIX
DEUTCH
ITT CANNON
3M
PLESSEY
THOMAS & BETTS
TRW

Figure 8: Connector Manufacturers



LED & EQUIVALENT CIRCUIT

REPRESENTATIVE MANUFACTURES OF EMITTERS—
LASER AND LED
ABORN
FAIRCHILD
GENERAL OPTRONICS
HP
ITT
LASER DIODE LABS
MATH ASSOCIATES
MERET
MONSANTO
MOTOROLA
NATIONAL SEMICONDUCTOR
PLESSEY
RCA
SPECTRONIC
TI

Figure 9: Emitters — Laser and LED Manufacturers

Optical Emitters

The two most practical methods of converting electrical signals to light for fiber optics are via the light emitting diode or laser diode. Typical LED's used as panel lights can produce 15 to 30 μW of optical power. LED's that are designed for fiber optic use can produce up to 10 mW. An electrical equivalent circuit for a typical LED is shown in Figure 9. Typical operating currents are in the range of 50 to 100 mA peak with a forward voltage of 1.6 to 2.0 volts.

Light Emitting Diodes

LED's are normally broken down into three categories, surface, edge and Burrus. Surface emitters emit light over the entire surface of the die whereas edge emitters produce maximum light power along the edge of the die. The Burrus LED emits light from an etched well in the surface of the LED; this permits tailoring the size of the well to the diameter of the optical fiber being used.

Speed of response can vary from a few nanoseconds to 500 ns. Note that even if we are able to impress the proper voltage across an LED, and the proper current through it, this does not mean that we have optical power output. Consult the manufacturer or the data sheet to ascertain if the chosen LED will support the bandwidth or data rate for which the link is designed.

LED's are obtainable with wavelengths from green (565 nM) to infrared (1300 nM). Conventional red (660 nM) is the most popular and the least expensive. Figure 9 also lists a number of manufacturers of LED's and laser diodes.

Laser Diodes

There are two popular kinds of laser diodes, single and double heterostructure. The single heterostructure laser diode is not capable of producing continuous optical power. It must be used in a small duty cycle mode with typical pulse widths of 100 ns. Output power is high (10W), although the drive requirements are severe, 6 to 30A peak. The double heterostructure laser diode is similar to an LED in ease of use. It exhibits no duty cycle limitations, and requires about 100 to 400 mA peak current for typical operation. Output power is 10-20 mW, wavelength is near 900 nM, and optical rise-time is less than a nanosecond. Unfortunately, the price of these lasers at the time of this writing is still high, approximately $1000 each, although the price is expected to drop dramatically over the next few years.

Transmitter Circuitry

Figure 10 shows three methods of modulating LED's. In Figure 10a., an open collector TTL gate drives a transistor which shunts current away from the LED in the off state. When the input to the gate is low, the transistor is turned off and resistor R2 supplies the desired on current. This method is good for data rates to 20 megabits.

Figures 10b and c show how to modulate an LED linearly. U1 is any general purpose op amp and operates as a voltage controlled current source with the LED as the load. Q1 is a general purpose NPN (2N2222), which is capable of supplying up to 100 mA necessary for driving the LED. Note that the circuit works for positive input voltages only. High speed operation may be obtained by using

wide bandwidth op amps such as the LH0032. Figure 10c illustrates an alternative method of analog modulation. An LH0002 unity gain buffer is used, with the LED in the positive supply of the buffer. An input voltage is converted to a drive current for the LED by means of driving load resistor R1. The 6 to 10 mA of LH0002 quiescent supply current also flows thru the LED. A shunt resistor in parallel with the LED can divert the bulk of this current, if desired.

The transmitter circuitry remains fairly simple for data rates to 50 Mbps. Temperature compensation of optical output power can be easily accomplished if necessary with the addition of a small amount of circuitry as shown in Figure 10d.

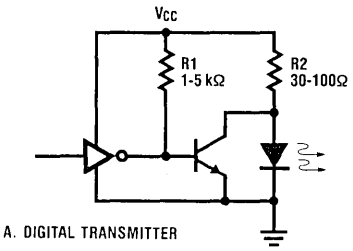


Figure 10a: Digital Transmitter

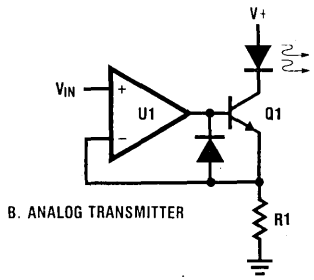


Figure 10b: Analog Transmitter

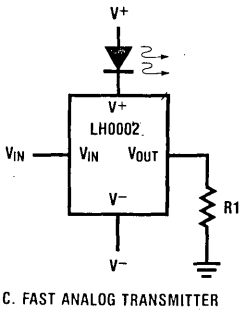


Figure 10c: Analog Transmitter

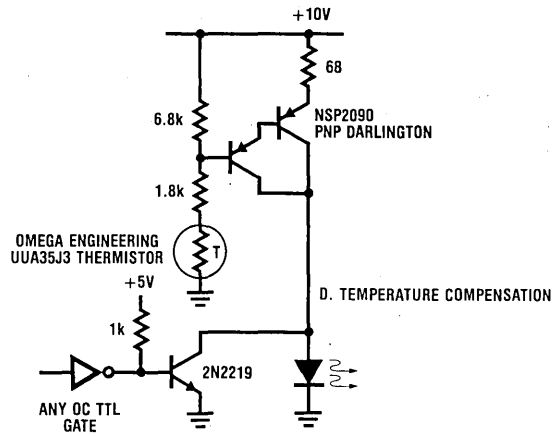


Figure 10d: Temperature Compensation

Optical Sensors

The receiver circuitry for fiber optic transmission is slightly more difficult. First, we will discuss the basic characteristics of the most commonly used photodetectors. The four most popular photosensors are shown in Figure 11. The photodiode, phototransistor, PIN photodiode and avalanche photodiode all operate on the same basic principle. An incident photon creates a hole-electron pair near or within the depletion region. The electrical field separates the pair and causes current to flow in an external circuit. Figure 11 also shows an equivalent circuit for a photodiode. R_S is usually on the order of 10 to 100 ohms, R_P is 10^9 to 10^{10} ohms typically, and C_P is the photodiode's capacitance, dependent upon processing and area. Note the direction of photo-induced current flow, as conventional current is sourced by the anode. This is not the same mode typically used for solar cell operation — the photovoltaic mode. In this mode, a portion of the photocurrent flows thru the photodiode itself, producing a voltage from anode to cathode. The photocurrent mode, however, is superior to the photovoltaic mode in linearity, speed of response, stability and temperature coefficient. Thus, we will limit our circuitry discussion to using the photodiode in the photocurrent mode alone.

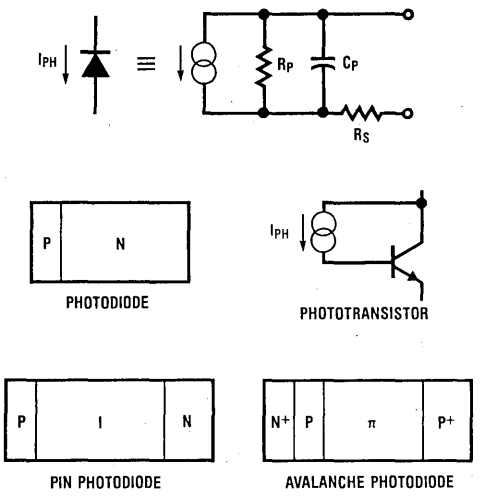


Figure 11: Photodetectors

Phototransistor

The phototransistor can be modeled by a photo-induced current source between the collector and the base. Beta multiplication produces a much larger photocurrent at the emitter or collector; however, this is at the expense of speed of response. The small photocurrent must charge the base-emitter capacitance, producing slow rise and fall times. Gain-bandwidth is typically 200 MHz. The uncertainty in sensitivity due to beta variations, and the slow response relegate the phototransistor to relatively low performance fiber optic receivers.

PIN Photodiode

The PIN photodiode enhances the conventional photodiode's utility by producing the same amount of photocurrent from a lower capacitance source, thus giving higher speed operation. In normal operation, the entire intrinsic region is depleted, thus spreading apart the "plates" of the capacitor. Frequency response is typically to 1 GHz.

Avalanche Photodiode

The avalanche photodiode requires 150 to 300 volts of reverse bias to operate. Photo induced carriers are swept into a high field region where avalanche multiplication takes place. This produces front-end signal gain (50-500) without paying a speed penalty. Gain-bandwidth product of an avalanche photodiode is in the neighborhood of 100 GHz. The drawbacks to avalanche photodiodes are the high bias voltage needed, and the temperature compensation necessary for stable operation.

Responsivity

A photodiode's most fundamental characteristic is its responsivity, i.e., the amount of current it will produce in response to the incident light power. Responsivity is given in amperes per watt. Figure 12 illustrates a typical reponsivity versus wavelength for a silicon photodiode. The responsivity drops below 900 nM due to absorption, and above 900 nM due to the band gap of silicon (1.2 eV). A similar graph could be shown for a phototransistor or an avalanche photodiode. The y-axis would simply be multiplied by beta or the avalanche gain respectively. Note that when the incident light is measured in watts, the area of the detector does not play a part in the quantity of current produced. A photodiode whose responsivity at a given wavelength is 0.5 will produce 1 μA in response to an incident light power of 2 μW as long as all of the light falls on the photodiode's sensitive area. Figure 13 gives a list of some of the manufacturers of photodiodes, phototransistors, and avalanche photodiodes.

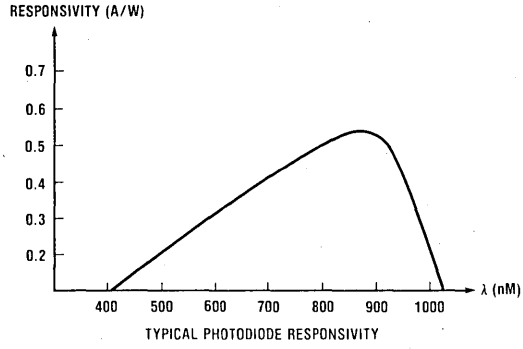


Figure 12: Typical Photodiode Responsivity

DETECTOR MANUFACTURERS
ABORN
CENTRONIC
EG & G
HP
MATH ASSOCIATES
MERET
MOTOROLA
RCA
SPECTRONICS
TI
UNITED DETECTOR TECHNOLOGY
VALTEC

Figure 13: Detector Manufacturers

Receiver Circuitry

The most challenging aspect of many fiber optic links is the design of the receiver. The receiver must convert the low level current output of a photodiode to a high level analog or digital signal with accuracy and speed.

Figure 14 illustrates the simplest of fiber optic receivers. The photodiode is back biased with a resistor to convert the photo-induced current to a voltage. Let us assume that we want to convert an input light power of 300 nW to a 15 mV signal. If the photodiode's responsivity is 0.5 A/W, then the photodiode will produce 150 nA, and for a 15 mV signal level, the resistor must be 100k. If the capacitance of the photodiode is 10 pF, then the rise time of the voltage output in response to a step light input will be approximately 2.2 μs. This also implies that our analog bandwidth is limited to a −3 dB frequency of 159 kHz.

How is it possible to obtain higher frequency performance at the same sensitivity without sacrificing signal-to-noise ratio? Decreasing the size of the resistor and using voltage amplifiers can achieve the same responsivity at a higher speed but it will sacrifice signal to noise ratio since a resistor's noise current contribution increases as the value of the resistor decreases. As we will see later, signal-to-noise is not only important for analog communication, but also sets the limiting bit error rate for digital signaling.

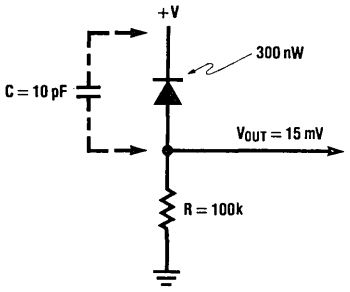


Figure 14: Simple Receiver

A single circuit topology can be practically applied in two ways to help us out. Figure 15 illustrates the general topology, with the first of the two specific implemenations shown below. This is known as the bootstrap configuration as the function of the amplifier is to chase the voltage developed by the photocurrent flowing thru the resistor, and to apply this voltage to the opposite end of the photodiode. By keeping the voltage change across the photodiode's capacitance small, the effect of this reactance is reduced, and the circuit will respond faster. By rearranging the general topology once again, we arrive at the second implementation, known as the transimpedance approach as shown in Figure 16. Since the negative input of the amplifier can be considered a virtual ground, the voltage change across the photodiodes's capacitance is kept small and thus its effect is reduced. The choice between either of the two approaches is left to the designer; however, the constraints placed on either of the amplifiers are the same when speed of response is used as the criterion.

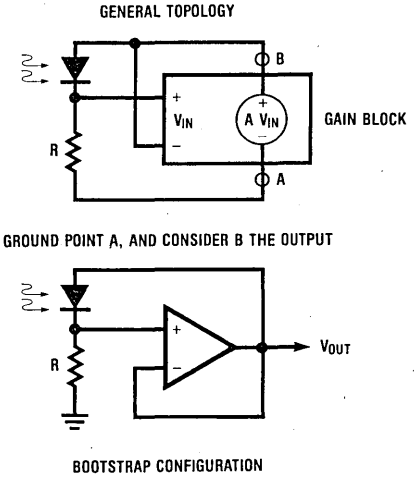


Figure 15: General Topology, Bootstrap Configuration

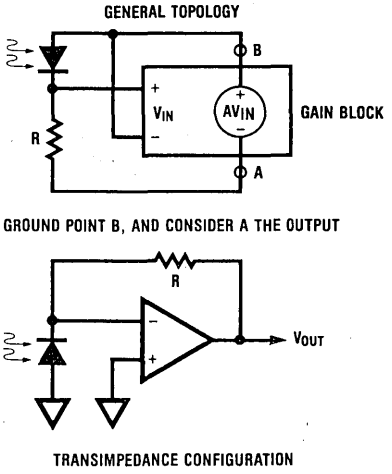


Figure 16: General Topology, Transimpedance Configuration

To give us an idea of how fast an amplifier we need to produce the desired speed of response, we will analyze the transimpedance circuit of Figure 17. We first define a time constant t that is equal to the product of the feedback resistor and lumped circuit capacitance C. C is the sum of stray capacitance, amplifier input capacitance and photodiode capacitance. The only other parameter to define is t_A, the inverse of the gain-bandwidth product of the amplifier. When we solve this simple circuit analysis problem, we find that the rise time of V_{OUT} is:

$$t_R = \pi\sqrt{t \cdot t_A}$$

$$t = RC,\ t_A = \frac{1}{2\pi(GBW)}$$

Rise time is chosen as the prime indicator of circuit speed performance as it allows us to make rapid calculations of the maximum bit rate for a digital communications link. The equation given above is an approximation as it assumes that the open loop gain of the amplifier is greater than 10 and $t < 2A_O t_A$, where A_O is the open loop gain of the amplifier.

Returning to our original problem, how fast must our amplifier be to produce the desired overall fiber optic receiver speed? Let us use a specific example to determine the required amplifier speed. Suppose that we want to receive a 5 Mbit NRZ signal, our feedback resistor is 100k, and the circuit capacitance is 5.5 pF. From the data rate, we know that the rise time of the receiver must be 100 ns or less. Rearranging the above equation, we obtain:

$$\frac{1}{t_A} = \frac{\pi^2 t}{t_r^2}$$

When we plug in the numbers, we find that the gain-bandwidth of the amplifier must be 86 MHz! It's obvious that a 741-type amplifer with a gain-bandwidth of 1 MHz will not even come close to providing the speed we need. Fortunately, the LH0082 fiber optic receiver produced by National Semiconductor contains a preamp with a gain-bandwidth product of nearly 2 GHz. The LH0082 will provide the sensitivity and speed necessary for the example application, and it also includes a comparator for providing a TTL/DTL/CMOS compatible output. Figure 18 is a block diagram of the LH0082. Two internal feedback resistors are included for use with the preamp to set sensitivity. External resistors can also be used. The output of the preamp is AC coupled to a comparator that can be connected as an edge triggered flip-flop. In this mode, the bit error rate can be set by the amount of hysteresis applied to the comparator. Using the internal hysteresis resistor, the bit error rate is better than 10^{-10}. The entire circuit operates from a single 4.5 to 5.5 volt power supply, although the preamp can be operated to 10 volts, and the comparator to 15 volts.

Figure 19 shows how to use the LH0082 as a 5 Mbit, 300 nW sensitivity fiber optic receiver. The only external components needed are the photodiode, a power supply decoupling resistor and two bypass capacitors.

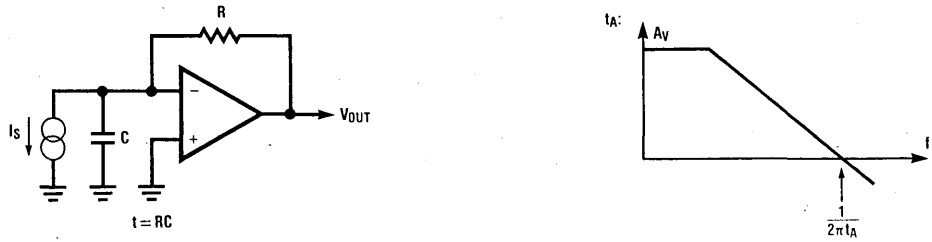


Figure 17: Equivalent Circuit and Amplifier Characteristic

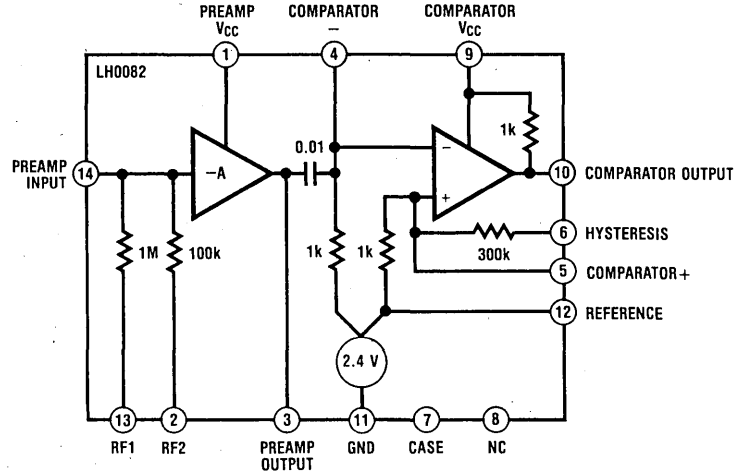


Figure 18: LH0082 Circuit Diagram

Bit Error Rate

The bit error rate (BER) is a very important consideration in any digital communications system; fiber optic data links are no exception. A BER of 10^{-10} means that one bit of 10 billion will be a bad bit. Obviously, the smaller the BER, the better off we are. There is a very simple relationship between the signal-to-noise ratio and the bit error rate. Given δ as the RMS noise voltage, A as the peak-to-peak signal level, and we determine the presence of one or a zero with a threshold of A/2, then the BER is:

$$BER = \tfrac{1}{2}\left(1 - \text{erf}\ \frac{A}{2\sqrt{2}\,\delta}\right)$$

$$\text{Where: erf}\ (x) = \frac{2}{\sqrt{\pi}}\int_0^x e^{-y^2}dy$$

Figure 20 is a plot of this somewhat obtuse function. Note that we are guaranteed a BER of 10^{-10} with only 22dB of signal-to-noise ratio. Thus, if we have a comparator threshold of 10mV, a peak signal level of 20mV, then the RMS noise must be less than 1.6mV to give us 10^{-10} BER.

Stray Signal Pickup Problems

Although communication via fiber optic cable provides freedom from the effects of radio frequency interference, the circuitry at the receiver is not so fortunate. Let's take the example of the basic LH0082 300nW sensitivity receiver. Assuming a 0.5A/W photodiode, the LH0082 requires only 150nA at its input to cause the comparator to switch states. Suppose that the output of a TTL gate is nearby and at that point the voltage can traverse 3V in as little as 5ns. How much stray capacitance from this TTL output to the input of the LH0082 is needed to equal the signal level generated by the photodiode.

$$\text{Since } I = C\frac{dv}{dt}$$

$$\text{Then } C = \frac{I\,dt}{dv}$$

$$C = \frac{(150\,nA)\,(5\,ns)}{3V}$$

Thus $C = 2.5 \times 10^{-16}$F or .00025pF!!!

Although this may seem like an impossibly small amount of capacitance to live without, straightforward printed circuit board layout techniques can provide trouble-free operation.

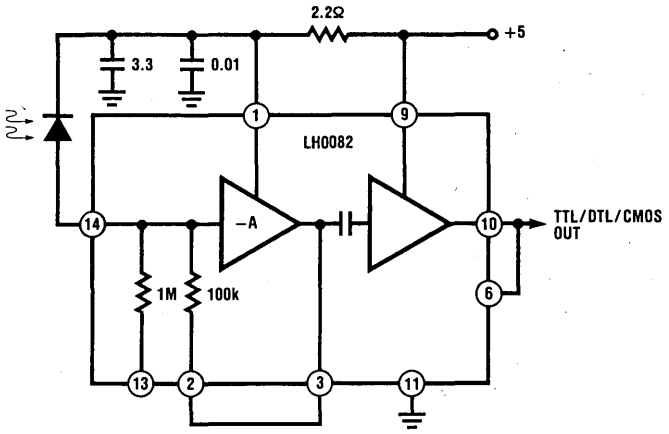


Figure 19: LH0082 Basic Operating Circuit — 300nW, 5Mbit

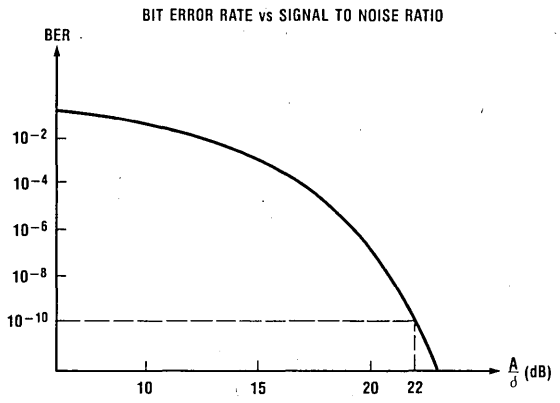


Figure 20: Bit Error vs. Signal-to-Noise Ratio

A Complete Link

Putting together a total link is not so difficult as the "experts" would have you believe. We can be almost sloppy in our handling of the transmitter circuitry, light coupling to transducers, and connecting the cable. The expense is a little care at the receiver end.

Figure 21 gives a sample application ideally suited to fiber optics. A data entry room is located 300 meters from a computer facility, separated by a manufacturing area containing arc welders, punch presses and the like. One-way communication from the three data entry terminals to the computer is required at 19.2 Kbits. Let us assume that we will multiplex the three data channels with one sync. channel and send the signal through one fiber optic cable, and demultiplex the signal at the computer end. We will sample each of the three data channels and the sync. channel at 5 times the data rate or $4 \times 19{,}200 \times 5 = 384$ kbit data rate. We will select an inexpensive red indicator LED whose total output power is only 30 μW or -15 dBm. We must now account for all of the losses involved in transferring this light to the photodiode at the receiving end:

$$\begin{aligned} \text{LED-transmitter connector:} &\quad -10\text{dB} \\ \text{receiver connector:} &\quad -3\text{dB} \\ 300\text{M} \times \frac{40\text{dB}}{1000\text{M}}\ \text{(cable):} &\quad -12\text{dB} \\ \text{Safety factor:} &\quad -3\text{dB} \\ \text{Total loss} &= -28\text{dB} \end{aligned}$$

Thus, the power at the receiver is:

$-15\text{dBm} - 28\text{dB} = -43\text{dBm}$ (50 nW)

The LH0082 in the high sensitivity mode ($R_F = 1$M) has a 30 nW sensitivity with a 0.3 A/W photodiode and can provide a maximum data rate of 650 kbit. The use of inexpensive connectors, poor coupling of light to the fiber at the transmitter end, and cheap, moderate loss cable (40 dB/km) does not prohibit a high performance data link when used with a versatile receiver such as the LH0082.

Conclusion

Many such applications can be implemented by using cost effective, moderate performance LEDs, connectors and fiber optic cable by taking a little extra care with the receiver circuitry. The National Semiconductor LH0082 provides a versatile solution to such fiber optic receiver needs.

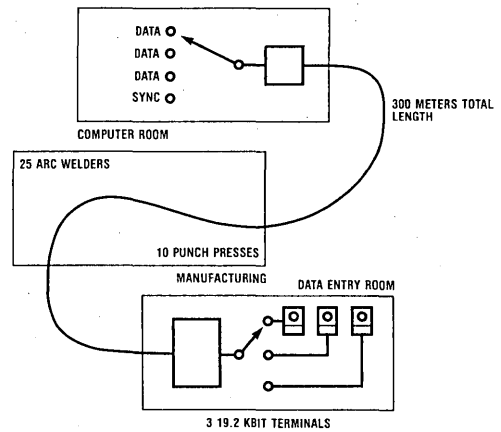


Figure 21: Sample System

Application of the ADC1210 CMOS A/D Converter

National Semiconductor
Application Note 245
James Wong

Introduction

The ADC1210 is the answer to a need for analog to digital conversion in applications requiring low power, medium speed, or medium to high accuracy for low cost. The versatile input configurations allow many different input scale ranges and output logic formats.

The wide supply voltage range of 5V to 15V readily adapts the device to many applications. The very low power dissipation yields remarkable conversion linearity over the full operating temperature range. *Table I* below summarizes the typical performance of the ADC1210.

TABLE I
ADC1210 Performance Characteristics

Resolution	12 bits
Linearity Error, $T_A = 25°C$	±0.0122% FS MAX
Over Temperature	±0.0244% FS MAX
Full Scale Error, $T_A = 25°C$	0.1% FS MAX
Zero Scale Error, $T_A = 25°C$	0.1% FS MAX
Quantization Error	± ½ LSB MAX
Conversion Time	200 μs MAX

This note expands the scope of application configurations and techniques beyond those shown in the data sheet. The first section discusses the theory of operation. The remaining sections are devoted to applications that extract the optimum potential from the ADC1210.

Theory of Operation

Like most successive approximation A to D's, the ADC1210 consists of a successive approximation register (SAR), a D to A converter, and a comparator to test the SAR's output against the unknown analog input. In the case of the ADC1210, these elements are connected to allow unusual versatility in matching performance to the user's applications.

The SAR is a specialized shift register programmed such that a start pulse applies a logical low to the most significant bit (MSB) and logical highs to all other bits, thus applying a half scale digital signal to the DAC. If the comparator finds that the unknown analog input is below half scale, the low is shifted to the second bit to test for quarter scale. If, on the other hand, the comparator finds that the analog input is above half scale, the "low" state is not only shifted to the second bit, but also retained in the MSB, thus forming the digital code for three quarters scale. Upon completing the quarter (or three-quarter) scale test, the next clock pulse sets the SAR to test either ⅛, ⅜, ⅝, or ⅞ full scale, depending on the input and the previous decisions. This successive half-the-previous-scale approximation sequence continues for the remaining lower order bits. The thirteenth clock pulse shifts the test bit off the end of the working register and into the conversion complete output. *Figure 1* shows the schematic diagram of the device.

Operating Configurations

Figures 2 through *5* show four operating configurations in addition to those presented in the data sheet.

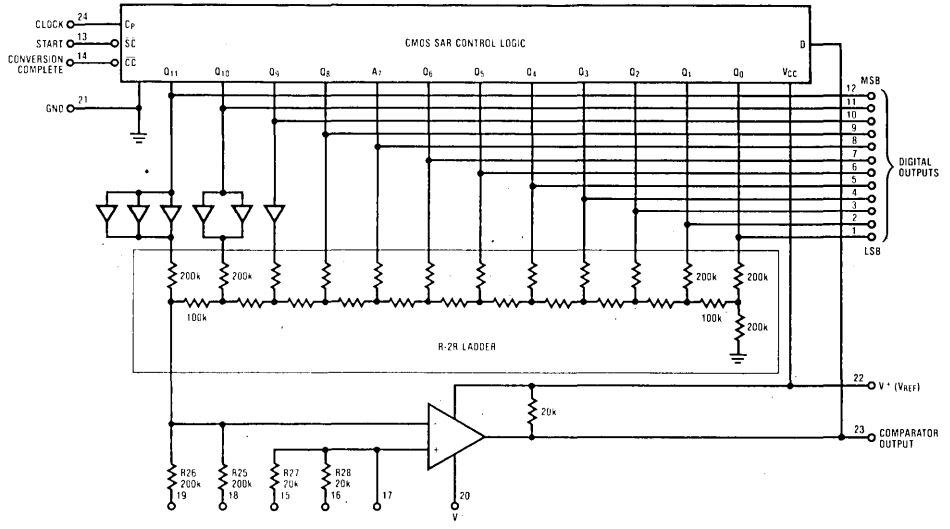


Figure 1. Schematic Drawing

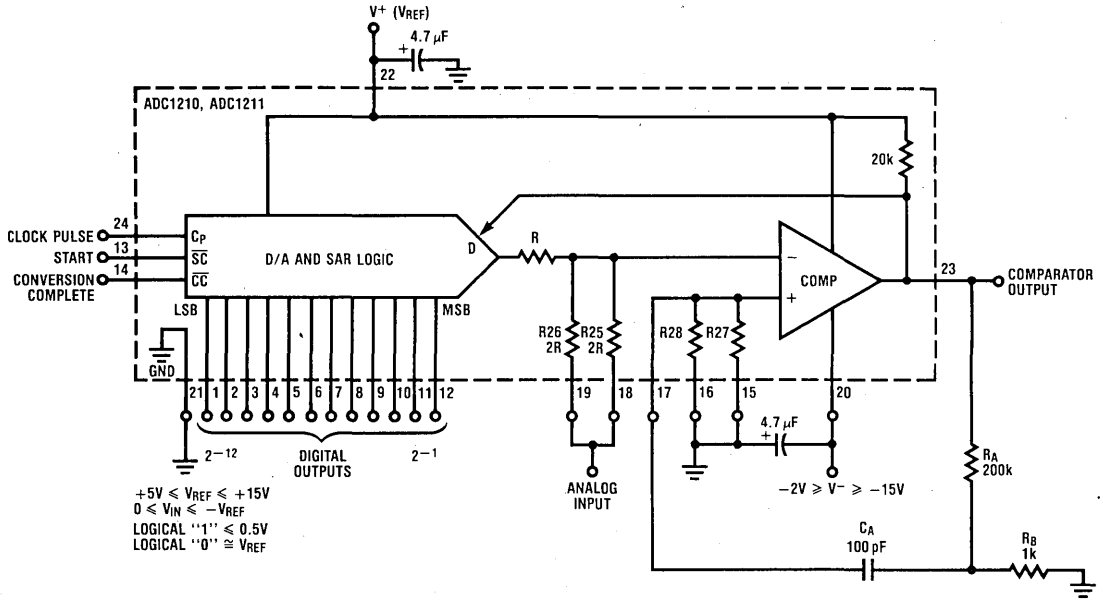


Figure 2. Complementary Logic, 0V to $-V_{REF}$ Input

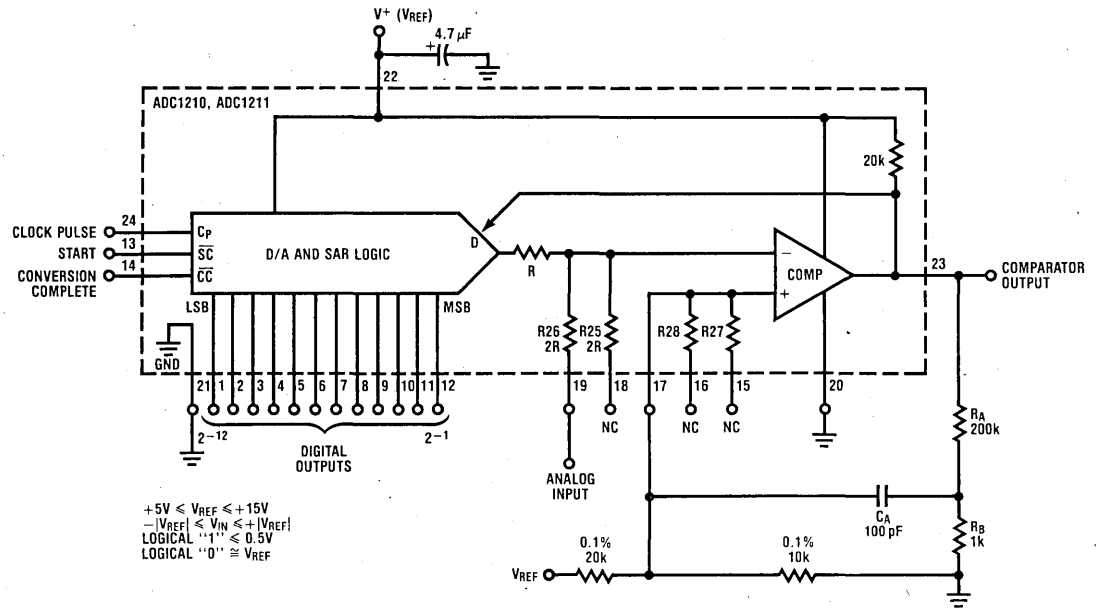


Figure 3. Complementary Logic, Bipolar $-V_{REF}$ to $+V_{REF}$ Input

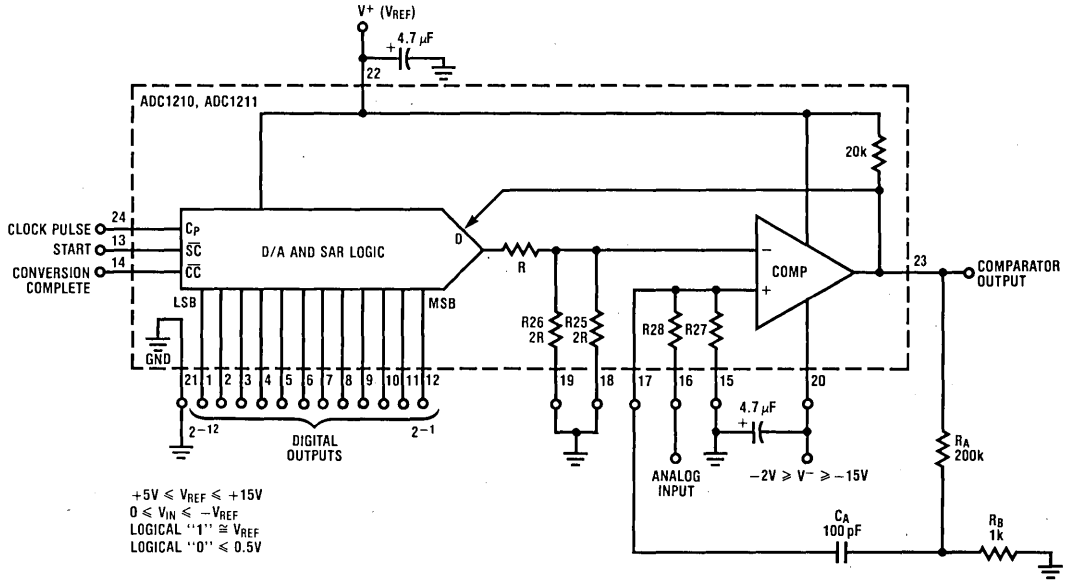


Figure 4. Positive True Logic, 0V to $+V_{REF}$ Input

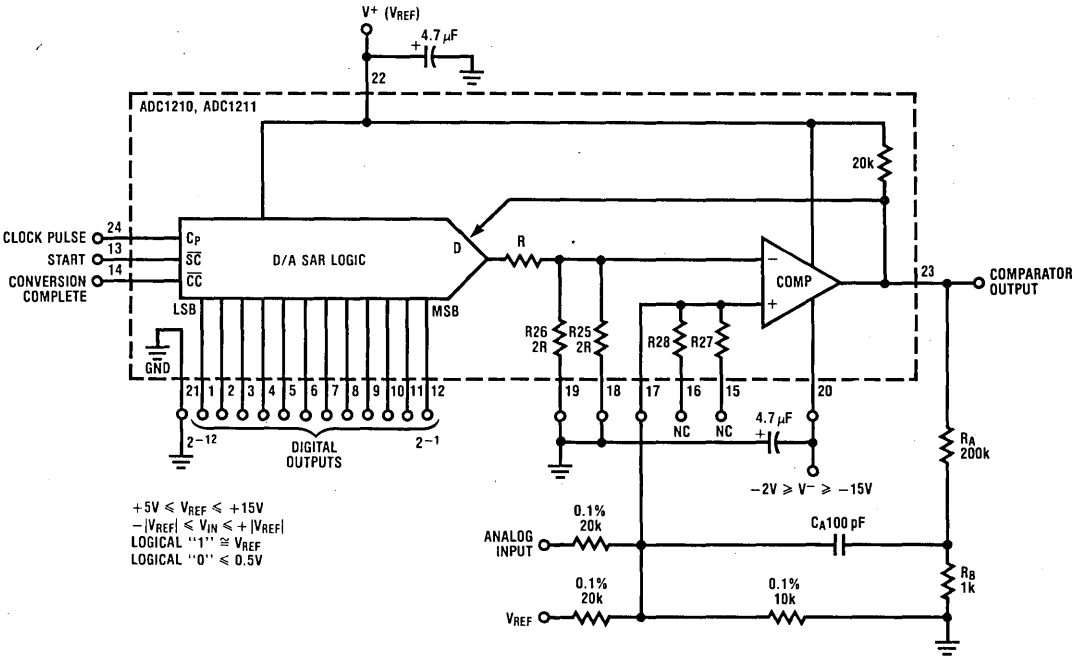


Figure 5. Positive True Logic, Bipolar $-V_{REF}$ to $+V_{REF}$ Input

Design Considerations

To Complement, or Not to Complement

Of the two recommended logic configurations, the complementary version is preferred. It provides greater accuracy than the straight binary version. The reason for that is that with the complementary logic configuration, a reference voltage is fixed at the non-inverting input of the comparator. Consequently, the comparator operates at this fixed threshold independent of the input voltage. For the straight binary configuration, the analog input drives the non-inverting input of the comparator so that the common mode voltage on the comparator input varies with the analog input. This adds a non-linear offset voltage of less than ¼LSB.

Regardless which configuration is used, the comparator input common mode range must net be exceeded. In fact, the voltage at either comparator input must be no less than 0.5 volts from the negative supply and 2.0 volts from the positive supply. Therefore, for applications requiring common mode range to ground, simply connect a negative supply (−2V to −15V) to pin 20.

Layout Considerations

High resolution D/A and A/D converter circuits may have their entire error budget blown if any digital noise is allowed to enter the analog circuit.

Exercising care in the layout is certain to minimize frustrations. Single point analog grounding is a good place to start. All analog ground connections and supply bypassing should be returned to this point. In fact, in critical applications, the ADC1210 GND pin should be made "the" reference node. Furthermore, one should separate the analog ground from the digital ground. Any excursion of switching spikes generated in the digital circuit is, to some degree, decoupled from the analog circuitries. *Figure 6* illustrates this. Of course, these two points are eventually tied together at the power supply/chassis common.

In addition to a good ground system, it is a good idea to keep digital signal traces as far apart from the analog input as is practical in order to avoid signal cross coupling.

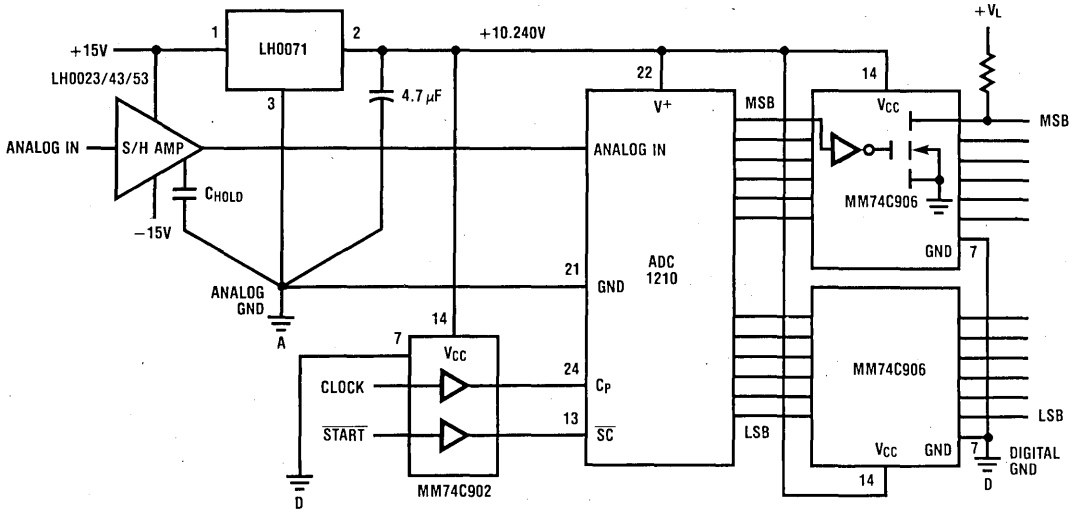


Figure 6. Grounding Considerations of Interface Circuits

Power Supply Bypassing

The supply input not only provides power to the digital logic, it is also a reference voltage to the resistor ladder network of the ADC1210. This voltage must be a very stable source. A precision reference device such as the LH0070 or LH0071 is ideal for the ADC1210. However, the internal CMOS Successive Approximation Register (SAR) invariably generates current spikes (10-20 mA peak) in the supply pin as the logic circuit switches pass the linear region. Consequently, if a reference device such as the LH0070 is used, the current spike tends to cause excursions in the reference voltage, thus threatening conversion accuracy. To preserve the 12-bit accuracy, bypass the supply pin with a 4.7 μF tantalum capacitor. In high noise environments, a 22 μF capacitor shunted by a 0.1 μF ceramic disc capacitor is desirable.

If pin 20 is connected to a negative supply, it too should be bypassed to prevent voltage fluctuations from affecting the comparator operation.

Output Drive Capability

The digital outputs of the ADC1210 and the outputs of the SAR, through which the resistor ladder is referenced, are one and the same. Any excessive load current on the digital outpt lines will degrade conversion accuracy. For this reason, the ADC1210 must interface with CMOS logic. However, the three most significant bits (pins 10, 11, and 12) are buffered from the R-2R ladder and are capable of driving light loads without degrading linearity. This could prove useful in 2's complement applications where an inverter is necessary in the MSB; one might construct this inverter with a discrete NPN transistor and two resistors. The bit most sensitive to output loading is the fourth most significant (pin 9). An error voltage at this pin gets divided down by a factor of 16 before being applied to the comparator, so if we wish to limit the error due to output loading to say, ½LSB, or 1.25 mV at the comparator, we can tolerate 20 mV at pin 9. If all lower bits will have the same output load, the error must be limited to 10 mV. Since all of the digital outputs have a maximum ON resistance of 350Ω at 10V V_{REF} in both high and low states, the maximum allowable load current is 10 mV/350Ω = 29 μA. This current requirement is easily satisfied with an MM74C914 or MM74C901 thru MM74C902 level translators for interface with logic levels different than V_{REF}.

Comparator Hysteresis

Even an ideal comparator can be expected to oscillate due to stray capacitive feedback if biased in the linar region. It is the normal operation of the SAR feedback loop to do just that . . . at least at or toward the end of the conversion cycle. For most applications, this oscillation is only a minor bother, as the SAR register would have locked out the converted data from further changes at the end of conversion. If that is still undesirable, the Conversion Complete ($\overline{CC}$) Signal may be used to drive an open-collector gate (such as the MM74C906) with the output wire-ORed to the comparator output. In this way, the comparator is always clamped to the low state at the end of conversion. Normal operation resumes upon restart of a new conversion cycle.

In normal operation, however, if we want to preserve 12-bit accurcy, the comparator oscillation should be suppressed. The recommended technique is to apply a slight amount of AC hysteresis (50 mV) at the beginning of the decision cycle, but let it decay away to an acceptable accuracy before the decision is actually recorded in the SAR. The approximate decay time is (5) × (10k + 1k) × (100 pF), or 5.5 microseconds (see *Figure 2*).

For those applications using supply voltage other than 10V, say 5V, and if 50 mV initial hysteresis is to be maintained, the 200kΩ (R_A) resistor in *Figure 2* should be changed to 100kΩ based on the relationship:

$$\frac{R_B}{R_A + R_B} V_{REF} = 50\,mV$$

Where: $R_B = 1\,k\Omega$

High Speed Conversion Technique

By using one IC, one discrete NPN transistor, and a resistor, the ADC1210 can be made to run at up to 500kHz clock frequency, or 12-bit conversion time of 26 μs. The circuit is shown in *Figure 7*. The idea is to clamp the comparator output low until the SAR is ready to strobe in the data at the rising edge of the conversion clock. Comparator oscillation is suppressed and kept from influencing the conversion decisions. This technique eliminates the need for the AC hysteresis circuit.

To implement the idea, a complementary phased clock is required. The positive phase is used to clock the converter SAR as is normally the case. The inverted clock, generated from the same clock signal, is inverted by the transistor. The open collector is wire-ORed to the output of the comparator. During the first half of the clock cycle (50% duty cycle), the comparator output is clamped and disabled, though its internal operation is still in working order. During the last half cycle, the comparator output is unclamped. Thus, the output is permitted to slew to the final logic state just before the decision is logged into the SAR. The MM74C906 buffer (or with two inverting buffers) provides adequate propagation delay such that the comparator output data is held long enough to resolve any internal logic set-up time requirements.

The 500kHz clock implies that the absolute minimum amount of time required for the comparator output to be unclamped is 1 μs. Therefore, for applications with clock signal other than 50% duty cycle, this 1 μs period must be observed.

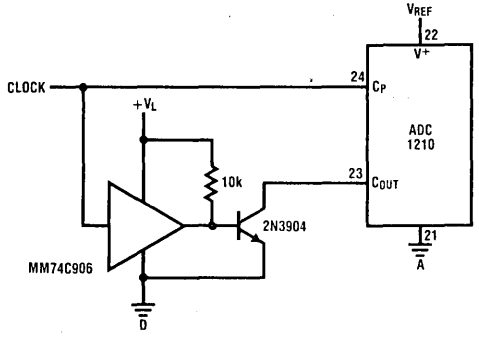


Figure 7. High Speed Conversion Circuit

Testing has demonstrated reliable performance from this circuit beyond the recommended device operating frequency of 65 kHz. However, the AC hysteresis circuit is still a very reliable technique below this clock frequency and, therefore, should be used. Only in applications where the required clock frequency is above 65 kHz should the above-mentioned technique be adopted.

Synchronizing Conversion Start Signal

It is recommended that the $\overline{\text{START CONVERT}}$ input be synchronized to the CLOCK input. This avoids the possibility of the comparator making an error on the first (MSB) decision when the analog input is near ½ scale. There is a chance that energy can be coupled to the comparator from the rising edge of the $\overline{\text{START}}$ signal. If this occurs just before the rising edge of the clock, a wrong MSB decision can be made if time is not allowed for the charge to dissipate. The synchronization circuit in *Figure 8* effectively prevents this from occurring.

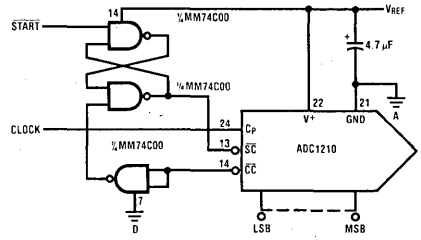


Figure 8. Synchronizing START CONVERT Signal

The circuit operates as follows: initially the latch is in the RESET state and the converter is in the end-of-conversion state ($\overline{\text{CC}}$ output at logic low). The $\overline{\text{START}}$ signal sets the latch and, on the next positive clock transition, initializes all internal registers in the converter. The $\overline{\text{CC}}$ output is set to logic high, presetting the external latch. The latch is held in the "RESET" state during the entire conversion period, effectively preventing a new $\overline{\text{START}}$ signal from interrupting the conversion.

Serial Output

The comparator output does contain the stream of serially converted data with the most significant bit first. However, recognizing the danger of comparator oscillation, there is a potential for the external serial data register to latch a data bit different from that recorded in the SAR due to different logic set-up time requirements. If the ADC1210 accepts an error in any one data bit, the subsequent lower order bits tend to correct for it. On the other hand, an external serial register has no provision for error correction. All subsequent bits following a bit in error will not be valid data.

The 12 bits of information can be shifted out serially by using an MM74C150 digital multiplexer. The circuit is shown in *Figure 9*. This scheme permits valid data to be available at the serial output port as fast as half a clock cycle after the most current decision. The data are thus synchronized to the converter clock (here the serial data are synchronized at the falling edge of the system, CLOCK to avoid clock skew). Obviously, a number of variations can be made to this basic circuit for use with different handshake protocols.

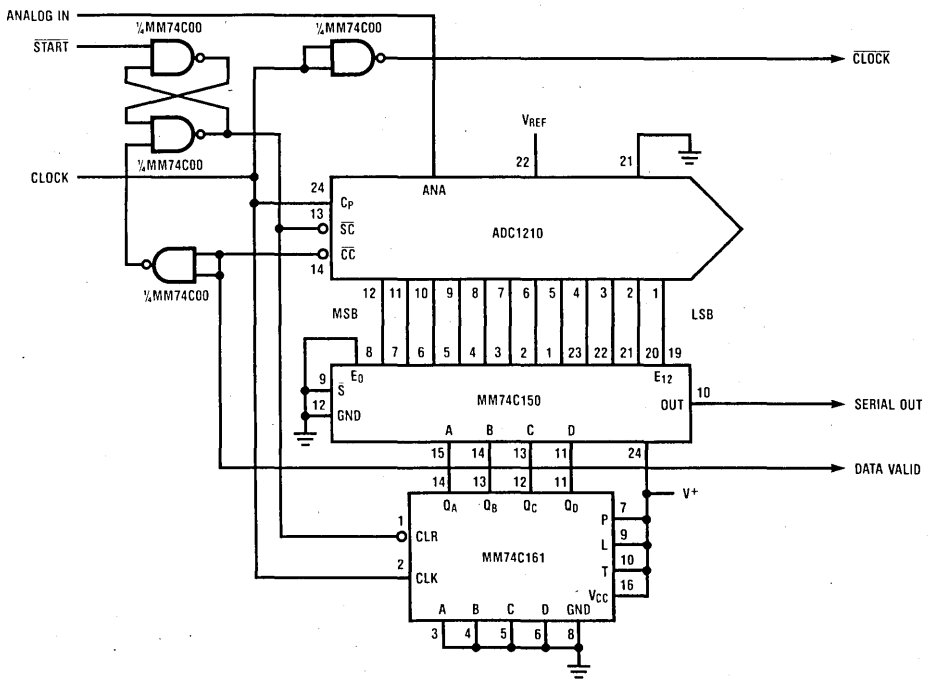


Figure 9. 12-Bit A/D Converter with Serial Output

Applications

Long Time Sample and Hold

The circuit in *Figure 10* is a particularly simple realization of an infinite sample and hold. This scheme requires two low-cost analog sample-and-hold amplifiers to complete the circuit.

The idea is to utilize the digital-loop feedback mechanism of the ADC1210 which, in the normal conversion mode, replicates the analog input voltage at the output of the SAR/D-to-A converter.

The operation of the circuit may be described as follows: During the normal "hold" mode, the replicated analog voltage is buffered straight through the S/H amplifier to the output. Upon an issuance of a $\overline{\text{SAMPLE}}$ signal, this S/H amplifier is placed in the hold mode, holding the voltage until the new analog voltage is valid. The same $\overline{\text{SAMPLE}}$ signal triggers an update to the input sample-and-hold amplifier. The most current analog voltage is captured and held for conversion. This way, the previously determined voltage is held stable at the output during the conversion cycle while the SAR/D-to-A continuously adjust to replicate the new input voltage. At the end of the conversion, the output sample-and-hold amplifier is once again placed in the track mode. The new analog voltage is then regenerated.

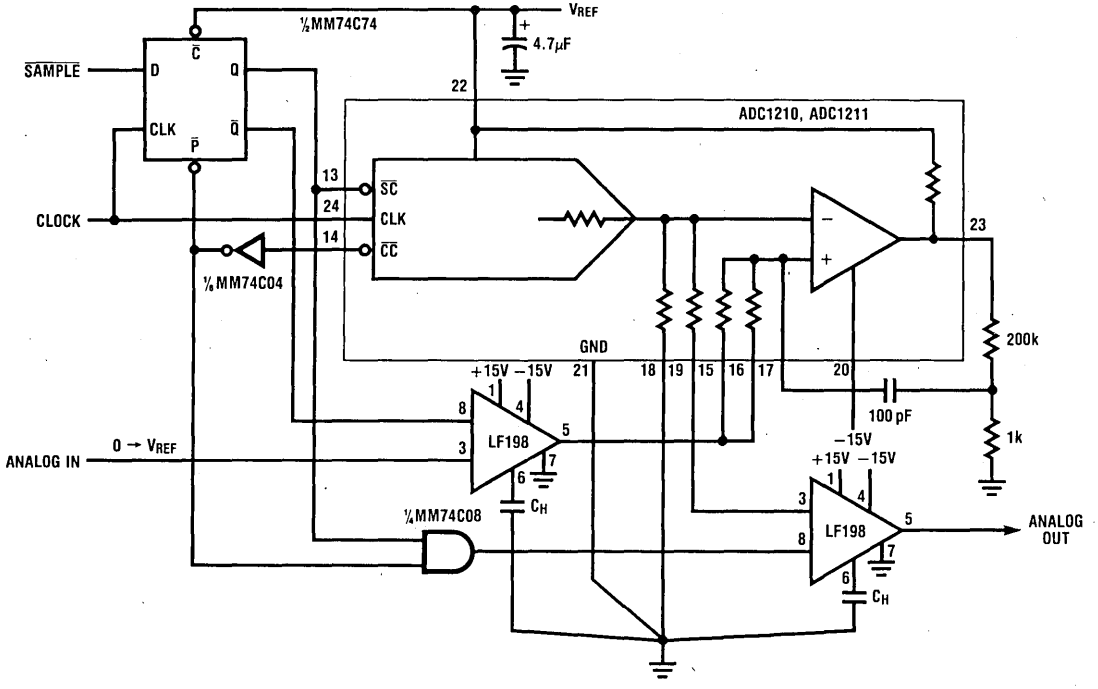


Figure 10. Infinite Sample and Hold Amplifer

An Auto-Ranging Gain-Programmed A/D Converter

The circuit in *Figure 11* shows one possible circuit of an auto-ranging A/D converter. The circuit has a total of 8 gain ranges, with the ranging done in the LH0086 Programmable Gain Amplifier (for differential input, use the LH0084 with ranges of 1, 2, 5, 10 digitally programmed, or pin strap programmed for multiplying factors of 1, 4, and 10). The gain ranges are: 1, 2, 5, 10, 20, 50, 100, and 200. It effectively improves the A/D *resolution* from 12 bits to an equivalent of 19 bits, a dynamic range of better than 100 dB.

The circuit has relatively high speed ranging due to the very fast settling time of the LH0086, typically 5μs for 10V swing, well within the 15μs converter clock period. Thus, the ranging circuit is designed to work off the same clock.

The circuit is designed such that the auto-ranging function is transparent to the user. All command signals into and out of the system are identical to those of an ADC1210 operating alone. The only exception is that the system requires one and one-half clock cycle (mandatory auto range cycle), plus however many ranges it has to scale to (each scale requires one clock period, 7 possible range switching in all) in addition to the basic 13 conversion cycle required by the ADC1210. Therefore, in the best case where no ranging is necessary, the circuit adds 22.5μs to the conversion time; and in the worst case, an additional 128μs.

In the quiescent state where the ADC1210 is in the non-conversion mode, the auto-ranging circuit is free to function normally. Upon an issuance of a $\overline{\text{START}}$ signal, the next clock rising edge puts the circuit in the final auto range cycle before conversion begins. If the need for up-range or down-range is detected, the circuit remains in the auto range mode until all necessary scaling is completed. The control circuit then issues a start conversion signal to the ADC1210. Half a clock cycle later, the ADC1210 begins conversion and suspends the auto-ranging operation until the conversion is completed. At which time the 12-bit converter data plus the 3-bit range data are valid for further processing.

This design is suitable for applications in data-acquisition systems or portable instruments, particularly where low power is an important consideration. Other variations from this basic scheme can be realized depending on the user's requirements.

Summary

The ADC1210 is a low-cost, medium-speed CMOS analog-to-digital converter with 12-bit resolution and linearity. It has wide supply range and flexible configuration to allow varied applications such as field instruments and sampled data systems.

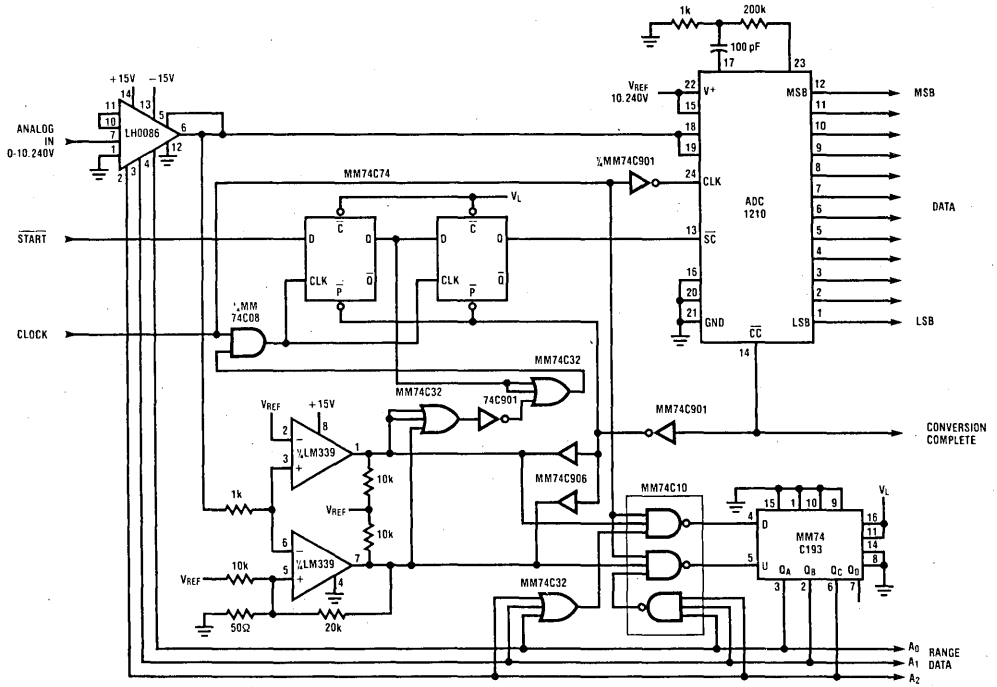


Figure 11. Auto Gain Ranging A/D Converter

LH0024 and LH0032 High Speed Op Amp Applications

National Semiconductor
Application Note 253
James Wong

Introduction

The LH0024 and LH0032 are very high speed general purpose operational amplifiers exhibiting 70 MHz bandwidths, 500 V/μs slew rates and 100 to 300 nanosecond settling time to 0.1%. The LH0032 has the added advantage of FET input characteristics. Both, however, can drive loads with peak currents of 100 milli-amperes (mA). The op amps are stable without external compensation when operating at closed-loop gains of more than 100. Both are constructed with thick film hybrid technology and are actively trimmed for consistent device performance. Table I summarizes the typical performance data for these op amps. Additional information may be obtained from the respective data sheets.

This note is divided into three parts, with the first giving a general description of the circuit topology of each op amp. In the following section, several high performance applications are discussed. Finally, the last section consolidates all application techniques into an integral design approach, much of which is applicable to any high frequency circuit.

LH0024 Circuit Description

The LH0024 contains two gain stages: One is a differential NPN pair and the other is a single-ended PNP stage. The complete schematic is shown in *Figure 1*.

The input stage differential pair, Q8 and Q9, is biased at 6 mA by a current source made up of Q1, Q2, R3, and R5. First stage differential voltage gain is typically 2. Its output is applied differentially from base to emitter of the second stage transistor Q3 which has a gain of about 1,700. This stage also converts the differential signal to a single-ended output.

Current source Q5 and R4 provide 5 mA of DC bias current and a high impedance load to Q3. Overall amplifier gain is the product of the gains of the two stages — 2 × 1700 = 3,400, or 71 dB.

The output complementary pair with class B bias provides a low impedance sourcing and sinking output drive. Although the class B bias contributes a small amount of cross-over distortion, it is barely detectable in closed loop operation.

LH0032 Circuit Description

The LH0032 is a general purpose operational amplifier similar to the LH0024, but with JFET input devices instead of bipolar. As a result, the LH0032 DC input bias and offset currents are three orders of magnitude lower than the LH0024. Its output drive capability is improved due to the use of a larger package with lower thermal resistance, and its class AB output, which is normally biased on, virtually eliminates cross-over distortion.

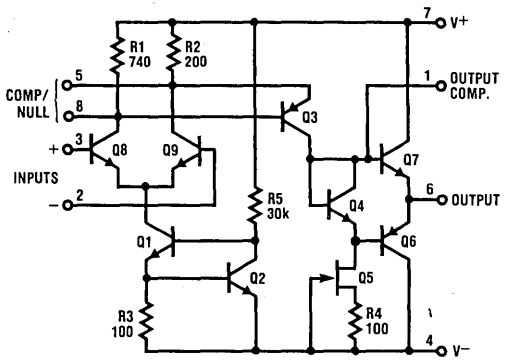


Figure 1. Complete LH0024 Schematic Diagram

Table I. *Typical* Performance Characteristics

Parameter ($T_A = 25°C$)	Conditions	LH0024	LH0032	Units
Input Offset Voltage		2	2	mV
Input Bias Current		15μA	10pA	
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $f = 1kHz$, $R_L = 1k\Omega$	71	70	dB
Slew Rate	$A_V = +1$, $\Delta V_{IN} = 20V$	500	500	V/μs
Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$	8	8	ns
Settling Time to 1.0% of Final Value	$A_V = -1$, $\Delta V_{IN} = 20V$	80	100	ns
Settling Time to 0.1% of Final Value		275	300	ns
Unity Gain Bandwidth	(uncompensated)	70	70	MHz

The improved DC performance is due, in part, to the incorporation of monolithic dual junction FETs in the input stage of the LH0032, providing matched DC tracking and good common-mode input characteristics. First stage operating current is set at 6mA by the current source made up of transistors Q8 and Q9 and resistors R4 and R9, as shown in *Figure 2*. The first stage voltage gain is:

$$A_V \text{ (1st stage)} = g_m R_L = 1.4 \quad (1)$$

Where: $g_m = 3.5\,\text{mmho}$

$R_L = R_1 \parallel (\beta_3 + 1)(r_{e3} + 2R_3)$

The second stage consists of two identical pairs of differential PNP transistors in a cascode configuration. Each side operates at 5mA set by the emitter resistor R3 and the bias of the first stage. The differential amplifier Q3 and Q4 feeds the common-base pair Q5 and Q6 with the base voltage fixed at $V^+ - 1.9$ volts by the diode string Q13-Q15. Thus the collectors of the differential pair Q3 and Q4 are held at one V_{BE} drop more positive than the reference voltage. Any signal amplified by the differential stage produces only a very small change in Q3 and Q4 collector voltage. Consequently, the Miller effect on Q3 and Q4 (base-to-collector capacitances) is virtually eliminated. Using hybrid π model of the transistor, the voltage gain of the cascode stage may be approximated as:

$$A_V \text{ (2nd stage)} = g_{m4} \times R_{eq} \cong 1{,}400 \quad (2)$$

Where: $g_{m4} = \dfrac{5\,\text{mA}}{0.026\text{V}}$

$$R_{eq} = \frac{1}{h_{ob6}} \parallel \frac{1}{h_{oe10}} \parallel (\beta_{11} + 1)(R_L)$$

Notice that the full differential gain is realized with the use of the current mirror Q10 and Q16, which also provides high active load resistance to the PNP cascoded pair, resulting in high amplifier gain.

The collector output of the cascode stage is buffered by a pair of complementary emitter follower transistors, Q11 and Q12. This class AB output stage is normally biased at 1mA by the $1.8V_{BE}$ voltage produced by Q7, R5, and R6. The emitter degeneration resistors provide protection from thermal runaway.

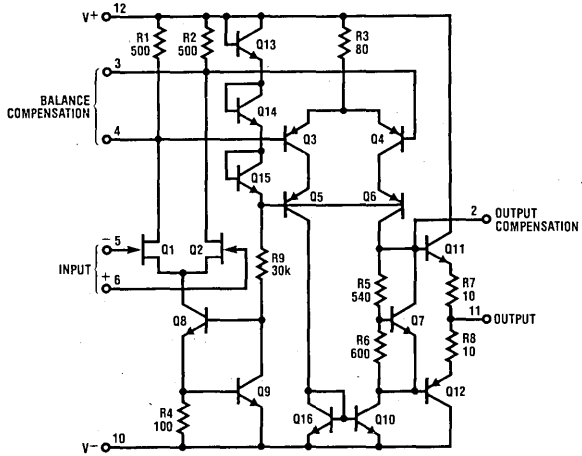


Figure 2. Complete LH0032 Schematic Diagram

Applications of the LH0024/LH0032

Applications of the high speed LH0024 and LH0032 range from video amplifiers to sampling circuits. The applications described below include high speed sample and hold circuits, photo-detector amplifiers, fast settling digital to analog converters and buffered amplifiers.

A High Speed S/H Circuit

High Speed sample-and-hold circuits require high slew rate and fast settling amplifiers. The LH0032 is ideal for these applications. An example is shown in *Figure 3*.

The complementary emitter-follower Q3 and Q4 sources or sinks large peak current to rapidly charge or discharge the hold capacitor during step changes, thus effectively

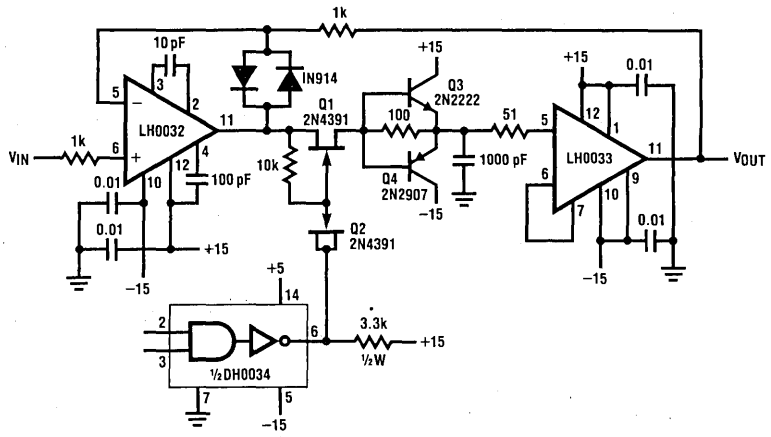


Figure 3. High Speed Sample and Hold Circuit

buffering the FET switch, Q1, whose $r_{D(ON)}$ would otherwise slow the charge time. The LH0033 FET-input amplifier buffers the output signal, providing 100mA drive capability.

The circuit exhibits a 10V acquisition time of 900ns to 0.1% accuracy and a droop rate of only 100μV/ms at 25°C ambient condition. An even faster acquisition time can be obtained using a smaller value hold-capacitor. By decreasing the value from 1000pF to 220pF, the acquisition time improves to 500ns for a 10V step. However, droop rate increases to 500μV/mS.

Fiber Optic Transmitter-Receiver Applications

Many fiber optic applications require analog drivers and receivers operating in the megahertz region where many so-called wide-band op amps simply run out of steam. Packed with 70MHz gain-bandwidth product (unity gain compensated), the LH0032 is quite suitable for optical communication applications up to 3.5MHz. *Figure 4* demonstrates a complete analog transmission system using this device.

The transmitter incorporates the LF356 to drive the light emitter. The LED is normally biased at 50mA operating current. The input is capacitively coupled and ranges from 0 to 5V, modulating the LED current from 0 to 100mA. The circuit can be easily modified to operate from a single +15V power supply. The only requirement is that the amplifier must be biased within the input common mode range.

The receiver circuit uses an LH0032 configured as a transimpedance amplifier. A photodiode with 0.5 amp per watt responsivity such as the Hewlett-Packard type HP5082-4220, generates 50mV signal at the receiver output for 1μW of light input.

Expectedly, the bandwidth of the entire optical link rests on the receiver circuit. Therefore, if the response time is to be optimized, one should reverse bias the photodiode to minimize junction capacitance. As a result, rise time improves more than 2 orders of magnitude. Next, the feedback resistor value should be chosen to be as large as possible in order to maximize sensitivity within the limits of allowable bandwidth degradation. Using 100kΩ feedback resistor, the maximum system bandwidth is 3.5MHz.

Fast Settling 12-Bit D/A Converter

A high resolution, fast-settling DAC can be constructed using the LH0032. Its low input bias current causes no significant DC error in conversion accuracy. Great care must be exercised in circuit layout to assure highest performance. A single point analog ground should be used with the digital ground separated. A complete circuit with 12-bit resolution is shown in *Figure 5*. The converter typically settles to ½LSB in 800ns for a 10V full-scale swing. Similarly, 10-bit or 8-bit resolution DACs may be constructed using the DAC1020 or DAC0808, respectively.

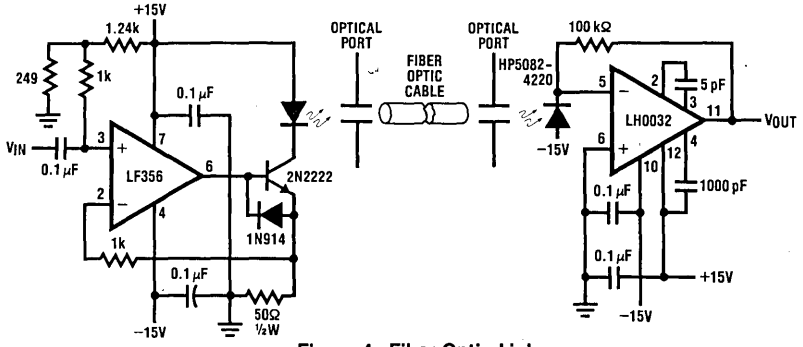


Figure 4. Fiber Optic Link

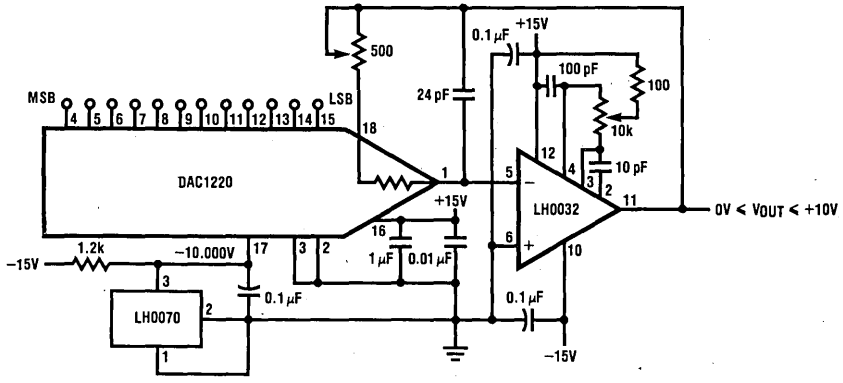


Figure 5. Fast Settling DAC

Buffered Amplifier

Whenever higher output current is required, a buffer amplifier may be added to the loop as shown in *Figure 6*. The LH0033 boosts the output drive capability to ±100mA continuous and ±400mA peak.

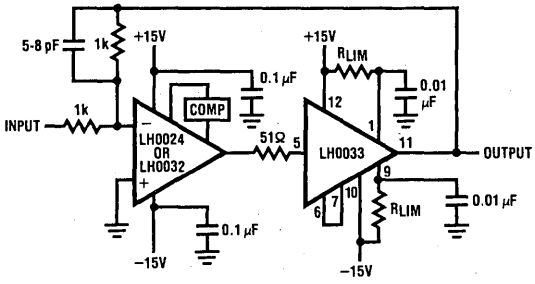


Figure 6. Wide Band Amplifier with 100mA Output Capability

Despite its 100MHz bandwidth, the LH0033 introduces about 15 degrees of phase lag at the LH0032 unity-gain frequency of 70MHz. As a result, phase margin is degraded by the same amount. Slight overcompensation may be required in order to restore adequate phase margin. One way is to increase the feedback capacitor from 5pF to a slightly larger value, 6 to 8pF should be sufficient. If the load is predominantly capacitive, the total phase shift of the buffer stage may exceed 180° and appear as negative impedance seen looking into the input of the buffer. The 51Ω resistor restores some real resistance to alleviate this condition and prevents potential oscillation. In cases where the load capacitance is relatively large, up to 100Ω may be necessary to compensate for it.

Design Considerations

Optimizing LH0024/32 Performance

The LH0024 and LH0032 allow considerable flexibility in designing high performance circuits if care is taken in the way they are used and implemented. Indeed, the printed circuit board layout in high frequency circuits is as important as the design of the hybrid devices themselves.

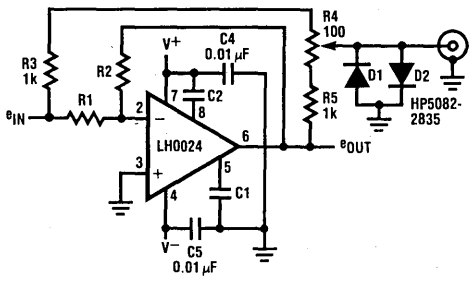
It is good practice to use ground plane PC board design. It provides a low resistance, low inductance path, and reduces stray signal coupling to sensitive circuitry. A double-sided ground plane is usually better and should be considered.

In addition, signal trace connections should be kept as short and wide as possible. Avoid closely-spaced parallel signal traces as signal cross-coupling may occur. Circuit elements should be placed close to the amplifier, particularly critical components that directly affect the amplifier's frequency response, such as compensation capacitors. If at all possible, one should maintain single point ground throughout the circuit to minimize signal phase delay.

Examples of single-sided PC layouts for the LH0024 and LH0032 are shown in *Figure 7* and *Figure 8*, respectively. The layouts include a settling time test circuit, optional inverting or noninverting mode. Note that the summing junction side of the feedback resistor is kept very close to the device pin, thus minimizing lead capacitance. The power supply decoupling capacitors should also be kept close to the device pins, preferably ⅜ of an inch.

Input Guarding and Bootstrapping

In applications where input leakage currents are important, trace guarding, such as used in sample and hold circuits, can improve performance at no additional cost.



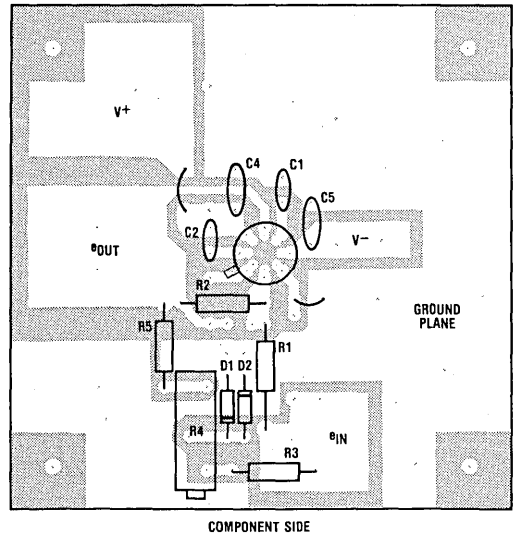


Figure 7. Single-Sided Sample PC Layout for LH0024

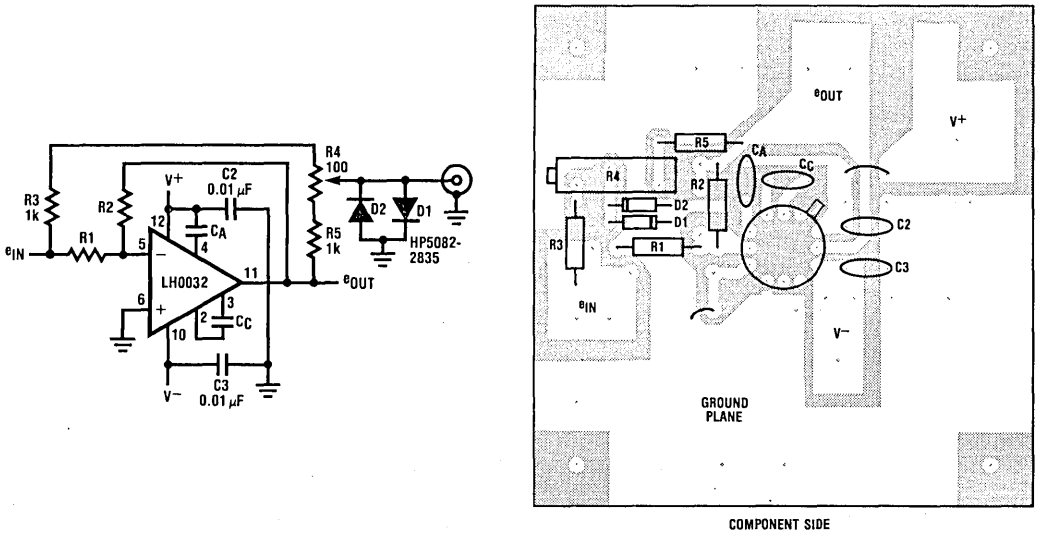


Figure 8. Single-Sided Sample PC Layout for LH0032

The guard conductor serves to intercept leakage currents from inputs to the surrounding circuit. It is most effective when it is driven to the same potential as the guarded circuit. *Figures 9* and *10* show how the technique is implemented in inverting and non-inverting configurations, respectively.

One other benefit of input guarding is the reduction of input stray capacitance effects. A comprehensive discussion of this technique is described in Application Note AN-63.

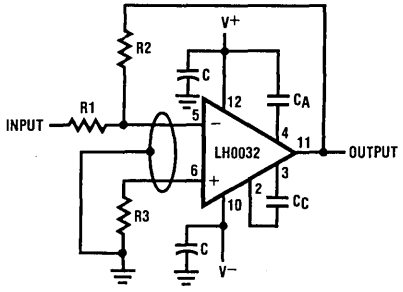


Figure 9. Guarding Inverting Figure Amplifier

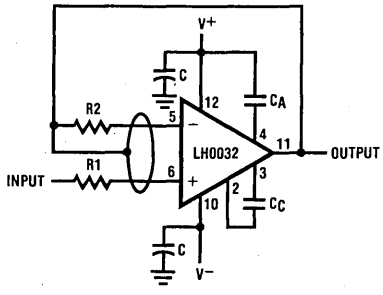


Figure 10. Guarding Non-Inverting Unity Gain Amplifier

Input Capacitance Cancellation

The intrinsic input capacitance of the amplifier cannot be totally eliminated by the input guarding technique. This input capacitance introduces a pole in the amplifier response at the frequency given by:

$$f_P = \frac{1}{2\pi R_S C_{IN}} \quad (3)$$

This pole may become extremely important as, for example, a C_{IN} of 5pF (typical input capacitance of the LH0024 and LH0032) with a 500 ohm effective source resistance creates a pole at about 64 MHz — well before the amplifier's natural frequency response rolls off to unity gain at 70 MHz. If closed-loop gain is unity, more than 135° total phase lag is introduced even before the crossover frequency is reached and will destroy phase margin. Oscillation is certain to occur. The solution is to cancel its effect. As shown in *Figure 11*, the lead capacitor C1 across the feedback resistor is used to introduce a zero in the loop response such that it exactly cancels the pole caused by the input RC network.

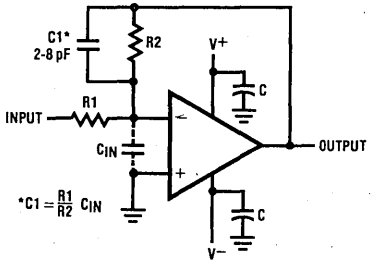


Figure 11. Compensating Amplifier Input Capacitance

Ideally, the ratio of input capacitance C_{IN} to lead capacitor C1 should equal the closed-loop gain of the amplifier. Under this condition, exact pole-zero cancellation is realized.

Note that Equation (3) dictates the use of source resistance values less than 1kΩ in circuits operating at or near unity gain to keep f_P greater than 70MHz.

Frequency Compensation

High-performance wideband op amps such as the LH0024 and LH0032 require external frequency compensation, depending on the closed-loop gain. Optimum AC performance will be affected by a given circuit and its layout. Several compensation techniques are recommended and the best should be selected according to the particular application. Each is discussed in the following sections.

Compensating the LH0024

Table II provides a guide to compensate the LH0024 at several values of closed-loop gain. *Figure 12* shows the basic scheme.

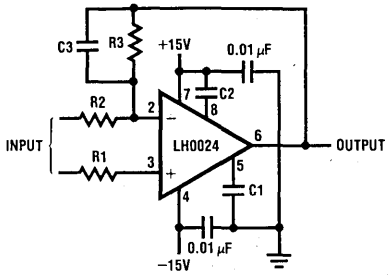


Figure 12. LH0024 Frequency Compensation Circuit

When operating with closed-loop gain of −1, C3 is required and may need slight adjustment to completely cancel the input capacitance of the device, typically 5pF.

Table II

Closed-Loop Gain	C1	C2	C3
100	0	0	0
20	0	0	0
10	0	20pF	1pF
1	30pF	30pF	5pF

An alternate technique for compensation at a closed-loop gain of 1 is to use an input RC lag compensation network as shown in *Figure 13*.

With 1kΩ resistor values in the circuit, R_C and C_C should be 82 ohms and 0.047μF, respectively. The difficulty in using this compensation is its involved calculation and experimenting required in order to find the optimum R_C and C_C values if resistors orther than 1kΩ are used when the above R_C and C_C values are no longer valid and must be redetermined. For this reason, optimum compensation is almost always determined empirically, as were the values given.

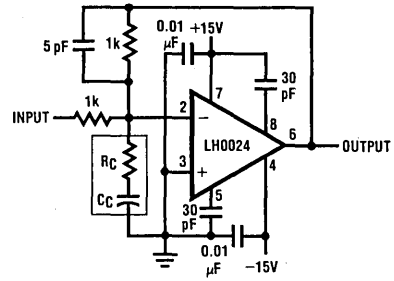


Figure 13. Input RC Lag Compensation Circuit

Compensating the LH0032

With the LH0032, two compensation schemes may be used, depending on the designer's specific needs.

The first technique is shown in *Figure 14*. It offers the best 0.1% settling time for a ±10V square wave input. The compensation capacitors C_C and C_A should be selected from *Figure 15* for various closed-loop gains. *Figure 16* shows how the LH0032 frequency response is modified for different value compensation capacitors.

Although this approach offers the shortest settling time, the falling edge exhibits overshoot up to 30% lasting 200 to 300ns. *Figure 17* shows the typical pulse response.

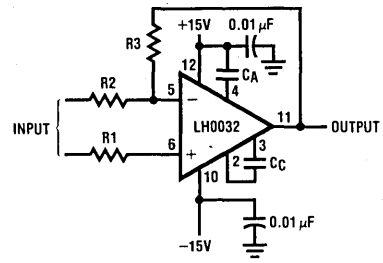


Figure 14. LH0032 Frequency Compensation Circuit

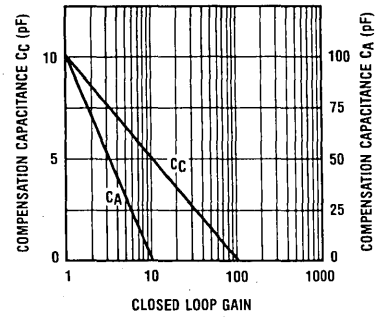


Figure 15. Recommended Value of Compensation Capacitor vs. Closed-Loop Gain for Optimum Settling Time

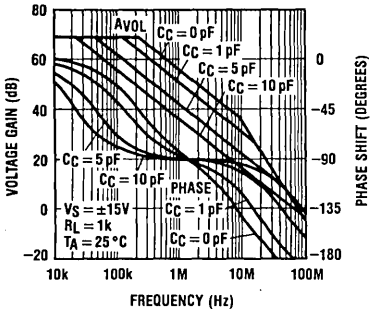


Figure 16. The Effect of Various Compensation Capacitors on LH0032 Open Loop Frequency Response

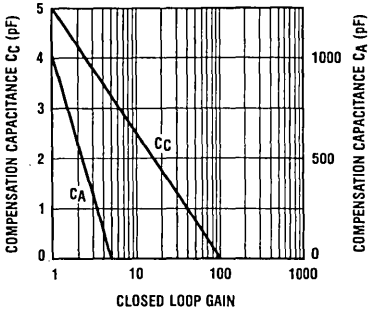


Figure 18. Recommended Value of Compensation Capacitor vs. Closed-Loop Gain for Optimum Slew Rate

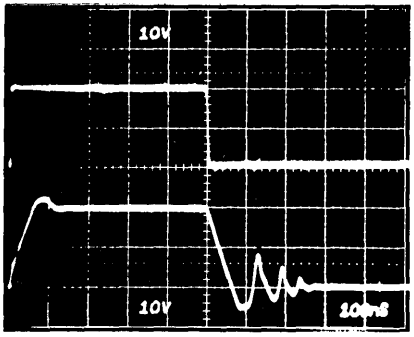


Figure 17. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response: $T_A = 25°C$, $C_C = 10pF$, $C_A = 100pF$

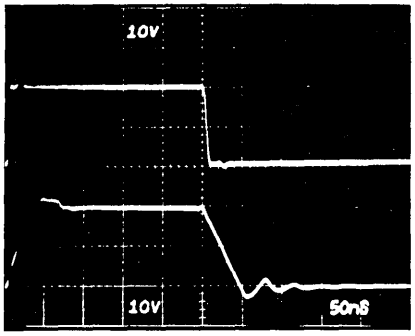


Figure 19. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response: $C_C = 5pF$, $C_A = 1000pF$

If obtaining minimum ringing at the falling edge is the primary objective, a slight modification to the above is recommended. It is based on the same circuit as that of *Figure 14.*

The values of the unity gain compensation capacitors C_C and C_A should be modified to 5pF and 1000pF, respectively. *Figure 18* shows the suitable capacitance to use for various closed-loop gains. The resulting unity gain pulse response waveform is shown in *Figure 19.* The settling time to 1% final value is actually superior to the first method of compensation. However, the LH0032 suffers slow settling thereafter to 0.1% accuracy at the falling edge, and nearly four times as much at the rising edge, compared to the previous scheme. Note, however, that the falling edge ringing is considerably reduced. Furthermore, the slew rate is consistently superior using this compensation because of the smaller value of Miller capacitance C_C required. Typical improvement is as much as 50%. A more detailed discussion of this effect is provided in the Slew Response section of this Application Note.

The second compensation scheme works well with both inverting or non-inverting modes. *Figure 20* shows the circuit schematic, in which a 270 ohm resistor and a 0.01μF capacitor are shunted across the inputs of the device. This lag compensation introduces a zero in the loop modifying the response such that adequate phase margin is preserved at unity gain crossover frequency. Note that the circuit requires no additional compensation.

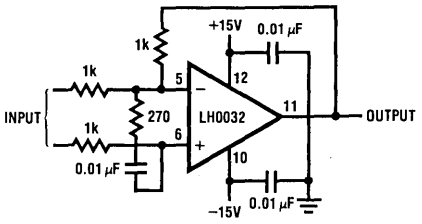
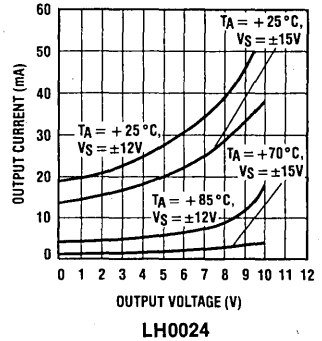


Figure 20. LH0032 Non-Compensated Unity Gain Compensation

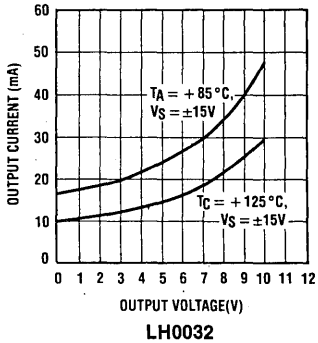
Output Drive Capability

The LH0024 and LH0032 op amps are designed to deliver, but not to exceed, ±100mA peak output current for durations under 1μs at duty cycles under 1%.

The output drive capability of these op amps is limited primarily by device power dissipation. *Figure 21* shows the maximum drive capabilities under various conditions. These limits should be observed. Furthermore, the open loop gain decreases slightly as a result of increased output loading. For this reason, continuous output current should be kept under 50mA.



LH0024



LH0032

Figure 21. Continuous Output Drive Capability

Capacitive Load Compensation

Capacitive loads cause increased phase shifts in such a way that phase margin decreases toward an unstable state and oscillation may result. The cure is to overcompensate the op amp and to isolate the load with a series resistor (100 to 200 ohms) as shown in *Figure 22*. For example, an unterminated coaxial cable presents a capacitive load. Slight overcompensation may be required to maintain stability.

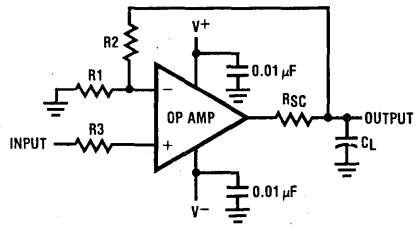


Figure 22. Output Protection when Driving Capacitive Load

Power Dissipation

A simple design rule that is often bent, if not broken, is that relating to power dissipation. The limits for the LH0024 and LH0032 are shown in *Figure 23*. Under no circumstances should these guidelines be exceeded within the temperature range specified. The total power dissipation can be easily calculated from the following equation:

$$P_{Total} = P_Q + P_{Out} \quad (4)$$

Where: P_Q = the quiescent power at a given supply voltage and current as specified by the data sheet, and,

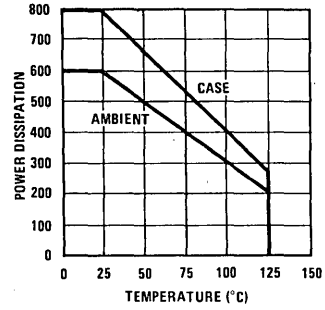
P_{Out} = the drive power dissipated in the device output stage, computed as the net rms collector-emitter voltage of the output transistor times the load current.

Determining power dissipation when driving a capacitive load is more involved. The peak power required to charge or discharge the load capacitor is:

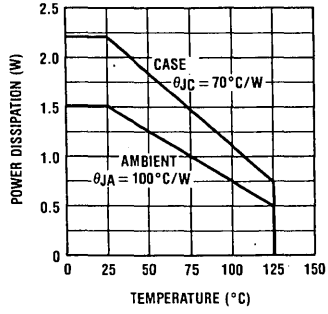
$$P_{Peak} = \frac{C_L (\Delta V)^2}{t} \quad (5)$$

Where: ΔV = the change in voltage across C_L.
$t = t_{Peak}$ charging time into C_L.

Over a full charge and discharge cycle, the power is directly proportional to the frequency of the input pulse waveform. As the pulse repetition frequency increases, so does power dissipation.



LH0024



LH0032

Figure 23. Maximum Power Dissipation

Short Circuit Protection

Since the LH0024 and LH0032 have no internal short circuit protection, their relatively high drive capability can sustain current levels sufficient to destroy the devices if high frequency oscillation is induced. This can occur with a large capacitance load. To design in protection, a current limiting resistor R_{sc} should be inserted at the output of the amplifier inside the feedback loop as shown in *Figure 22*. The value of R_{sc} can be determined from the following equation:

$$R_{sc} = \frac{V^+}{I_{sc}} \quad (6)$$

Where: V^+ is the power supply voltage.

Heat Sinking Considerations

Under severe environmental and electrical operating conditions, a low thermal resistance heat sink should be used to assure safe operation. The following is a list of heat sinks from various sources recommended for the TO-8 case style:

Thermalloy 2240A, 33°C/W

Wakefield 215CB, 30°C/W

IERC, UP-TO8-48CB, 15°C/W

Heat sinks for the TO-5 case style are readily available from many manufacturers. A reasonably priced clip-on unit from Thermalloy, Model 2228B, offers modest thermal resistance of 35°C/W.

Case Grounding

Grounding the case of the device offers improved immunity from circuit cross-talk, but it compromises additional stray capacitance to every device pin (usually 1-2pF). In the rare situation where case grounding is required, slight recompensation may be necessary. However, most applications are not demanding enough to warrant its use.

There are several ways to strap, or ground the case. For the LH0032, the best approach is to solder a small metal washer or a small piece of wire between the base of the device metal can and the base of an unassigned lead post. Dedicating pin 7 of the LH0032 for this purpose is recommended, although any other "no connection" pin is acceptable. High temperature solder should be used to avoid solder reflow during normal assembly operations.

The LH0024 has no unused pins available, and thus is not readily adaptable to case strapping. An alternative approach is to use an electrically conductive heatsink with a PC board-mountable option, such as Thermalloy type 2230C-5.

In all uses of case grounding, be on the lookout for ground-induced noise into the signal path. In short, be sure the ground is a *quiet* ground.

Power Supply Bypass

Power supply pins must be bypassed in all cases to prevent oscillation. A 0.01 to 0.1μF disc or monolithic ceramic capacitor at each supply pin to ground is adequate. The capacitors should be placed no more than ½ inch from the device pins.

Adjustment of Offset Voltages

When required, the offset voltage of the operational amplifiers may be nulled using a balance potentiometer as shown in *Figure 24*. The 100 ohm series resistors prevent any adverse oscillation or malfunction when the pot is shorted to either end of the adjustment range.

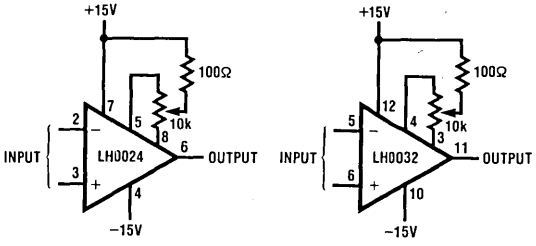


Figure 24. Offset Voltage Adjustment

Slew Response Improvement

Slew rate is the internally limited maximum rate of rise, or fall, at maximum amplifier output swing when driven by a large signal step input. It is primarily limited by the operating current of the input stage. When overdriven by a step function, the input stage operating current charges or discharges the effective circuit capacitance of the second stage. The rate of charge is:

$$\frac{dV}{dt} = \frac{I_{Input\ Stage}}{C_{Node}} \quad (7)$$

In the case of the LH0032, where Miller Compensation is used, the external capacitance adds to the internal circuit capacitance, resulting in reduced slew rate. *Figure 25* illustrates this effect as a function of the capacitance value.

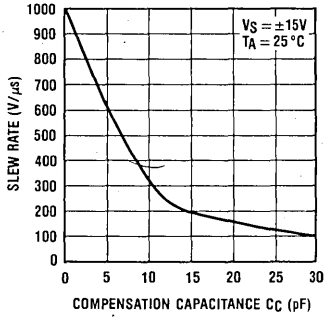


Figure 25. LH0032 Slew Rate vs. Frequency Compensation Capacitance

Figures 26, 27, and *28* demonstrate the rising and falling slew capabilities of the LH0024 and LH0032. Notice the improved slew rate performance of the LH0032 using the alternative compensation technique in *Figure 28* compared to *Figure 27*. The difference is due to the smaller Miller capacitance used in the former.

The LH0024 does not use Miller Compensation, so slew rate is not compromised. Consequently, large signal frequency response is significantly higher than that of the LH0032.

Finally, power supply voltage affects slew rate. As the voltage decreases, input stage operating current decreases accordingly. The net effect is a reduction in the slew rate as the available charging current drops off. *Figure 29* shows the typical slew response of each op amp as a function of supply voltage.

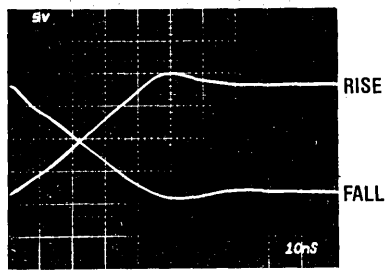


Figure 26. LH0024 Slew Response, Unity Gain Inverting Mode

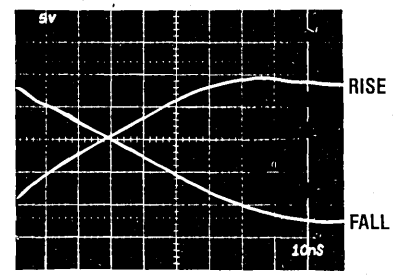


Figure 27. LH0032 Slew Response, Unity Gain Inverting Mode, Standard Compensation ($C_C = 10pF$, $C_A = 100pF$)

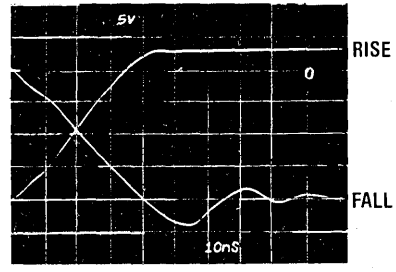


Figure 28. LH0032 Slew Response, Unity Gain Inverting Mode, Improved Compensation ($C_C = 5pF$, $C_A = 1000pF$)

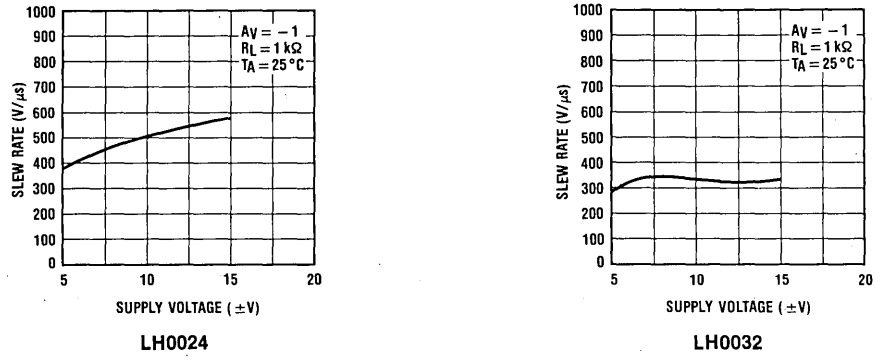


Figure 29. Slew Rate Response as a Function of Supply Voltages

Settling Time

Settling time is the time between the start of a step input to the time it takes the output to settle to within a specified error band of the final voltage. This parameter is heavily influenced by the frequency compensation of the amplifier (degree of damping). Undercompensation results in excessive phase shift, overshoot and ringing, and therefore, a long settling time. Equally poor performance results from overcompensation, which yields an overdamped system, slow decay and, again, a long settling time.

Expectedly, settling time is affected by the loop gain of the amplifier. *Figure 30* illustrates this effect for these two devices.

One of the most demanding applications is driving a capacitive load in a circuit such as a high speed sample-and-hold, where accuracy and fast settling time are both important. Because of the additional phase shift introduced by driving the sampling capacitor, the LH0032 must be recompensated. *Figure 31* presents the optimum compensation to obtain fastest settling time under these conditions.

Conclusion

At first glance, the LH0024 and LH0032 seem harmless enough. A more in-depth look reveals the challenges in applying these high performance op amps. The ultimate capabilities that can be extracted are a direct function of careful engineering. With prudence, these devices are harmless indeed.

Application of these high performance amplifiers requires an understanding of compensation and layout technique. With the information presented in this note, the designer should be able to enjoy the benefits of their superior capabilities.

References:

1. National Semiconductor *Special Functions Databook.*
2. R. K. Underwood, "New Design Techniques For FET Op Amps" National Semiconductor AN-63, March 1972..
3. J. Wong, J. Sherwin, "Applications Of Wide-Band Buffer Amplifiers" National Semiconductor AN-227, October 1979..
4. "LH0082 Optical Communication Receiver" Data Sheet, National Semiconductor Corp..
5. E. Miller, "Introduction to Practical Fiber Optics" National Semiconductor AN-244, May 1980.

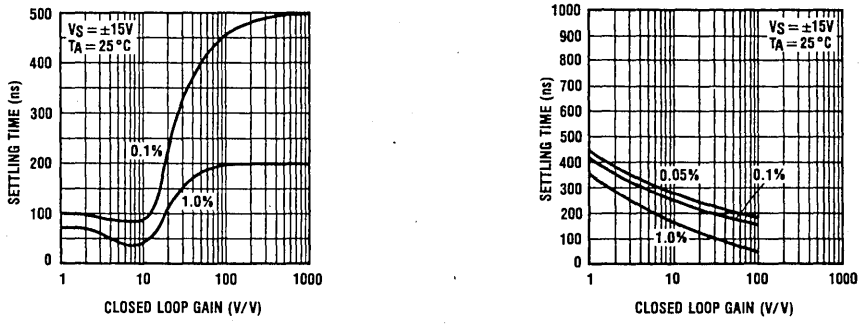


Figure 30. Settling Time vs. Closed-Loop Gain

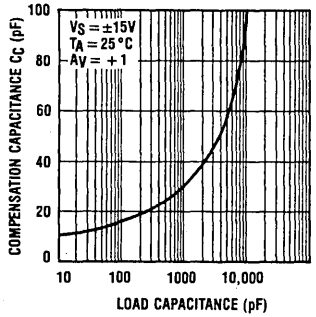


Figure 31. Frequency Compensation vs. Load Capacitance

Low Distortion Wideband Power Op Amp

National Semiconductor
Application Note AN-261
James Wong & Richard Johnson

The LH0101 is a new power operational amplifier capable of delivering a high-current low-distortion output. The device is conservatively rated at 2 amps continuous current. A novel design technique is used to eliminate the crossover distortion often plaguing power op amps. Additional features include a frequency response from DC to greater than 4 MHz. Excellent DC performance is attained by using FET input devices, and the unity gain frequency compensation has been performed internally. Finally, the device is hermetically sealed in a standard 8-pin TO-3 power package.

The initial LH0101 design goal was to develop an easy to use wideband operational amplifier capable of driving a variety of loads. This requirement focused a major portion of the design effort in the power output stage where considerable emphasis was placed on eliminating crossover distortion. Another consideration was to remove the ground connection typically associated with power amplifiers in order to ease the usage with single or dual power supply configurations.

Our discussion is sectioned into three subtopics where the first details the LH0101 internal circuitry, the second presents a variety of user product development/ design precautions, and the third presents typical applications for the LH0101, supported by circuit diagrams.

Table 1. LH0101 Typical Performance Characteristics at 25°C Ambient, ±15 V Supply.

Parameter	Conditions	Value
Output current		2 A
Input offset voltage		5 mV
Input bias current		50 pA
Input offset current		25 pA
Input resistance		$10^{12}\Omega$
Large signal voltage gain		200 V/mV
Output voltage swing	$R_L = 100\Omega$	±12.5 V
	$R_L = 10\Omega$	±11.6 V
	$R_L = 5.0\Omega$	±11 V
Slew rate	$A_V = +1$	10 V/μs
Full power bandwidth	$A_V = +1$, $R_L = 10\Omega$	300 kHz
Small signal rise time	$A_V = +1$, $R_L = 10\Omega$	100 ns
Small signal settling time to 0.01%	$V_{IN} = 10$ V, $A_V = +1$	2 μs
Gain bandwidth		4 MHz
Harmonic distortion	f = 1 kHz, $P_O = 1$ W, $R_L = 10\Omega$, $A_V = +1$	0.005%
	f = 20 kHz, $P_O = 1$ W, $R_L = 10\Omega$, $A_V = +1$	0.05%

Circuit Topology

The LH0101 consists of 3 essential stages, an operational amplifier, a buffer, and a power output stage.

Selection of a BI-FET operational amplifier was prompted by a balance between the desired AC and DC performance. This decision was made in order to take advantage of the high performance BI-FET series' slew rate, settling time, and low bias current characteristics. The added feature of internal frequency compensation aided in making it an ideal amplifier upon which to build.

The zero-crossing distortion associated with high current and high frequency conditions is an age-old problem of class B and class AB power amplifiers. In order to minimize the distortion at crossover, the amplifier must maintain a low output impedance throughout zero crossing. This requires the push-pull output transistors to smoothly alternate current sourcing and sinking duty during the crossover.

To obtain a low output resistance the output stage must constantly remain in the active region. The usual approach is to incorporate a class AB output stage similar to that shown in *Figure 1.* During no load conditions, both output transistors are biased ON thus providing a low output resistance and hence eliminating crossover distortion. Under rated current load conditions, however, a potential source of distortion can develop. Take the case of an output at a positive voltage delivering the rated current to a load. The increased base-to-emitter voltage of the drive transistor tends to bias the bottom transistor OFF.

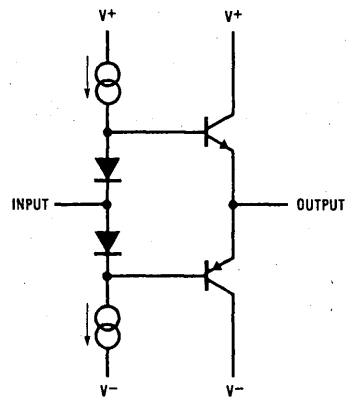


Figure 1. Class AB Output Stage as a Possible Solution to Minimize Distortion

As the output swings negative, crossover distortion can be seen to depend upon how quickly the bottom transistor can turn ON to assume its drive portion of the duty cycle. This condition becomes more acute at higher frequencies.

Of even greater concern is the risk of thermal runaway. An internal rise in temperature decreases transistor junction voltages which in turn increase the collector operating current. Typically emitter degeneration resistors can be used to compensate for this effect, but prove themselves inadequate under rated current load conditions. In order to minimize the junction voltage temperature effect a large resistor value must be selected. At the same time this limits the output drive current and, hence, the output voltage swing. On the other hand, if a small resistor value is selected, the output drive current is maintained but the voltage drop across this small resistance is inadequate to compensate for a decrease in junction voltage. This result brings the problem back to one of thermal runaway and clarifies the shortcomings of *Figure 1.*

Another commonly used technique is a pseudo-class B output stage found in many integrated power op amps, (see *Figure 2*). In this configuration, the limited output swing problem of class AB amplifiers is eliminated. The output swings to within one or two volts of either supply.

The obvious problem with this type of circuit is that it has significant crossover distortion. Distortion occurs when both output transistors are biased completely OFF during zero crossing, thus exhibiting relatively high resistance at the amplifier output. In addition, the minor loop feedback between the base drive of the transistors and the output almost always induces an abrupt change in the response. This further aggravates the amplifier distortion.

The new op amp successfully combines both techniques to achieve remarkably smooth crossover transitions under most demanding conditions. The complete schematic is shown in *Figure 3.*

The buffer stage, which consists of transistors Q3, Q5, Q10, and Q11 is a current amplifier with unity voltage gain. Connected as a class AB amplifier, its function is to provide distortion-free drive during zero crossing. Bandwidth is in excess of 50 MHz to ensure no bandwidth-induced distortion.

The buffer stage output is current limited by transistors Q7 and Q8 to no more than 50 mA. However, the power stage transistors Q1 and Q2 are designed to turn ON as the load current reaches about 25 mA. Any additional current demanded is sustained by these two output transistors right up to the rated output limit. Thus, the reserve drive of the buffer stage is used only to "smooth" the turn-on delay of the output Darlington transistors.

Q6 and Q9 base-to-emitter junctions are used as current limit sense to protect the output stage. Current sense resistors connected between the supply pins and the SC pins program the limit threshold. In operation, an approximate 0.6 volt differential turns ON either transistor Q6 or Q9, which in turn drives Q12 and Q4 respectively, starving any excess base current from driving the output beyond the preset limit.

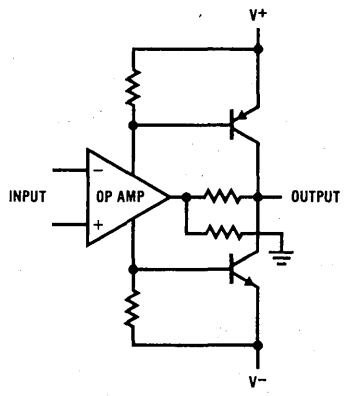


Figure 2. Class B Output Stage

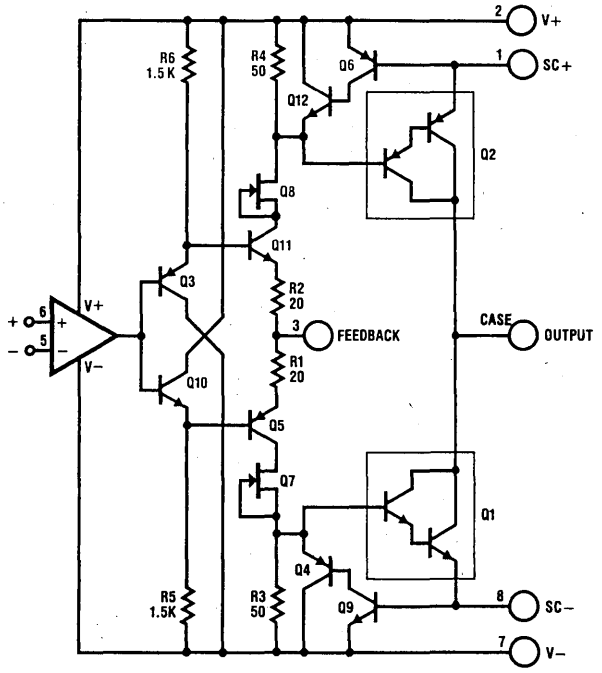


Figure 3. LH0101 Complete Schematic

Result

The performance of the LH0101 is best demonstrated in the following photographs. *Figure 4* shows the large signal slew response of the LH0101 into a 10Ω load. No crossover distortion is evident.

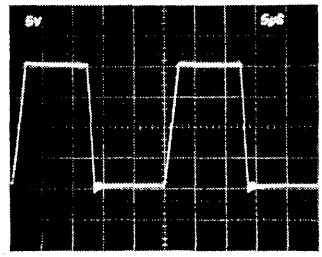


Figure 4. Large Signal Pulse Response, 10Ω Load

Generally, crossover distortion occurs within a small region near zero crossing. In order to amplify its effect, a signal of small amplitude is used. *Figures 5* and *6* show a signal amplitude of 2 volts peak, and loads of 10Ω and 1Ω respectively. Notice that a slight distortion is observed in *Figure 6*, but only under the extreme condition imposed by the 1Ω load!

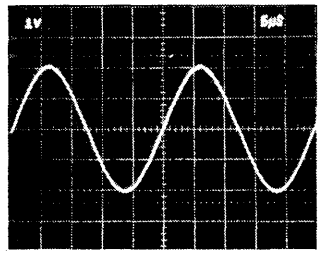


Figure 5. Small Signal Response, 10Ω Load

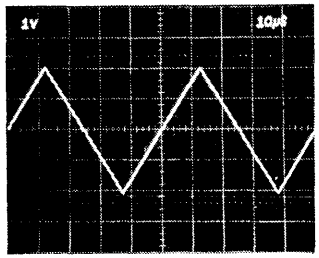


Figure 6. Small Signal Triangular Wave Response, 1Ω Load

Design Precautions

Circuit Layout Considerations

In high power applications, one must pay close attention to the trace connections in which high current is carried. Critical connections should be short to minimize line drop. For example, a 10mΩ PC trace carrying 2 amps develops 20mV of error voltage. It is important to be aware of where this error is generated and how it impacts accuracy.

Ground connections are probably the most important, if not the most troublesome. Not only can they contribute to circuit error, but in many situations the circuit can become unstable if the layout induces excessive phase error. *Figure 7* shows one correct technique for circuit grounding. The heavy lines represent high current paths. The analog signal ground is returned to the supply common.

Output Current Limit

As described in the previous section, current sense resistors may be inserted between the supply pins and the SC pins to limit excessive load currents. A voltage of 0.6 volt developed across the sense resistor triggers the limiting circuit. *Figure 8* illustrates the usage.

In cases where the chosen R_{SC} is small (<1Ω), the contact resistances from solder connections and socket ohmic contacts become important and must not be overlooked. A good solder joint typically exhibits 5mΩ of resistance and socket contacts have about 10mΩ. Even interconnecting traces will become significant if they are long.

Consider the circuit in *Figure 8;* a pair of good solder joints on the 0.3Ω current sense resistors contribute more than 3% error. Also, one can expect the current sense transistor threshold to vary as much as 10% from device to device. Furthermore, this threshold has a temperature coefficient of −2mV/°C. In summary, the expected accuracy is on the order of 20 to 25% under all operating conditions.

When designing the current limit, the threshold should not be set too close to the worst case peak current under any normal operating conditions. Signal distortion will occur even if the threshold is intermittently exceeded for a very short duration. In the worst instance, the circuit can trigger spurious oscillation, such as in the case of driving a capacitive load during transient conditions. These occurrences are very real in nearly all op amps having similar current sense circuits. Although the current limit circuit has high enough gain to produce a sharp response, it is a good idea to allow a 20% margin above the worst case operating condition.

Safe Operating Conditions

In order to preserve the reliable performance of the LH0101, the device must not operate beyond the boundary defined in the Safe Operating Area curve in the data sheet. Because of its importance, it has been reproduced in *Figure 9.*

Power Dissipation Considerations

Probably the single most important gauge of reliability is the operating temperature of this device. The derating curve, which has again been reproduced in *Figure 10,* must be followed faithfully. Similar to the Safe Operating Area curve, under no circumstances should the boundary be exceeded.

The curves relate operating and junction temperature, power dissipation and thermal resistance. The general relationship is expressed as follows:

$$P_{DISS} = \frac{T_{J(MAX)} - T_{A(MAX)}}{R_{\theta JC} + R_{\theta CS} + R_{\theta SA}} \quad (1)$$

where: P_{DISS} = the power dissipated by the device in watts.

$T_{J(MAX)}$ = the maximum junction temperature allowed, for the LH0101, $T_{J(MAX)} = 150°C$

$T_{A(MAX)}$ = the maximum ambient temperature in °C under which the device must operate.

$R_{\theta JC}$ = thermal resistance from the junction to case in °C/W, for the LH0101, $R_{\theta JC} = 2.5°C/W$.

$R_{\theta CS}$ = thermal resistance from case to surface of heat sink in °C/W.

$R_{\theta SA}$ = thermal resistance from heat sink to free air ambient in °C/W.

In simple terms, the expression is a measure of how well the internally generated heat is removed such that the power dissipated will not give rise to a maximum permissible junction temperature of 150°C. Thus, the sum of all the thermal resistance represents the thermal efficiency of the mechanical design. The lower the sum, the more efficient the thermal conductivity.

In a typical design, first and foremost is to calculate the maximum power dissipation that the device is designed to handle. There are two components, which are related by the following equation:

$$P_{DISS} = P_Q + P_O \quad (2)$$

The first part of the equation is the quiescent power at which the device operates under no load. The second term is the power dissipated by the output transistors due to the load. This is calculated as the average voltage difference between the supply voltage and the output voltage multiplied by the maximum rms load current the amplifier is required to deliver.

Once the power dissipation is calculated, the next step is to determine the maximum ambient temperature in which the device must operate.

To complete the thermal design, all contributions of thermal resistances must be summed per equation (1) above. First, the junction-to-case thermal resistance for the LH0101 is given in the data sheet; it is typically 2.5°C/W.

The metal case of the LH0101 is electrically connected to the output of the amplifier. Unless the application permits direct mounting to a heat sink, a sheet of insulation should be sandwiched between the case and the mounting surface for isolation purposes. Many types of insulators are available. The most popular of these is mica film. Its thermal resistance is listed in Table 2 along with other types.

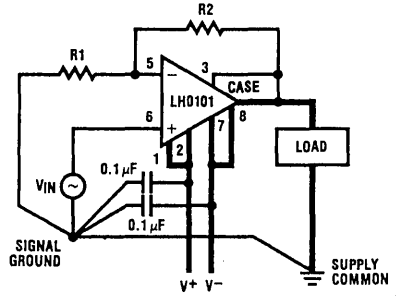


Figure 7. Proper Supply Connection

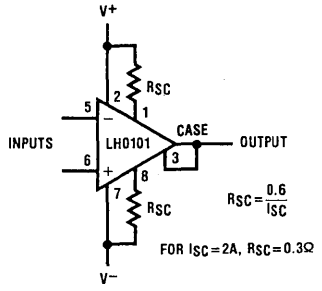


Figure 8. Current Limit Protection

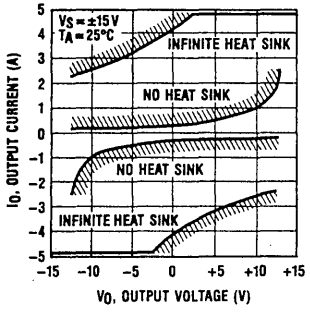


Figure 9. Safe Operating Area

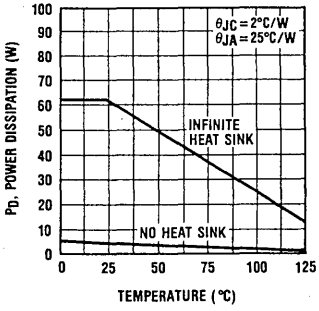


Figure 10. Power Derating Curve

Table 2. Thermal Resistance[1]

Insulator Material Type	W/O Thermal Joint Compound	W/ Thermal Joint Compound	Sources
Mica	1.3°C/W @ 0.003″ thick	0.25°C/W	Thermalloy Inc.
	1.2°C/W @ 0.002″ thick	0.33°C/W	Keystone Electronics Mod. #4658
Thermalfilm I[2]	1.5°C/W @ 0.002″ thick	0.52°C/W	Thermalloy Inc.
Aluminum Oxide[2]	1.0°C/W @ 0.062°C	0.3°C/W	
Beryllium Oxide[2-3]	0.6°C/W @ 0.062″ thick	0.15°C/W	
Insul-Cote[2]	0.5°C/W @ 0.002″ thick		Thermalloy Inc.

[1] Mounting bolts torqued to 6 oz.-in.

[2] Consult manufacturer on availability for 8-lead TO-3 package style

[3] Particle, dust, or fumes present health hazards when inhaled. Grinding, sanding, and pulverizing the material should be avoided.

In critical applications, thermal-joint compound should be used to maximize heat transfer across the case to the heatsink. With air being a poor heat conduction medium, the use of thermal joint compound eliminates air gaps between mounting surfaces, thus providing more than 3 times improvement in thermal efficiency over those cases without.

The remaining unknown, $R_{\theta SA}$, can now be determined from the proper selection of the heat sink. By itself, that is, with no heat sink, the TO-3 case has a junction-to-ambient thermal resistance ($R_{\theta JA}$ or θ_{JA}) of about 25°C/W. Consequently, a heatsink is almost always required in applications involving significant power. Most heat sink manufacturers specify the mounting-surface to ambient thermal resistance $R_{\theta SA}$. In a nutshell, the heatsink is selected such that the right hand side of equation (1) is equal to or greater than the left hand side, or total power dissipation. It is good engineering practice to allow at least a 10% safety margin.

Design Considerations Driving Inductive Load

The LH0101 is suitable for driving most inductive loads including voice-coils and motors. However, in many situations the device should be protected from the harmful effects of energy stored in the inductor. Such a condition exists when power is removed from the circuit at an instant when a high current is flowing through the inductor. A back-emf may have energy high enough to forward bias internal junctions at a current density level sufficient to destroy the device. *Figure 11* illustrates a simple way to prevent this.

Theoretically, an inductive load does not cause amplifier loop instability. However, if the circuit Q is high enough and stray capacitances are within a critical range, the load circuit can break out into oscillation. A series RC damping circuit of 10Ω and a 0.01μF capacitor across the inductor as shown in *Figure 12* usually alleviates the problem.

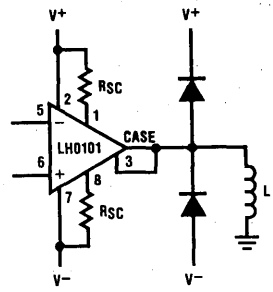


Figure 11. Back EMF Suppression Technique

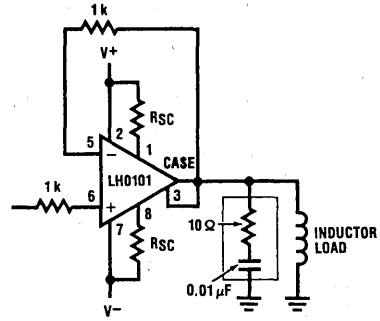


Figure 12. RC Damping to Compensate Inductor Load

In some applications where it is desirable to prevent power-on surges from actuating the load, for example a motor valve actuator or a disk drive read/write head servo loop, the same RC damping circuit provides an alternate conductive path to suppress surge current.

Design Considerations Driving Capacitor Load

Capacitive loads tend to create an unwanted pole at the tail end of the frequency response where the open loop gain approaches unity gain frequency. The effect is a net reduction of phase margin. For example, a 550pF load capacitor reduces the phase margin of the amplifier from a no load of 58° to 45°. A 1000pF capacitor pushes it down to 40°. With a large 0.01μF capacitor, the amplifier has a mere 22° phase margin. The latter cases are susceptible to oscillation. *Figure 13* shows a compensation technique to restore stability. The value of the lead capacitor C1 should be such that the capacitive reactance is one-fifth the resistance of R2 at the unity-gain crossover frequency of the amplifier, or 4MHz.

It is interesting to note that there is a critical value for the load capacitor above which oscillation cannot occur. That value is approximately 0.1μF. Under such a condition, the time constant is so large that the heavy damping effectively suppresses any chance for the circuit to oscillate.

Typical Applications

CRT Yoke Driver

One of the most natural applications for the LH0101 op amp is the deflection yoke driver for high resolution CRTs. The low distortion characteristics allow virtually unrestricted use in any circuit configuration. A typical design is shown in *Figure 14*.

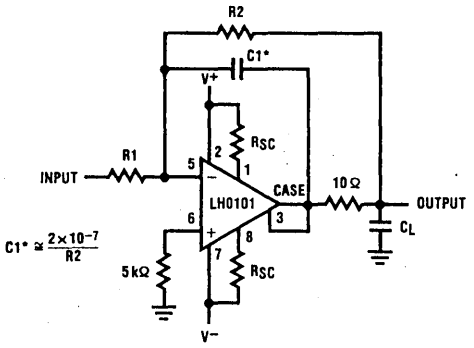


Figure 13. Compensation for Capacitance Load

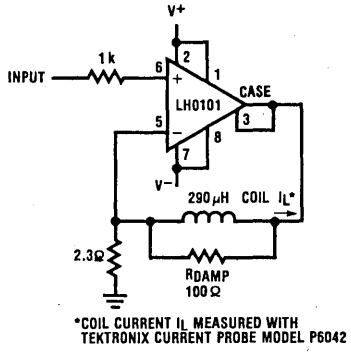


Figure 14. CRT Yoke Driver Circuit

A 500 mV peak-to-peak triangular waveform about ground is input to the amplifier, giving rise to a 100 mA peak current to the inductor. As shown in *Figures 15* and *16*, the responses were recorded at 60 Hz and 20 kHz respectively. At higher frequencies, R_{DAMP} becomes important. The value should be selected to yield the cleanest waveform.

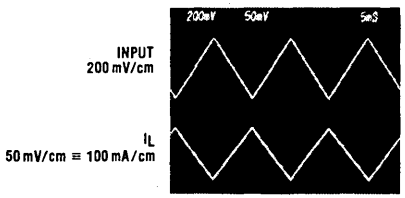


Figure 15. 60 Hz Current Drive Waveform of CRT Deflection Coil

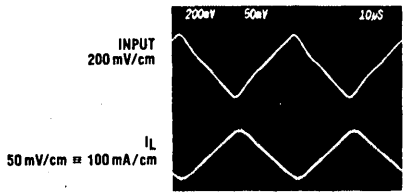


Figure 16. 20 kHz Current Drive Waveform of CRT Deflection Coil

Servo Motor Amplifier

A typical motor driver circuit is shown in *Figure 17*. The amplifier will deliver the rated current into the motor. Again, care should be taken to keep power dissipation within the permitted level.

A variation of the same servo design is shown in *Figure 18*. This precision speed regulation circuit employs rate feedback for constant motor current at a given input voltage.

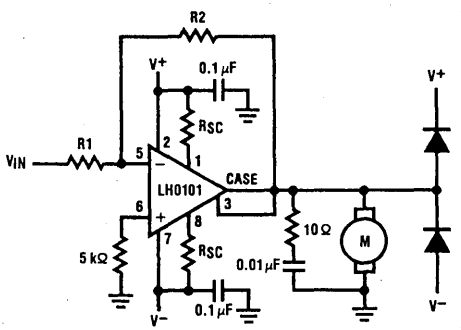


Figure 17. Servo Motor Amplifier

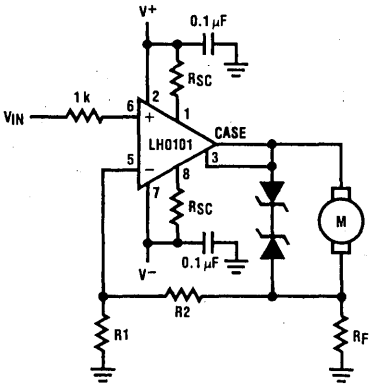


Figure 18. Rate Feedback Servo Motor Amplifer

Digitally Programmable Power Source

Designing precision voltage and current sources is made simple using the LH0101. Adding a digital-to-analog converter provides a tremendous amount of flexibility in speed and control. Applications range from DC precision power supplies to sophisticated programmable waveform generators. The design of the voltage source is relatively straightforward, whereas the programmable current source is a bit more involved. Such a circuit is shown in *Figure 19*. The DAC is configured to operated in a bipolar mode with an output range of ±10.000 V. With 12 bits, the DAC outputs an equivalent of 4.88 mV per bit-weight. Consequently, the resolution at the current source is 0.488 μA/bit.

The output sources and sinks current only to ground referenced loads. A negative full-scale code (all digital inputs low) effects a negative (source) 1 amp current output. A zero scale (MSB low and all other bits high) gives zero current. And a positive full scale code (all digital inputs high) forces a positive (sink) 1 amp current at the output.

The versatility of this circuit configuration is not without limitation. Because the output voltage is dependent upon the ground referred load, one must be aware of the potentially destructive power dissipation level the LH0101 must sustain. For example, 1 amp current into a 5Ω grounded loaded generates 10 watts of power in the amplifier. This level is high enough to destroy the device unless an appropriate heat sink is used to keep the device junction temperature from exceeding the 150°C limit.

Coaxial Cable Driver

The LH0101 makes an ideal cable driver of any type. It has adequate bandwidth for most audio and sub-video applications. The high current, distortion free output can easily interface any termination required. Large line capacitance does not present a problem for the LH0101. It has adequate reserve current capability to charge the capacitance without seriously degrading bandwidth. However, current limit protection against cable shorts is recommended. A typical interface circuit is shown in *Figure 20*. The op amp can drive up to 6 coaxial lines without the use of a heat sink.

Low Distortion Audio Amplifier

At this juncture, it would be of great interest to see how well the LH0101 performs in the audio high fidelity arena. The intent here is not to set a new standard but merely using the stringent requirements of the audio specifications as an ideal yardstick for comparison.

The complete design is illustrated in *Figure 21*. The circuit is configured as a bridge amplifier to maximize available output power for a given set of supply voltages.

The result is an impressive set of specifications summarized in Table 3. Although not earth-shaking, 0.14% total harmonic distortion at the rated 40 watt output, within the full audio frequency spectrum, is very respectable.

Transient slew rate of greater than 10 V/μs extends the full power bandwidth to beyond 200 kHz, and the distortion response is plotted over the entire audio spectrum in *Figure 22*. This would satisfy all but a handful of audio purists.

About the only difficulty encountered was finding a heat sink that was good enough for convection cooling. By following the previous section on Power Dissipation Considerations, the heat sink thermal resistance required is a maximum of 3.5°C/W at an ambient temperature of 25°C. The calculation included the use of mica insulator and liberal use of thermal-coat compound. As it turned out, a large extruded heat sink with fins similar to the Thermalloy type 6141 did an excellent job of keeping the junctions cool.

Table 3. Bridge Audio Amplifier Specifications

A_V (Voltage Gain)	3
Z_{IN} (Input Impedance)	10 kΩ
I_q (Quiescent Current)	60 mA
P_O (Output Power)	40 Watts into 8Ω
—RMS Continuous 20 Hz-20 kHz	28 Watts into 16Ω
Full Power Bandwidth	DC to > 100 kHz
THD (Total Harmonic Distortion)	
1 W 20-20,000 Hz	< 0.8%
40 W 20-20,000 Hz	< 0.15%
IMD (Intermodulation Distortion)	
1 W 60 Hz/100 kHz 4:1	0.01%
40 W 60 Hz/100 kHz 4:1	0.002%
Peak Output Current	3.125 A into 8Ω
Supply Voltage	±18 V
Maximum Output Voltage Swing	21.2 V RMS
	30 V Peak

References

1. National Semiconductor, *Special Functions Databook.*
2. National Semiconductor, *Linear Applications Handbook.*
3. J. Wong, J. Sherwin, "Applications of Wide-Band Buffer Amplifier", National Semiconductor AN-227, October 1979.
4. National Semiconductor "LH0101 Power Operational Amplifier" data sheet.

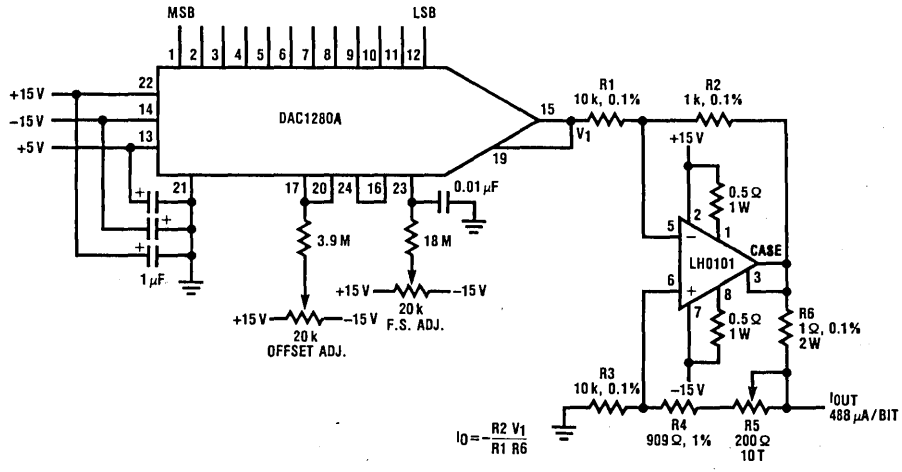


Figure 19. Digitally Progammable Current Source

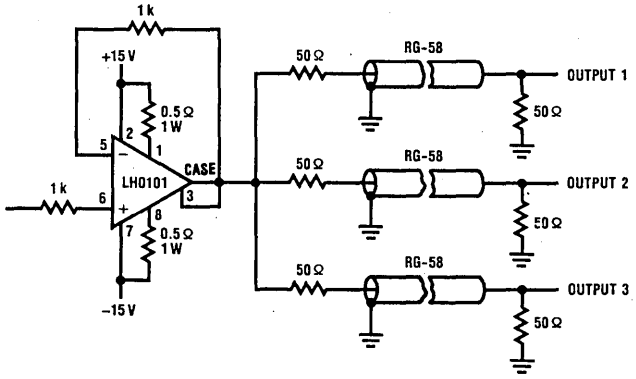
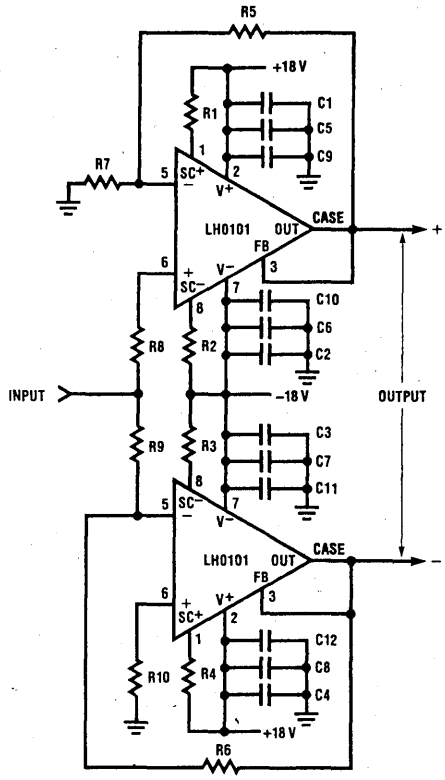


Figure 20. Multi-Line Coaxial Cable Driver



R1-R4	CURRENT LIMIT RESISTOR	0.15 Ω 2 W
R5	FEEDBACK RESISTOR	5 kΩ
R6	FEEDBACK RESISTOR	15 kΩ
R7-R10	INPUT RESISTORS	10 kΩ
C1-C4	BYPASS CAPACITORS	47 μF 25 V ELECTROLYTIC
C5-C8	BYPASS CAPACITORS	10 μF 25 V TANTALUM
C9-C12	BYPASS CAPACITORS	0.1 μF 25V CERAMIC

Figure 21. LH0101 Bridge Audio Power Amplifier

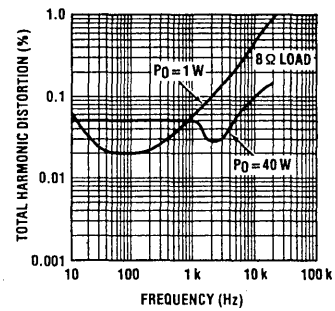


Figure 22. Total Harmonic Distortion vs. Frequency of Bridge Power Amplifier

MOS Clock Drivers

National Semiconductor
MOS Brief 9
John Vennard

How many MOS devices can a clock driver operate? There is no hard and fast answer. Fanout is bounded by the driver's current and power ratings, but can vary greatly with drive requirements and with the way the driver itself is driven by the clock signal source.

Any of the drivers in the table might clock an MOS shift-register string with thousands of stages, for instance, but if that were the only consideration we wouldn't be producing a variety of types. All the drivers have the same basic function—translating a bipolar clock signal to MOS voltage levels and boosting the output current. They have similar output stages, whose operation was detailed in AN-18, "MOS Clock Driver."

What makes them tick differently is their input stages. The MH0007 includes an input AND gate and can be coupled directly to a TTL or DTL gate. The MH0009 is directly or capacitively coupled to a TTL line driver that provides at least 20 mA. To work at its full speed, the MH0012 requires direct-coupled, opposite phase inputs from a TTL driver. And the MH0013 is capacitively coupled to a TTL driver.

The MH0013 offers high fanout at lowest cost. It is most efficient because it does not have a built-in level shifter and the output duty cycle is lower than the input duty cycle. Essentially, it is the MH0009 without the Q1-Q2 input stages seen in Figure 1. However, the MH0013's output pulse width depends on the input drive circuitry rather than the input pulse timing. This is also true of the MH0009 when it is capacitive coupled.

When it is direct-coupled as shown in Figure 2 (most people use it capacitive coupled), the MH0009 will follow the input. That is, the driver output will remain at the MOS "1" level (near V2) for as long as the input is at the TTL "1" level. The output will be MOS "0" (near V3) while the input is at TTL "0". The MH0007 and MH0012 do the same.

In contrast, the MH0013 (or an MH0009 capacitively coupled) as shown in Figure 3 will produce an output MOS "1" level pulse during the period following the bipolar logic transition from the TTL "0" state to the "1" state. At all other times, the output will remain at the MOS "0" level. The width of the "1" output pulse depends on the cur-

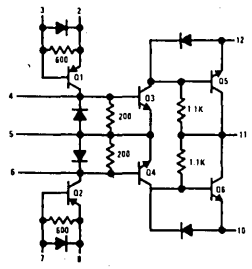


FIGURE 1. MH0009 Dual MOS Clock Driver

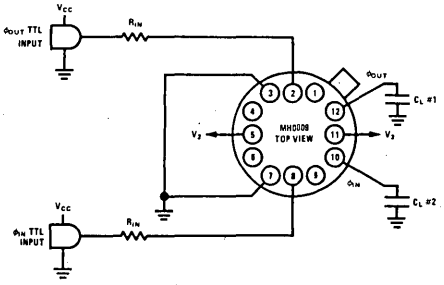


FIGURE 2. Directly Coupled Dual Driver

Characteristics of National MOS Clock Drivers

TYPE	PACKAGE	OUTPUT PHASES	INPUT COUPLING	INPUT LEVEL TRANSLATOR	MAX REP RATE—MHz	MAX OUTPUT SWING—V	I_{OUT}—mA	P_{MAX}—mW @25°C/@70°C	P_{OFF} mW
MH0007	TO-5	1	dc	Yes	5	30	±500	800/600	5
MH0009	TO-8	2	dc or Cap	Yes	3	30	±500	1500/1000	0
MH0012	TO-8	1	dc	Yes	10	30	±1000	1500/1000	20
MH0013	TO-8	2	Cap	No	5	30	±500	1500/1000	0

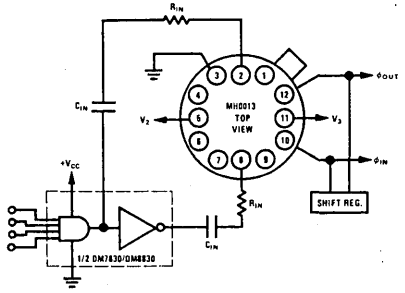


FIGURE 3. Capacitively Coupled Dual Driver

rent available from the TTL driver and the input capacitor (see Figure 4):

$$P.W. \alpha C_{IN} \times V_{drive}/I_{drive}$$

As soon as the input rises about 0.5V, the output is driven to the MOS "1" level (V2). The output returns to the MOS "0" level (V3) when the input capacitor charges.

Capacitive coupling from the TTL driver to the MH0013 helps cut system power consumption and cost to the bone when used with other low duty cycle techniques. Low duty cycle driver efficiency is discussed in AN-18 and low frequency memory operation to reduce system power is discussed in AN-19, "Low Power MOS."

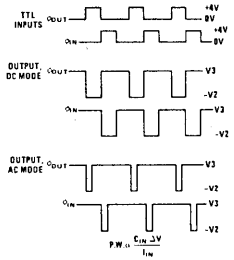


FIGURE 4. Waveforms, Each Half of Dual Driver

One point not covered in previous application notes is that capacitive coupling yields an additional fanout bonus by significantly reducing the power dissipation in the driver input (See MH0013 data sheet for more detailed calculations). Let's compare fanouts of half an MH0009 operating dc and half an MH0013 under the following typical conditions:

$f = 2$ MHz
$t_r = 50$ ns
P.W. = 200 ns
$V_{CC} = +5V$
$V_2 = -16V$
$V_3 = 0V$
$T_A = 70°C$

where t_r is the rise time and P.W. the pulse width of the input signal.

One factor limiting fanout is P_{max}, the package power dissipation. This is 500 mW for each half at 70°C, which covers both the internal dissipation P_{dc} and the transient dissipation P_{ac} involved in driving the load. That is,

$$P_{max} = P_{dc} + P_{ac}$$

The only significant P_{dc} in National's two-phase drivers occurs during the "1" output, so P_{dc} in half a direct-coupled MH0009 is

$$P_{"1"} = \left[(V_{CC}-V_2)I_{IN} + \frac{(V_3 - V_2)^2}{R_b}\right] \times \text{"1" duty cycle}$$

where I_{IN} from the TTL driver averages 20 mA and R_b is the output collector load resistor of 1.1 kΩ. Therefore,

$$P_{"1"} = (21 \times 20 + 16^2/1.1) \times 0.4 \times 10^{-3}$$
$$= 261 \text{ mW}$$

This allows P_{ac} to be 239 mW in the MH0009.

In the MH0013, the input voltage component is only the TTL "1" level of about 4.0V, so its $P_{"1"}$ is only 125 mW and P_{ac} can be 375 mW. In all drivers,

$$P_{ac} = C_L f \times (V_3 - V_2)^2$$

where C_L is the capacitive load presented by the MOS devices' clock inputs. Therefore, in this example each half of the directly coupled MH0009 would drive 467 pF worth of MOS devices, and the MH0013, 732 pF. The difference is more pronounced when the voltage swings are larger. In other words, each MH0013 could drive several more large MOS registers while dissipating the same power as the direct-coupled MH0009.

The two become equal when the absolute limit on fanout imposed by output current capability is reached. This is

$$C_{L(max)} = I \times t_r/V$$

where I is the output current limit and V the output voltage swing. These drivers will withstand transient currents of 600 mA, so $C_{L(max)}$ would be 1,875 pF at $V_2 = -16V$, $V_3 = 0V$ and $t_r = 50$ ns. Techniques such as lowering the duty cycle or making both V_3 and V_2 more positive can be used to work C_L up toward $C_{L(max)}$. But don't exceed it (a precaution that has sometimes been overlooked on the data sheets of rival devices).

Feedforward Compensation Speeds Op Amp

National Semiconductor
Linear Brief 2
Robert C. Dobkin

A feedforward compensation method increases the slew rate of the LM101A from 0.5/μs to 10V/μs as an inverting amplifier. This extends the usefulness of the device to frequencies an order of magnitude higher than the standard compensation network. With this speed improvement, IC op amps may be used in applications that previously required discretes. The compensation is relatively simple and does not change the offset voltage or current of the amplifier.

In order to achieve unconditional closed loop stability for all feedback connections, the gain of an operational amplifier is rolled off at 6 dB per octave, with the accompanying 90 degrees of phase shift, until a gain of unity is reached. The frequency compensation networks shape the open loop response to cross unity gain before the amplifier phase shift exceeds 180 degrees. Unity gain for the LM101A is designed to occur at 1 MHz. The reason for this is the lateral PNP transistors used for level shifting have poor high frequency response and exhibit excess phase shift about 1 MHz. Therefore, the stable closed loop bandwidth is limited to approximately 1 MHz.

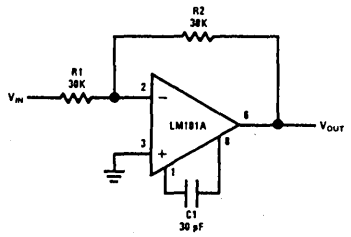


FIGURE 1. Standard Frequency Compensation

Usually, the LM101A is frequency compensated by a single 30 pF capacitor between Pins 1 and 8, as shown in Figure 1. This gives a slew rate of 0.5V/μs. The feedforward is achieved by connecting a 150 pF capacitor between the inverting input, Pin 2, and one of the compensation terminals, Pin 1, as shown in Figure 2. This eliminates the lateral PNP's from the signal path at high frequencies. Unity gain bandwidth is 10 MHz and the slew rate is 10V/μs. The diode can be added to improve slew with high speed input pulses.

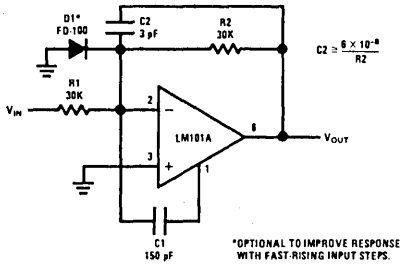


FIGURE 2. Feedforward Frequency Compensation

Figure 3 shows the open loop response in the high and low speed configuration. Higher open loop gain is realized with the fast compensation, as the gain rolls off at about 6 dB per octave until a gain of unity is reached at about 10 MHz. Figures 4 and 5 show the small signal and large signal transient response. There is a small amount of ringing; however, the amplifier is stable over a −55°C to +125°C temperature range. For comparison, large signal transient response with 30 pF frequency compensation is shown in Figure 6.

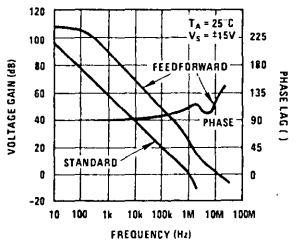


FIGURE 3. Open Loop Response for Both Frequency Compensation Networks

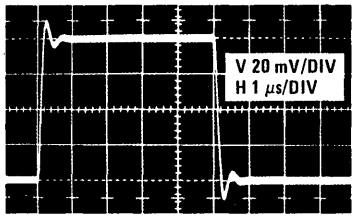


FIGURE 4. Small Signal Transient Response with Feedforward Compensation

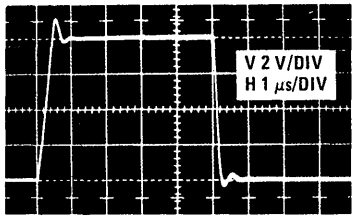


FIGURE 5. Large Signal Transient Response with Feedforward Compensation

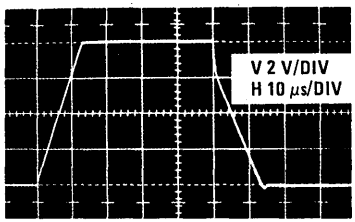


FIGURE 6. Large Signal Transient Response with Standard Compensation

As with all high frequency, high-gain amplifiers, certain precautions should be taken to insure stable operation. The power supplies should be bypassed near the amplifier with .01 μF disc capacitors. Stray capacitance, such as large lands on printed circuit boards, should be avoided at Pins 1, 2, 5, and 8. Load capacitance in excess of 75 pF should be decoupled, as shown in Figure 7; however, 500 pF of load capacitance can be tolerated without decoupling at the expense of bandwidth by the addition of 3 pF between Pins 1 and 8. A small capacitor C_2 is needed as a lead across the feedback resistor to insure that the rolloff is less than 12 dB per octave at unity gain. The capacitive reactance of C_2 should equal the feedback resistance between 2 and 3 MHz. For integrator applications, the lead capacitor is isolated from the feedback capacitor by a resistor, as shown in Figure 8.

Feedforward compensation offers a marked improvement over standard compensation. In addition to having higher bandwidth and slew, there is vanishingly small gain error from DC to 3 kHz, and less than 1% gain error up to 100 kHz as a unity gain inverter. The power bandwidth is also extended from 6 kHz to 250 kHz. Some applications for this type of amplifier are: fast summing amplifier, pulse amplifier, D/A and A/D systems, and fast integrator.

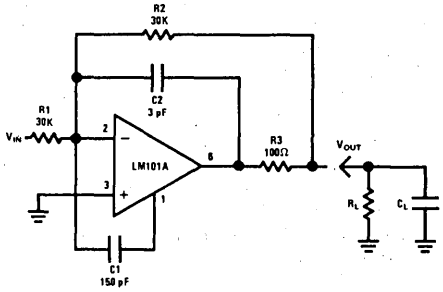


FIGURE 7. Capacitive Load Isolation

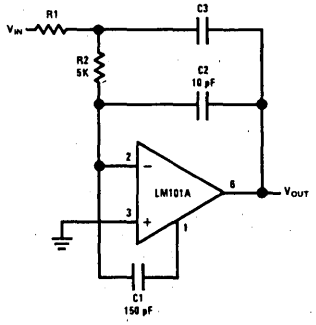


FIGURE 8. Fast Integrator

Speed Up the LM108 Feedforward Compensation

National Semiconductor
Linear Brief 14
Robert C. Dobkin

Feedforward frequency compensation of operational amplifiers can provide a significant increase in slew rate and bandwidth over standard lag compensation. When feedforward compensation is applied to the LM101A operational amplifier,[1] an order of magnitude increase in bandwidth results. A simple feedforward network has also been developed for use with the LM108 micropower amplifier to give a factor of five improvement in speed. It uses no active components and does not degrade the excellent dc characteristics of the LM108.

Figure 1 shows a schematic of an LM108 using the new compensation. The signal from the inverting input is fed forward around the input stage by a 500 pF capacitor, C_1. At high frequencies it provides a phase lead. With this lead, overall phase

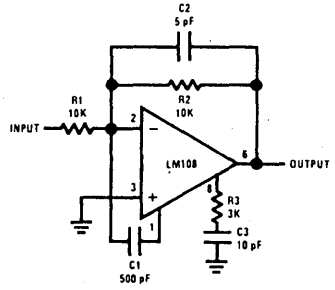


FIGURE 1. LM108 with Feedforward Compensation

shift is reduced and less compensation is needed to keep the amplifier stable. The $C_2 - R_1$ network provides lag compensation, insuring that the open loop gain is below unity before 180° phase shift occurs. The open loop gain and phase as a function of frequency is compared with standard compensation in Figure 2.

The slew rate is increased from 0.3V/μs to about 1.3V/μs and the 1 kHz gain is increased from 500 to 10,000. Small signal bandwidth is extended to 3 MHz. The bandwidth must be limited to 3 MHz because the phase shift through the lateral PNP transistors used in the second stage becomes excessive at higher frequencies. With the LM101A, 10 MHz bandwidth was possible since the signal was bypassed around the low frequency lateral PNP's. Nonetheless, 3 MHz is very respectable for a micropower amplifier drawing only 300 μA quiescent current.

When the LM108 is used with feedforward compensation, it is less tolerant of capacitive loading and stray capacitance. Precautions must be taken

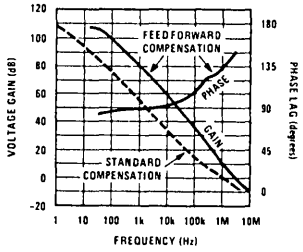


FIGURE 2. Open Loop Voltage Gain

to insure stability. If load capacitance is greater than about 75 to 100 pF, it must be isolated as shown in Figure 3. A small capacitor is always needed to provide a lead across the feedback resistor to compensate for strays at the input. About 3 to 5 pF is the minimum value capacitor. Care must be taken to minimize stray capacitance at Pins 1, 2 and 8 when feedforward compensation is used. Additionally, when the source resistance on the noninverting input is greater than 10k, it should be bypassed with a .01 μF capacitor.

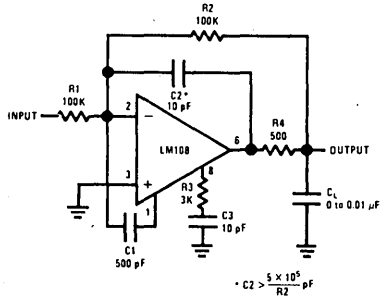


FIGURE 3. Decoupling Load Capacitance

As with any externally compensated amplifier, increasing the compensation of the LM108 increases the stability at the expense of slew and bandwidth. The circuit shown is for the fastest response. Increasing the size of C_2 to 20 or 30 pF

will provide 2 or 3 times greater stability and capacitive load tolerance. Therefore, the size of the compensation capacitor should be optimized for the bandwidth of the particular application.

The stability of the LM108 with feedforward compensation is indicated by the small signal transient responses shown in Figure 4. It is quite stable since there is little overshoot and ringing even though the amplifier is loaded with a 50 pF capacitor. Large signal transient response for a 20V square wave is shown in Figure 5. The small positive overshoot is not severe and usually causes no problems.

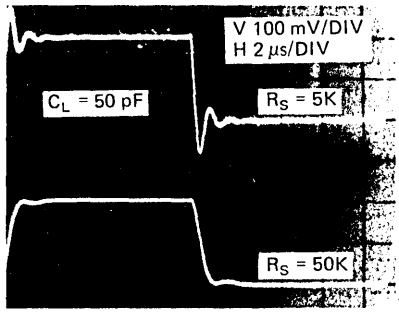


FIGURE 4. Small Signal Transient Response of LM108 with Feedforward Compensation

The LM108 is unusually insensitive to power supply bypassing with the new compensation. Even with several feet of wire between the device and power supply, it does not become unstable. However, it is still wise to bypass the supplies for drill since noise on the V^+ line can be injected to the summing junction by the 500 pF feedforward capacitor.

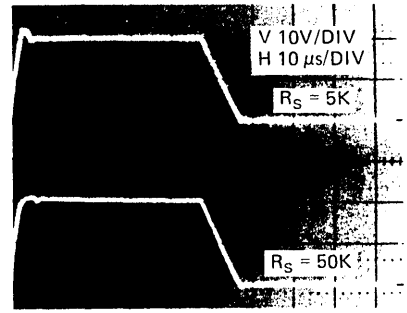


FIGURE 5. Large Signal Transient Response of LM108 with Feedforward Compensation

The new feedforward compensation is easy to use and offers a factor of five improvement over standard compensation. Slew rate is increased to 1.3V/μs and power bandwidth extended to 20 kHz. Also, gain error at high frequencies is reduced. This makes the LM108 more useful in precision applications where low dc error as well as low ac error is desired.

REFERENCE:

1. Robert C. Dobkin, "Feedforward Compensation Speeds Op Amp," *National Semiconductor LB-2,* March, 1969.

LM118 Op Amp Slews 70V/μsec

National Semiconductor
Linear Brief 17
Robert C. Dobkin

One of the greatest limitations of today's monolithic op amps is speed. With unity gain frequency compensation, general purpose op amps have 1 MHz bandwidth and 0.3 V/μs slew rate. Optimized compensation as well as feedforward compensation can improve op amp speed for some applications. Specialized devices such as fast, unity-gain buffers are available which provide partial solutions. This paper will describe a new high speed monolithic amplifier that offers an order of magnitude increase in speed with no loss in flexibility over general purpose devices.

The LM118 is constructed by the standard six mask monolithic process and features 15 MHz bandwidth and 70 V/μs slew rate. It operates over a ±5 to ±18V supply range with little change in speed. Additionally, the device has internal unity-gain frequency compensation and needs no external components for operation. However, unlike other internally compensated amplifiers, external feedforward compensation may be added to approximately double the bandwidth and slew rate.

DESIGN CONCEPTS

In general purpose amplifiers the unity-gain bandwidth is limited by the lateral PNP transistors used for level shifting. The response above 2 MHz is so poor that they cannot be used in a feedback amplifier. If the PNP transistors are used for level shifting only at DC or low frequencies and the signal is fed forward around the PNP transistors at high frequencies, wide bandwidth can be obtained without the excessive phase shift of the PNP transistors.

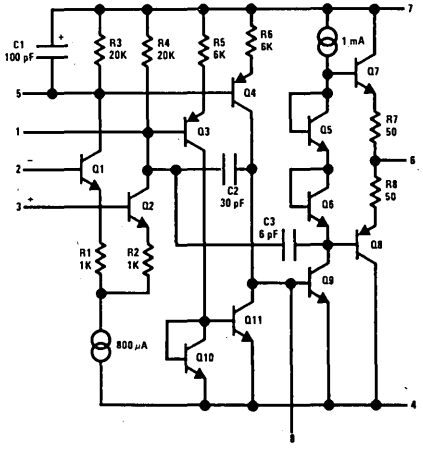


FIGURE 1. Simplified Circuit of the LM118

Figure 1 shows a simplified schematic of the LM118. Transistors Q_1 and Q_2 are a conventional differential input stage with emitter degeneration and resistive collector loads. Q_3 and Q_4 form the second stage which further amplify the signal and level shift the signal towards V^-. The collectors of Q_3 and Q_4 drive a current inverter, Q_{10} and Q_{11} to convert from differential to single ended. Q_9, which has a current source load for high gain, drives a class B output. The collectors of the input stage and the base of Q_9 are available for offset balancing and external compensation.

Frequency compensation is accomplished with three internal capacitors. C_1 rolls off on half the differential input stage so that the high frequency signal path is single-ended. Also, at high frequencies, the signal is fed forward around the lateral PNP transistors by a 30 pF capacitor, C_2. This eliminates the excessive phase shift. Overall frequency response is then set by capacitor, C_3, which rolls off the amplifier at 6 dB/octive. As previously mentioned feedforward compensation for inverting applications can be applied to the base of Q_9. Figure 2 shows the open loop frequency response of an LM118. Table 1 gives typical specifications for the new amplifier.

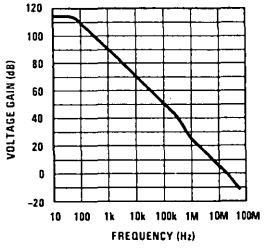


FIGURE 2. Open Loop Voltage Gain as a Function of Frequency for LM118.

TABLE 1. Typical Specifications for the LM118

Input Offset Voltage	2 mV
Input Bias Current	200 nA
Offset Current	20 nA
Voltage Gain	200K
Common Mode Range	±11.5V
Output Voltage Swing	±13V
Small Signal Bandwidth	15 MHz
Slew Rate	70 V/μs

OPERATING CONFIGURATION

Although considerable effort was taken to make the LM118 trouble free, high frequency amplifiers are more prone to oscillations than low frequency devices such as the LM101A. Care must be taken to minimize the stray capacitance at the inverting input and at the output; however the LM118 will drive a 100 pF load. Good power supply bypassing is also in order—0.1 μF disc ceramic capacitors should be used within a few inches of the amplifier. Additionally, a small capacitor is usually necessary across the feedback resistor to compensate for unavoidable stray capacitance.

Figure 3 shows feedforward compensation of the LM118 for fast inverting applications. The signal is fed from the summing junction to the output stage driver by C_1 and R_4. Resistors R_5, R_6 and R_7 have two purposes: they increase the internal operating current of the output stage to increase slew rate and they provide offset balancing. The current boost is necessary to drive internal stray capacitance at the higher slew rate. Mismatch of the external resistors can cause large voltage offsets so offset balancing is necessary. For supply voltages other than ±15V, R_5 and R_6 should be selected to draw about 500 μA from Pins 1 and 5.

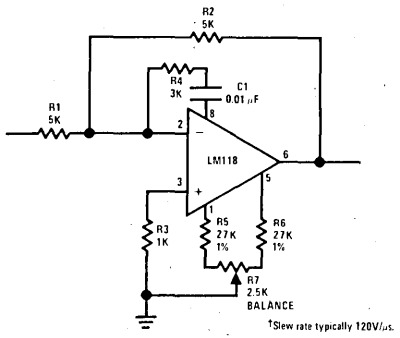


FIGURE 3. Feedforward Compensation for Greater Inverting Slew Rate†

When using feedforward, resistor R_4 should be optimized for the application. It is necessary to have about 8 kΩ in the path from the output of the amplifier through the feedback resistor and through feedforward network to Pin 8 of the device. The series resistance is needed to limit the bandwidth and prevent minor loop oscillation.

At high gains, or with high value feedback resistors R_4 can be quite low—but not less than 100Ω. When the LM118 is used a fast integrator, with a large feedback capacitor or with low values of feedback resistance, R_4 must be increased to 8 kΩ to insure stability over a full −55°C to 125°C temperature range.

One of the more important considerations for a high speed amplifier is settling time. Poor settling time can cancel the advantages of having high slew rate and bandwidth. For example—an amplifier can have severe ringing after a step input. A relatively long time is then needed before the output voltage can be read accurately. Settling time is the time necessary for the output to slew through a defined voltage change and settle to within a defined error of its final output voltage. Figure 4 shows optimized compensation for settling to

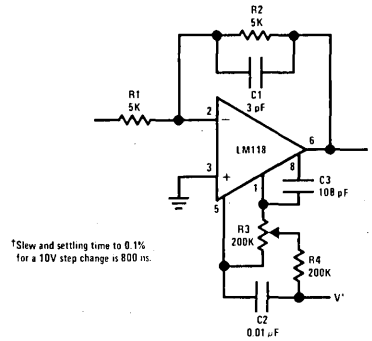


FIGURE 4. Compensation for Minimum Settling† Time

within 0.1% error. Typically the settling time is 800 ns for a simple inverter circuit as shown. Settling time is, of course, subject to operating conditions external to the IC such as closed loop gain, circuit layout, stray capacitance and source resistance. An optional offset balancing circuit, R_3 and R_4 is included.

The LM118 opens up new fields for IC operational amplifiers. It is more than an order of magnitude faster than general purpose amplifiers while retaining the ease of use features. It is ideally suited for analog to digital converters, active filters, sample and hold circuits and wide band amplification. Further, the LM118 has the same pin configuration as the LM101A or LM741 and is interchangeable with these devices when speed is of prime concern.

Reducing DC Errors in Op Amps

National Semiconductor
Technical Paper 15

Robert J. Widlar
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Abstract. *An IC op amp design that reduces bias currents below 100 pA over a −55°C to 125°C temperature range is discussed. Super-gain bipolar transistors with on-wafer trimming are used, providing low offset voltage and drift. The key to low bias current is the control of high temperature leakage currents along with the development of reasonably accurate nanoampere current sources with low parasitic capacitance.*

Introduction

A bipolar replacement for the LM108 [1] drastically reduces offset voltage, bias current and temperature drift. This design, the LM11, does not depend on new technology. Instead, the improvements result from a better understanding of transistor behavior, new circuit techniques and the application of proven offset trimming methods. Table I summarizes the results obtained. The combination of low offset voltage and low bias current is unique to IC op amps, while the performance at elevated temperatures represents an advance in the state of the art.

Table I. Input error terms of the LM11 show an improvement over FET op amps even at room temperature. There is little degradation in performance from −55°C to 125°C. Other important specifications are somewhat better than the LM108A.

parameter	$T_j = 25°C$		$-55°C \leq T_j \leq 125°C$	units
	typ	max	max	
input offset voltage	0.1	0.3	0.6	mV
input offset current	0.5	10	30	pA
input bias current	25	50	150	pA
offset voltage drift	1		3	μV/°C
offset current drift	20			fA/°C
bias current drift	0.5		0.5	pA/°C

Junction FETs

At first glance, field effect transistors seem to be the ideal input stage for an op amp, mainly because they have a low gate current, independent of their operating current. Practically, they do provide an attractive combination of performance characteristics in a relatively simple design. But there are serious shortcomings.

For one, FETs do not match as well as bipolar devices: the offset voltage is at least an order of magnitude worse. Laser trimming can compensate for this to some extent. But with FETs, low offset voltage does not guarantee low drift, as it does with bipolars. FETs are also sensitive to mechanical strains and subject to offset shifts during assembly or with temperature cycling. Typically, long term stability is about 100 μV/year, although this can go to 1 mV/year with no prior warning in early life. This contrasts to a 10 μV/year long term stability for bipolar pairs.

Lastly, although the input current of FETs is low at room temperature, it doubles for every 10°C increase. This, coupled with high offset voltage drift, makes FETs much less attractive as operating temperature is increased.

MOS FETs

Field effect transistors, with a metal gate and oxide insulation, give the ultimate in low input current. Practically, this advantage disappears when diodes are included to protect the gate from static charges encountered in normal handling. Further, the offset voltage problems of JFETs go double for MOS FETs. They are also subject to offset shifts due to contamination.

Interesting designs are on the horizon for various chopper-stabilized complementary MOS ICs. These solve most offset voltage problems, but not that of input leakage current. Even at moderate temperatures, this input current will seriously degrade the low offset voltage and drift even with relatively low source resistances. Chopper-stabilized amplifiers have added problems with overload recovery and noise, especially with high source impedances. These problems have limited solutions, but chopper stabilization is not usually suitable for general purpose applications.

bipolar op amps

Offset voltage, its drift or long term stability has not been a serious problem with bipolar-input op amps. Such techniques as cross-coupling or zener-zap trimming have reduced offset voltage to 25 μV in production. The real problem has been bias current. The LM108, introduced in 1968, has represented the state of the art in low bias currents for standard bipolar devices. At 3 nA, maximum over temperature, the bias current is lower than FETs above 85°C.

A Darlington version of the LM108, the LM216, provided bias currents in the 50 pA range; but this design was seriously marred by high offset voltage, drift, excessive low frequency noise and anomalous leakage currents at higher temperatures.

Improvements in this design were thwarted by the inability to provide nanoampere bleed currents to stabilize the Darlington input and the erroneous belief that uncontrollable surface states created the anomalous leakage.

a new design

With bipolar transistors, there is a tradeoff between current gain and breakdown voltage. Super-gain transistors are devices that have been diffused for maximum current gain at the expense of breakdown voltage (which is typically a couple volts for a current gain of 5000). These low voltage transistors can be operated in a cascode connection with standard transistors to give a composite device with both high gain and breakdown voltage.

Figure 1 shows a modified Darlington input stage for a super-gain op amp. Common base standard transistors (Q5 and Q6, drawn with a wider base) are bootstrapped to the super-gain input transistors so that the latter are operated at near zero collector base voltage. In addition to permitting the use of super-gain inputs, this connection also isolates the input transistors from common-mode variations, increasing common-mode rejection.

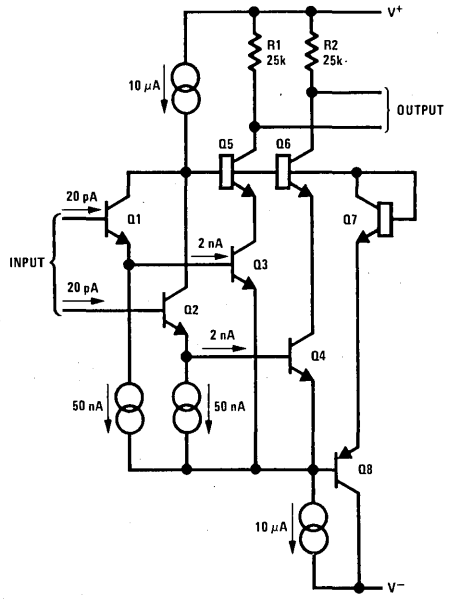
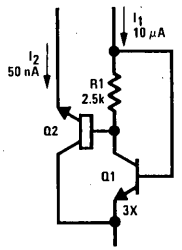


Figure 1. Bootstrapped input stage using super-gain transistors in modified-Darlington connection. The objectionable characteristics of the Darlington are virtually eliminated by operating the input transistors at a much larger current than the base current of the transistors they are driving.

The usual problems with the Darlington connection are avoided by providing a bleed current that operates the input transistors, Q1 and Q2, at a current much higher than the base current of the transistors they are driving, Q3 and Q4. This is necessary because the base currents are not that well matched, especially over temperature, and have excess low frequency noise.

a nanoampere current source

A circuit that generates the 50 nA bleed current is shown in figure 2. A super-gain transistor operated in the forward mode is used to bias a standard transistor in the reverse mode. The reverse connection is used because the capacitance of an ordinary collector tub would reduce the common-mode slew rate from 2 V/μs to 0.02 V/μs.



$$I_2 = \frac{h_{fe2}A_2 I_1}{h_{fe1}A_1} \exp.\frac{qI_1R_1}{kT}$$

Figure 2. Forming a nanoampere current source with low parasitic capacitance. Design takes advantage of predictable V_{BE} difference between standard and super-gain transistors and fact that V_{BE} of a transistor is the same when operated in forward or reverse mode.

At first look, this biasing scheme would seem to be subject to a number of process variations. This is not so. For one, the V_{BE} of a transistor depends on the base Gummel number ($Q_B/\bar{\mu}_B$), the number of majority carriers per unit area divided by their effective mobility. Since the Gummel number and the effective area are unchanged when the collector and emitter are interchanged, the V_{BE} will be the same in either connection, provided that base recombination is not excessive. In standard IC transistors, reverse h_{fe} is about 30, indicating that recombination is not a significant factor. Measured reverse h_{fe} is much lower, but this is the result of a parasitic PNP that does not affect V_{BE} or α_E, the common base current gain.

The bleed current depends also on the ratio of super-gain to standard transistor h_{fe}, as indicated by the equation in figure 2. Intuition suggests that super-gain h_{fe} will increase much faster than standard transistor h_{fe} with increasing emitter diffusion time, giving lower bleed current with higher super-gain h_{fe}. However, measurements with variances of standard LM108 processing indicate that the bleed current remains within 25% of design center.

As shown in figure 2, higher current ratios can be obtained by increasing the area of Q1 relative to Q2 or by including R1. The equation in figure 2 assumes that I_1 varies as absolute temperature. If the voltage drop across R1 is equal to kT/q, changes in the V_{BE} of Q1 with small changes in I_1 will be cancelled by changes in the voltage drop across R1. This makes input bias current essentially unaffected by variations in supply or common-mode voltage as long as I_1 is reasonably well controlled.

leakage currents

The input leakage currents of bipolar op amps can be kept under control because small geometry devices are satisfactory and because the collector-base junction can be operated at an arbitrarily low voltage if bootstrapping is used.

Simple theory predicts that bulk leakage saturates for reverse biases above 2kT/q. But generation in the depletion zone dominates below 125°C. Because the depletion width varies with reverse bias, so does leakage. The characteristics of a high quality junction plotted in figure 3 show that leakage current can be reduced with lower bias.

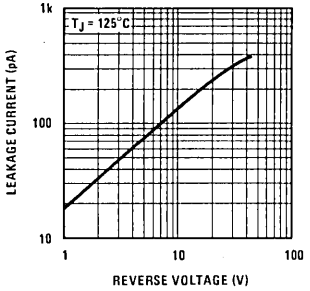


Figure 3. Voltage sensitivity of collector base leakage indicates that generation in the depletion zone dominates even at 125°C.

When more than one junction is involved, minimum leakage is not necessarily obtained for zero bias. This is illustrated in figure 4, a plot of I_{CBO} for a junction isolated NPN transistor. A parasitic PNP is formed between the base and the isolation as diagrammed in the inset. Zero leakage is obtained when V_{CB} is set so that the PNP diffusion current equals I_{CBO} of the NPN.

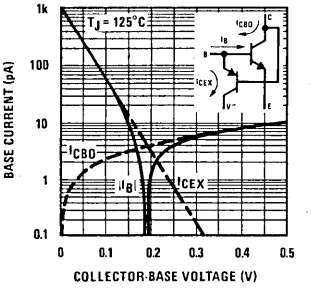


Figure 4. Plot above explains "anomalous" leakage of NPN transistors in ICs. As collector base bias is reduced, base current reverses then increases exponentially. This excess current is the forward diffusion current of parasitic PNP to substrate (see inset).

input protection

The input clamps perform a dual function. Most important, they protect the emitter base junction of the input transistors from damage by in-circuit overloads or static charges in handling. Secondly, they limit the voltage change across junction capacitances on low current nodes under transient conditions. This minimizes recovery delays.

The clamp circuitry is shown in figure 5. Emitters are added on the input transistors and cross-coupled to limit the differential input voltage. Another transistor, Q5, has been added to limit voltage on the input transistors if the inputs are driven below V^-.

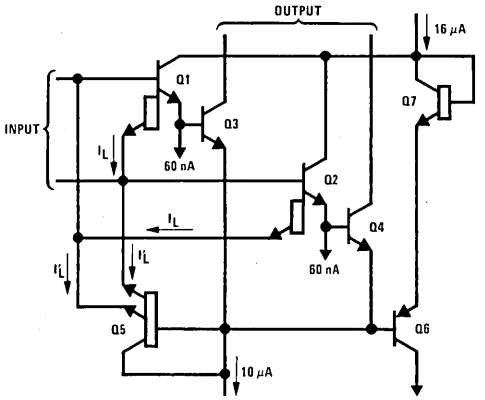


Figure 5. Separate clamps are used for differential and common-mode overloads. Leakage currents, I_{CES} of forward and reverse connected transistors, cancel.

The differential clamp transistors do contribute to input current because $V_{CR} > 0$, so collector current is not zero for $V_{BE} \cong 0$ ($I_{CES} \cong 100$ pA at 125°C). The common-mode input clamp, Q5, is also operated at $V_{BE} = 0$ and $V_{CB} > 0$, although in the inverted mode. The resulting error is diffusion current, dependent only on the characteristic V_{BE} of the transistors. Thus, the current contributed by the differential clamp transistors is cancelled, within a couple percent, by that from the common-mode clamp.

bias current

Figure 6 shows some results of the design approach described here. A room temperature bias current of 25 pA is obtained, and this is held to 60 pA over a −55°C to 125°C temperature range. The figure also shows the results of some improvements in development that have reduced bias current to 20 pA over the full operating temperature range.

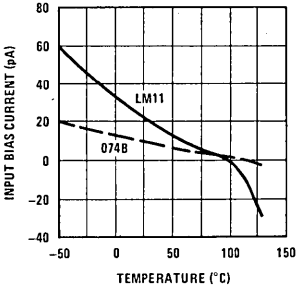


Figure 6. Input bias current of the LM11 remains low over military temperature range. Improvements in development give even better results (074B). Offset current is usually below 1 pA.

Figure 6 shows that bias current is very nearly a linear function of temperature, at least from −55°C to 100°C. This, coupled with the fact that bias current is virtually unaffected by changes in common-mode or supply voltage, suggests that bias current compensation can be provided for critical applications. An appropriate circuit is shown in figure 7. Details are given in reference [2], but properly set up it should be possible to hold bias currents to less than 20 pA over a −55°C to 100°C temperature range or 5 pA over a 15°C to 55°C range with a simple room temperature adjustment.

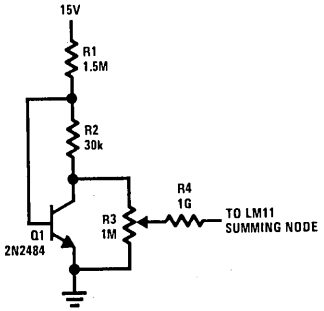


Figure 7. Bias current of LM11 varies linearly with temperature so it can be effectively compensated with this circuit. Bias currents less than 5 pA over 15°C to 55°C range or 20 pA over −55°C to 100°C are practical.

noise

The broadband noise of a bipolar transistor is given by

$$e_n = kT\sqrt{2\Delta f/qI_c} \quad (1)$$

Therefore, operating the input transistors at low collector current does increase noise. Because the noise of most op amps is greater than the theoretical noise voltage of the input transistors, the noise increase from low current input buffers is not as great as might be expected. In addition, when operating from higher source resistances, op amp noise is obscured by resistor noise, as shown in figure 8.

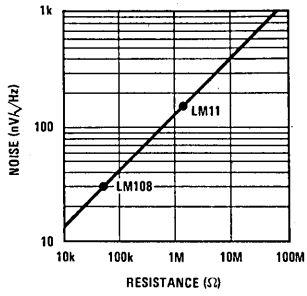


Figure 8. Increased noise of LM11 is consequence of low collector current in input transistors. But in high impedance applications, op amp noise is masked by the thermal noise of source resistance given above.

Low frequency noise is not as easily accounted for as broadband noise, but lower operating currents increase noise in much the same fashion. The low frequency noise of the LM11, shown in figure 9, is a bit less than FETs but greater than that of the LM108 when it is operated from source resistances less than 500 kΩ.

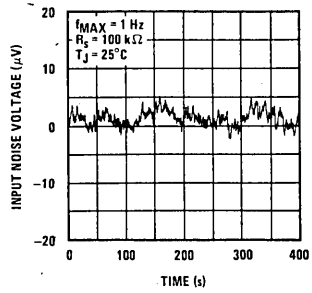


Figure 9. Low frequency noise of LM11 is high compared to other bipolar devices but somewhat less than FETs. It is equal to LM108 operating from 500 kΩ source resistance.

complete circuit

A schematic diagram of an IC op amp using the techniques described is shown in figure 10. Other than the input stage, the circuitry is much like the LM112, a compensated version of the LM108 that includes offset balancing.

One significant change has been the inclusion of wafer level trimming for offset voltage. This is done using zener-zap trimming across portions of the input stage collector load resistors, R4 and R5. This kind of zener is simply the emitter base junction of an NPN transistor. When pulsed with a large reverse current at wafer sort, the junction is destroyed by the formation of a low resistance filament between the emitter and base contact beneath the protective oxide. This shorts out a portion of the collector load resistor. The process is repeated on binary weighted segments until the offset voltage has been minimized.

Offset voltage of the LM11 is conservatively specified at 300 μV. Although low enough for most applications, offset voltage trimming is provided for fine adjustment. Balance range is determined by the resistance of the balance potentiometer, varying from ±5 mV at 100 kΩ to ±400 μV at 1 kΩ. Incidentally, when nulling offset voltages of 300 μV, the thermal matching of balance-pot resistance to the internal resistors is not a significant factor.

The actual balancing is done on the emitters of lateral PNP transistors, Q9 and Q10, that imbalance the collector loads of the input stage, This particular arrangement was used so that no damage would result from accidental connection of the balance pins to voltages outside either supply. Not obvious is that a balance pin voltage 15V more negative than V+ can effectively short these PNP transistors with a parallel P-channel MOS transistor, forcing the output to one limit or another.

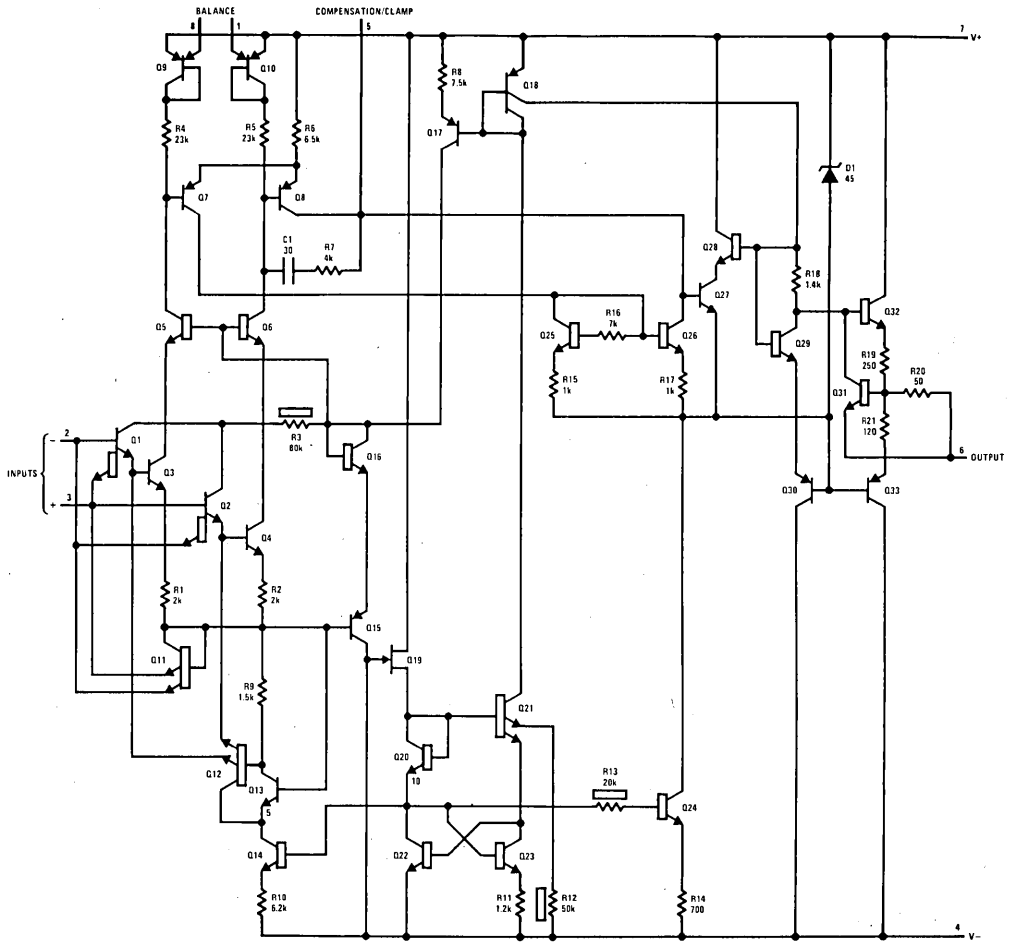


Figure 10. Complete schematic of the LM11. Except for the input stage, circuit is much like the LM112, a compensated version of the LM108 that includes offset balancing.

Although the LM11 is specified to a lower voltage than the LM108, the minimum common-mode voltage is a diode drop further from V^- because the bleed current generator, Q12 and Q13, has been added.

Proceeding from the input stage, the second stage amplifier is a differential pair of lateral PNPs, Q7 and Q8. These feed a current mirror, Q25 and Q26, which drive a super-gain follower, Q27. The collector base voltage of Q26 is kept near zero by including Q28. The current mirror is bootstrapped to the output so that second stage gain error depends only on how well Q7 and Q8 match with changes in output voltage. This gives a gain of 120 dB in a two stage amplifier. Frequency compensation is provided by MOS capacitor C1.

The output stage is a complementary class-B design with current limiting. Biasing has been altered so that the guaranteed output current is twice the LM108. A zener diode, D1, limits output voltage swing to prevent stressing the MOS capacitor to the point of catastrophic failure in the event of gross supply transients.

The main bias current generator design (Q20-Q23) is due to Dobkin [3]. It is powered by Q19, a collector FET. The circuit is auto-compensated so that output current of Q14 and Q21 varies as absolute temperature and changes by less than 1% for a 100:1 shift in Q19 current.

speed

With a unity gain bandwidth of 500 kHz and a 0.3 V/μs slew rate the LM11 is not fast. But it is no slower than might be expected for a supply current of only 300 μA.

If the precision of the LM11 is required along with greater speed, the circuit in figure 11 might be used. Here, the LM11 senses input voltage and makes appropriate adjustments to the balance terminals of a fast FET amplifier. The main signal path is through the fast amplifier.

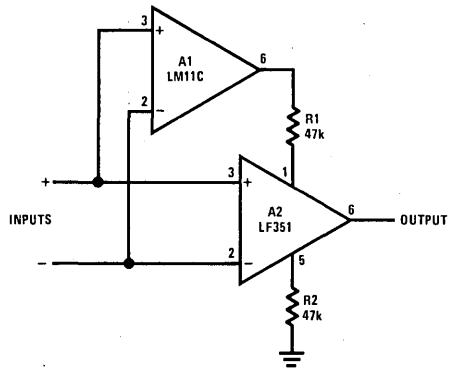


Figure 11. The LM11 can zero offset of fast FET op amp in either inverting or non-inverting configurations. Speed is that of fast amplifier. FET amplifier can be capacitively coupled to critical input to eliminate its leakage current.

Surprisingly, this connection will work even as a voltage follower. The common-mode slew recovery of the LM11 is about 10 μs to 1 mV, even for 30V excursions. This was accomplished by minimizing or bootstrapping stray capacitances and providing clamping to limit the voltage excursion across the strays.

When bias current is an important consideration, it will be advisable to ac couple the FET op amp to the critical input. Reference [2] discusses this and other practical aspects of fast operation with the LM11.

conclusions

A new IC op amp has been described that can not only increase the performance of existing equipment but also creates new design possibilities. Op amp error has been reduced to the point where other problems can dominate. Many of the practical difficulties encountered in high impedance circuitry are discussed in reference [4] along with solutions. A number of tested designs using these techniques are given in reference [2].

The LM11 is not the result of any breakthrough in processing technology. It is simply a modification of ICs that have been in volume production for over 10 years. The improvements have resulted primarily from an understanding of strange behavior observed on the earlier ICs and taking advantage of certain inherent characteristics of bipolar transistors that were not fully appreciated.

As users of the LM11 may have discovered, the offset voltage and bias current specifications are quite conservative. It seems possible to offer 50 μV offset voltage and perhaps 1 μV/°C drift even on low cost parts. Taking full advantage of 5 pA bias current would require guarded 10-pin TO-5 packages or 14-pin DIP packages. Further, the feasibility of reducing low frequency noise to 2 μV and 0.1 pA, peak to peak, has been demonstrated on prototype parts.

acknowledgement

The author would like to acknowledge the contributions of Dennis Foltz for solving the rather formidable production test problems of the LM11.

references

[1] R.J. Widlar, "IC op amp beats FETs on input current", National Semiconductor AN-29, December 1969.
[2] R.J. Widlar, R. Pease and M. Yamatake, "Applying a new precision op amp", National Semiconductor AN-242, April 1980.
[3] R. Dobkin, U.S. patent no. 3930172.
[4] R.J. Widlar, "Working with high impedance op amps", National Semiconductor AN-241, February 1980.

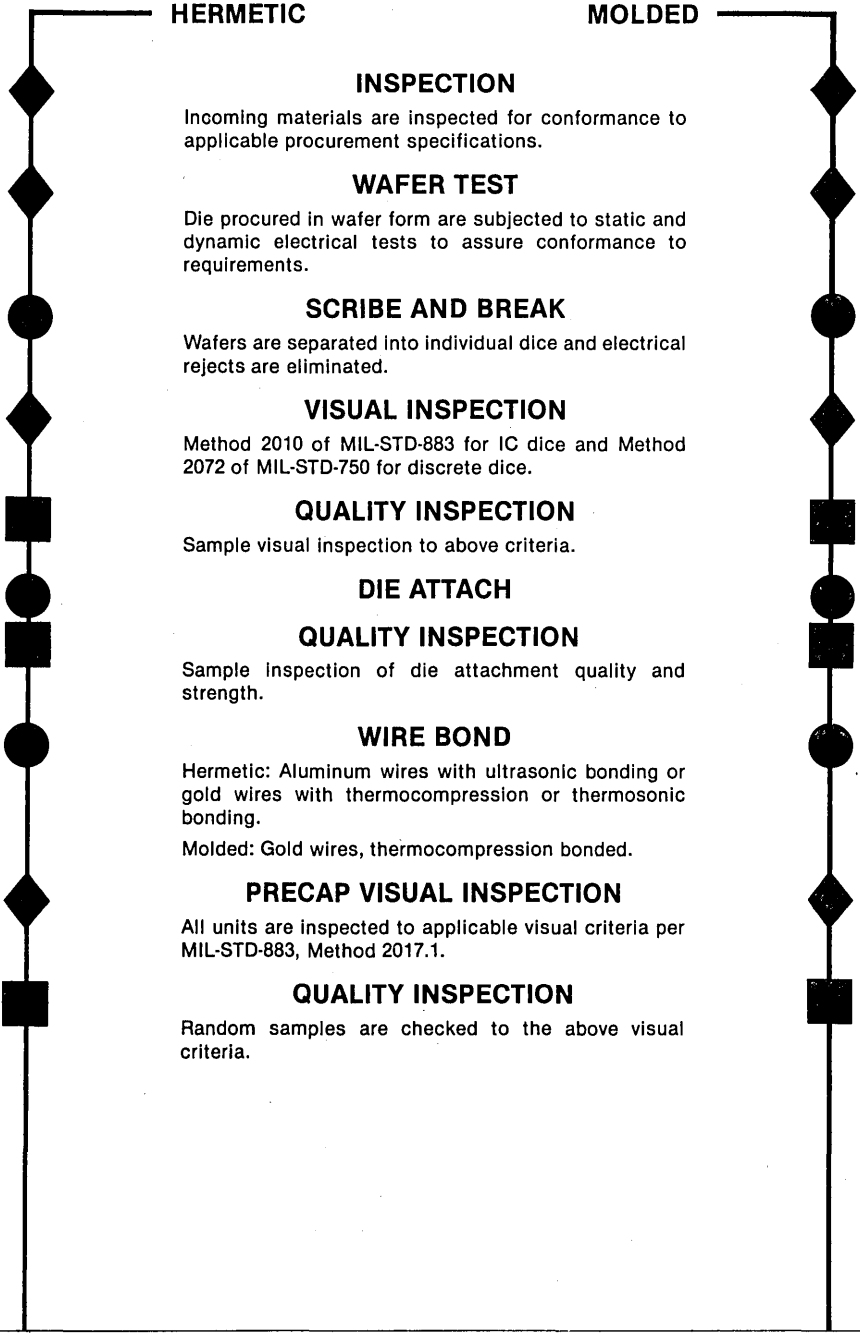
Section 18

Appendices/ Physical Dimensions

18

Appendix I.
Standard Production Flow for Hermetic and Molded Packages

See 883/RETS Program Section 16 for reliability process flow and group details.



FINAL SEAL ENCAPSULATION

STABILIZATION BAKE

MIL-STD-883, Method 1008, Cond. C, 150 °C, 24 hours.

TEMPERATURE CYCLE

MIL-STD-883, Method 1010, Cond. C.

Hermetic: −65 °C, +150 °C, 10 cycles.

CENTRIFUGE

MIL-STD-883, Method 2001, Cond. D, 20,000 G, Y1 direction only.

HERMETICITY

MIL-STD-883, Method 1014, Cond. B: Fine Leak.

MIL-STD-883, Method 1014, Cond. C2: Gross Leak.

ELECTRICAL TEST

MIL-STD-883, Method 5008, Para. 3.2.3.10: Static, dynamic, functional tests per specification.

QUALITY GROUP A ELECTRICAL TEST (TABLE I)

Sample size and quality levels per MIL-STD-883, Method 5008.

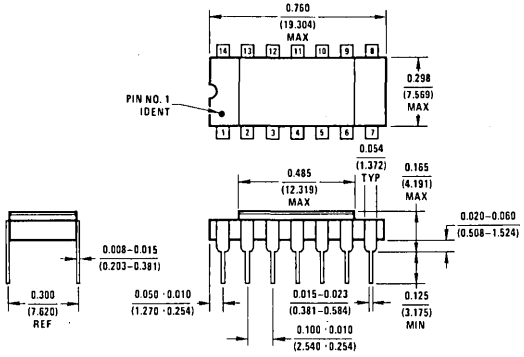
MARK, INSPECT, PACK

MIL-STD-883, Method 2009.1.

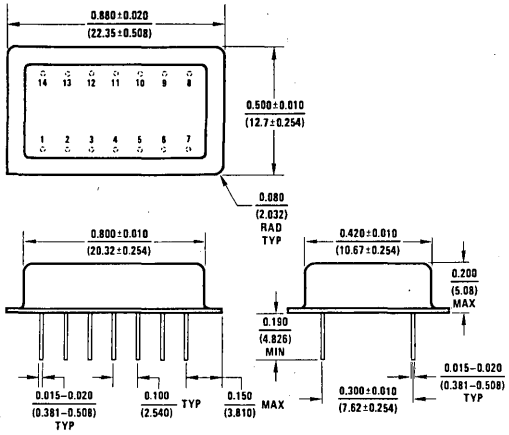
QUALITY INSPECTION

Marking, physical and electrical sample test to applicable specifications.

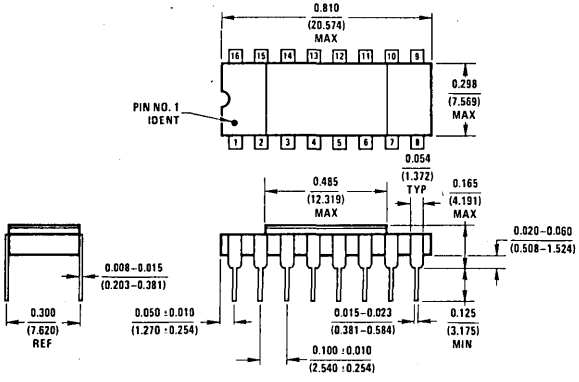
SHIP



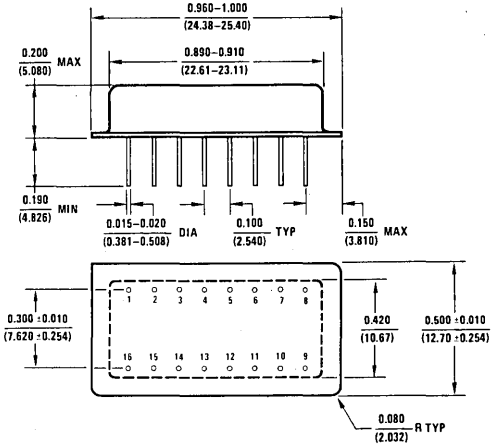
NS Package D14E
14-Lead Cavity DIP (D)
(Side Brazed)



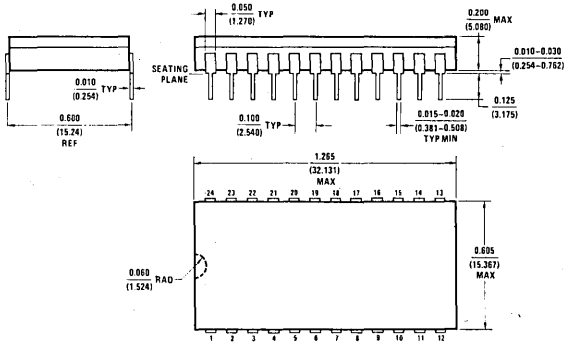
NS Package D14F
14-Lead Metal DIP



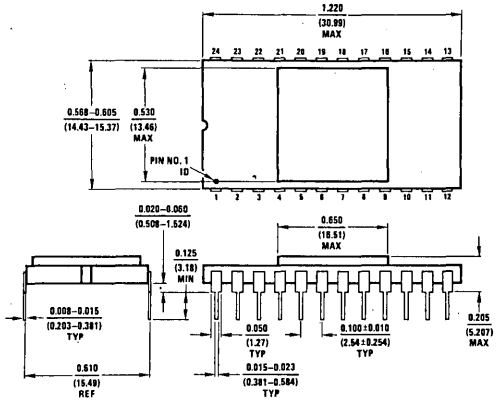
NS Package D16C
16-Lead Cavity DIP (D)
(Side Brazed)



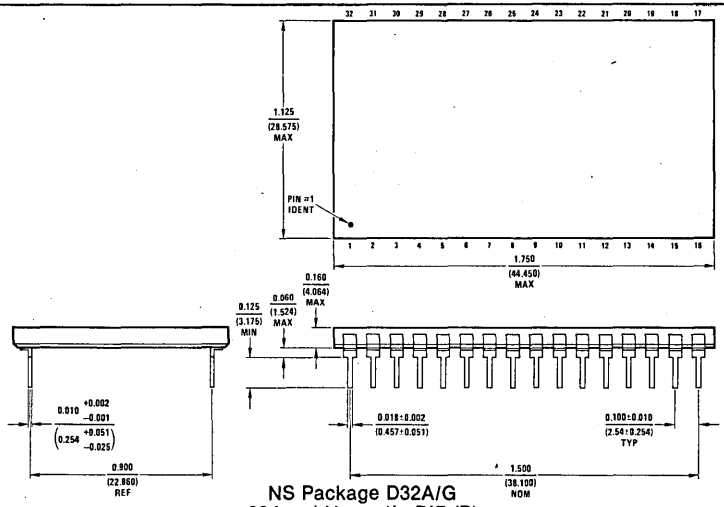
NS Package D16D
16-Lead Metal DIP24-lead DIP (D)



NS Package D24D
2-Lead TO-46 Metal Can Package

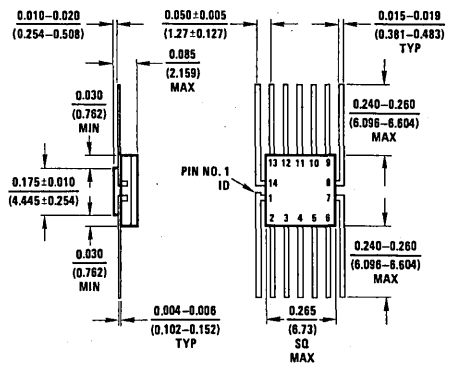


NS Package D24G
24-Lead Hermetic Dip (D)
(Hybrid)

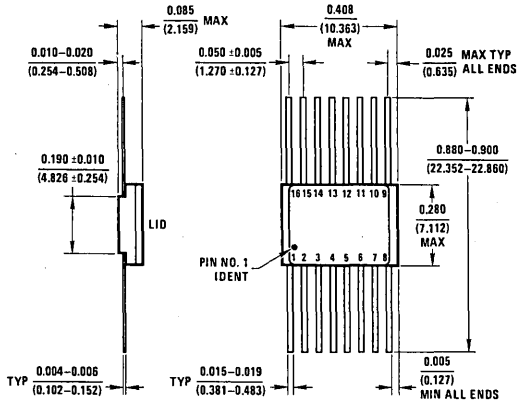


NS Package D32A/G
32-Lead Hermetic DIP (D)
(Hybrid Bottom Braze)

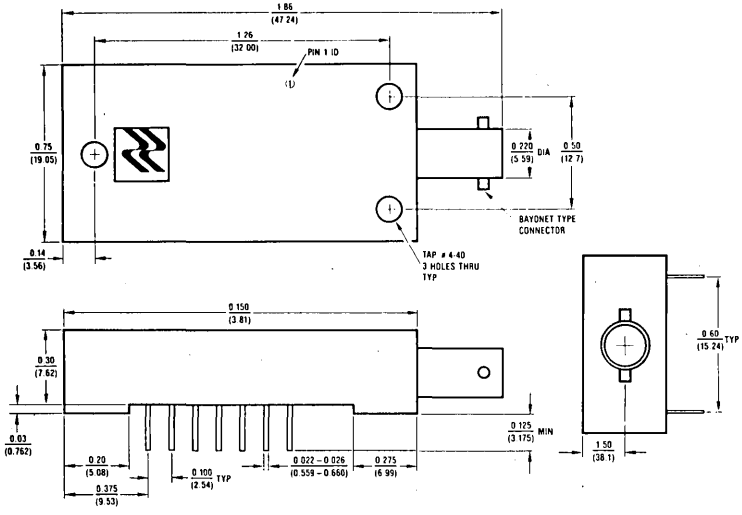
NS Package D32B
Contact National
Semiconductor Corp.,
Product Marketing
Group for Package
Information



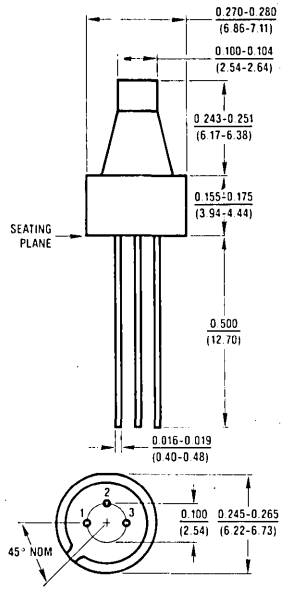
NS Package F14D
14-Lead Ceramic Flat Package (F)
(Hybrid)



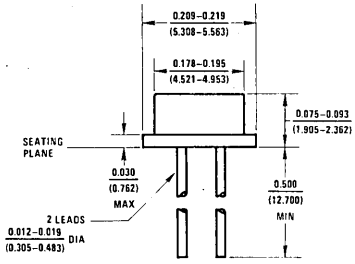
NS Package F16B
16-Lead Ceramic Flat Package (F)

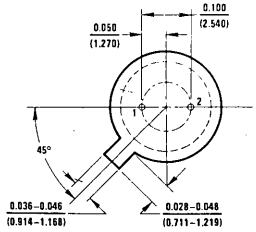


NS Package FO-03A
Short Ferrule Package (P)

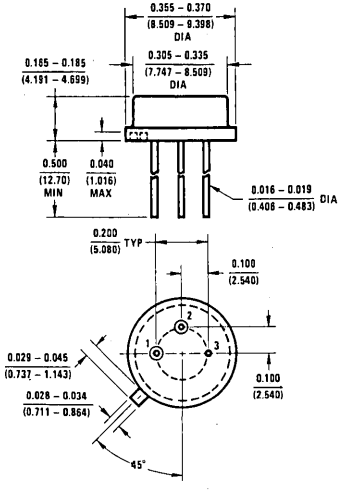


NS Package FO14A
14-Lead Fiber-Optic Cast DIP Package





NS Package H02A
2-Lead TO-46 Metal Can Package (H)



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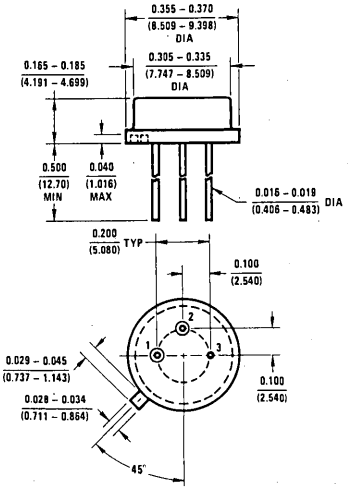
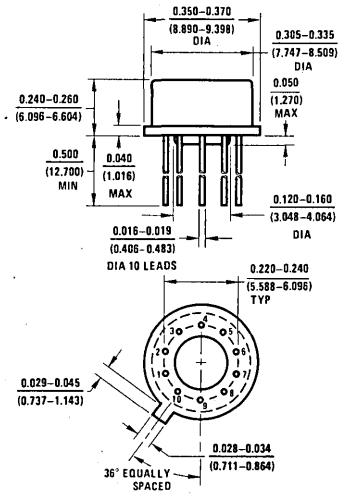
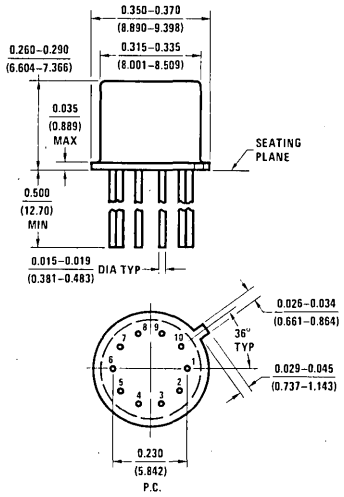
3-Lead TO-39 Metal Can Package (H)



NS Package H03B
3-Lead TO-5 Metal Can Package (H)



NS Package H10A
10-Lead TO-5 Metal Can Package (H)
(High Profile)



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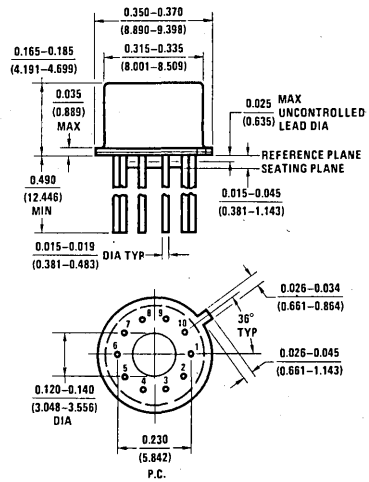
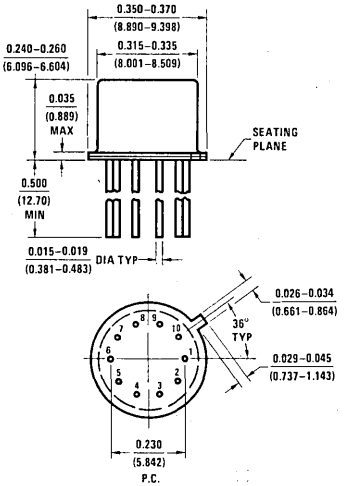
10-Lead TO-5 Metal Can Package (H)



NS Package H10C
10Lead TO-5 Metal Can Package (H)
(Low Profile)



NS Package H10D
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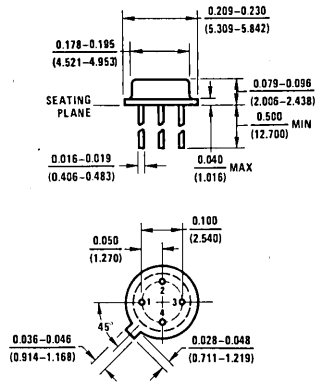
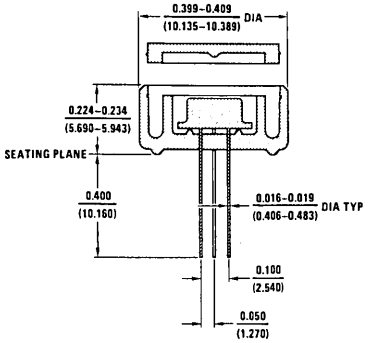


NS Package H04A
4-Lead TO-46 Metal Can Package (H)



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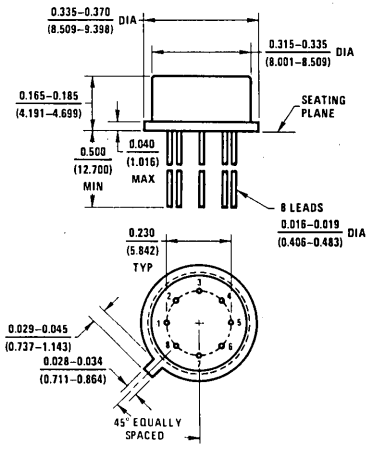
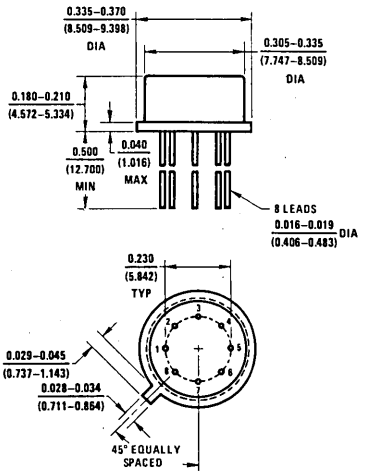
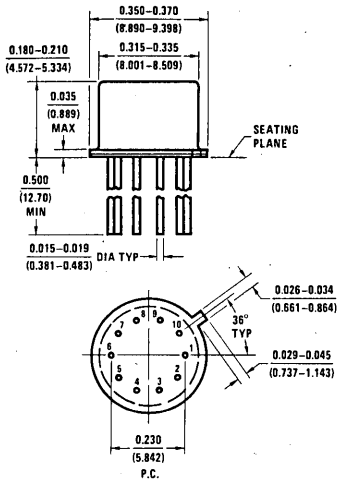
Thermal Shield for H04A



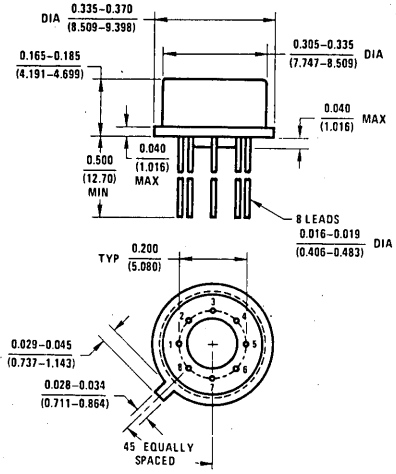
NS Package H08A
8-Lead TO-5 Metal Can Package (H)



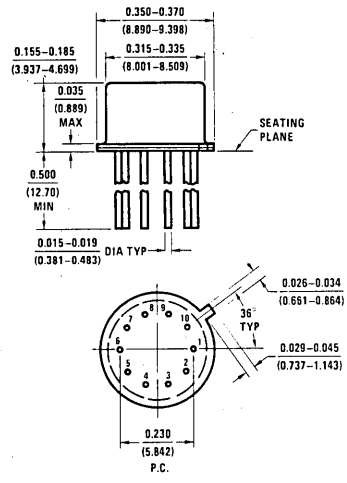
NS Package H08B
8-Lead TO-5 Metal Can Package (H)



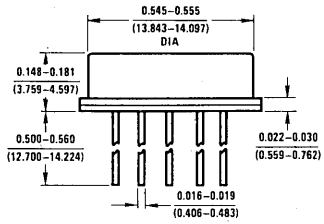
NS Package H10E
10-Lead TO-Metal Can Package (H)

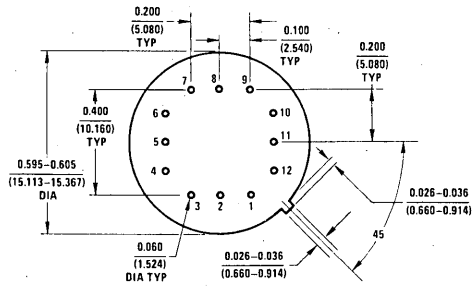


NS Package H08C
8-Lead Metal Can Package (H)

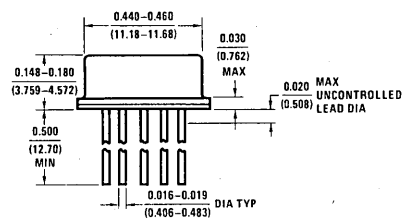


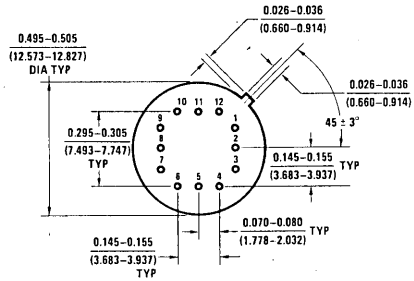
NS Package H10F
10-Lead TO-5 Metal Can Package (H)



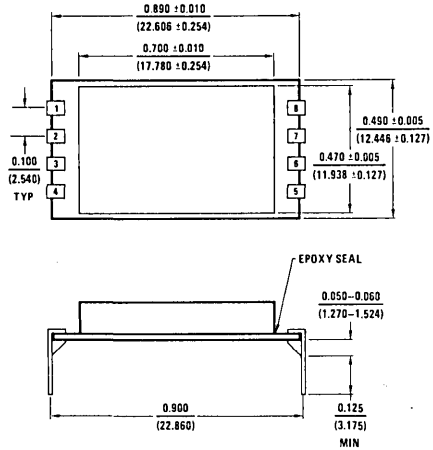


NS Package H12B
12-Lead TO-8 Metal Can Package (G)

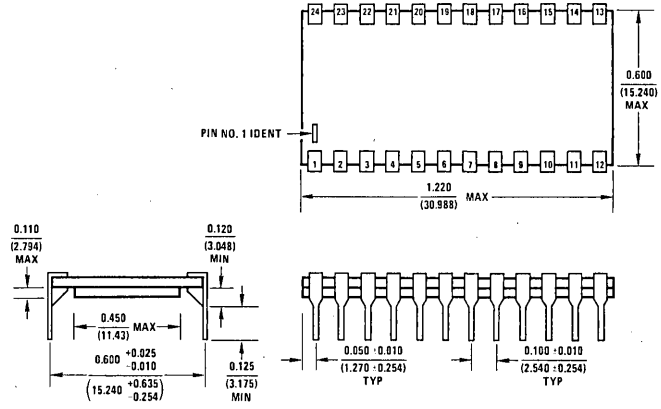




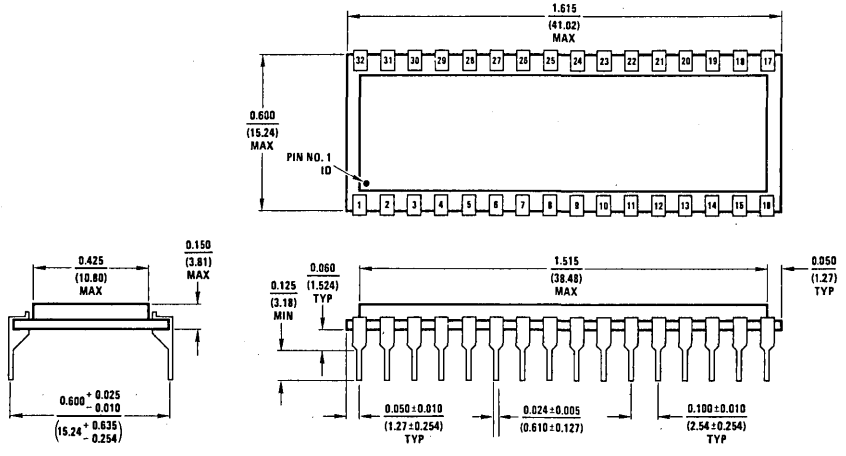
NS Package H12C
12-Lead TO-8 Metal Can Package (G)



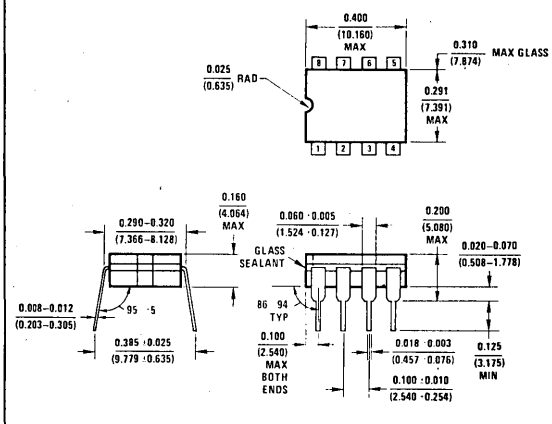
NS Package HY08A
8-Lead Cavity DIP (J) (Hybrid)



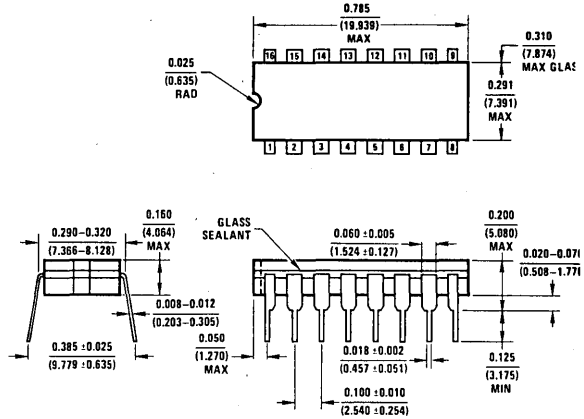
NS Package HY24A
24-Lead Cavity DIP (J)
(Hybrid Side Brazed)



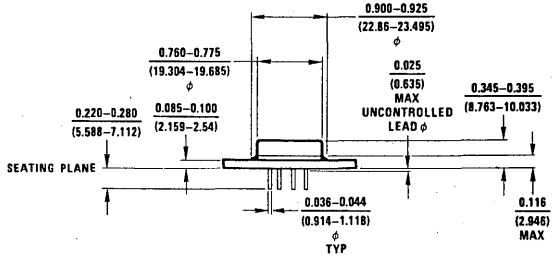
NS Package HY32A
32-Lead Cavity Dip (J)
(Hybrid)

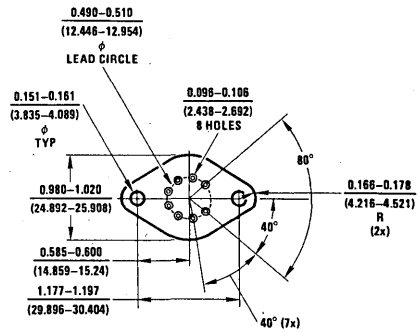


NS Package J08A
8-Lead Cavity Dual DIP (J)

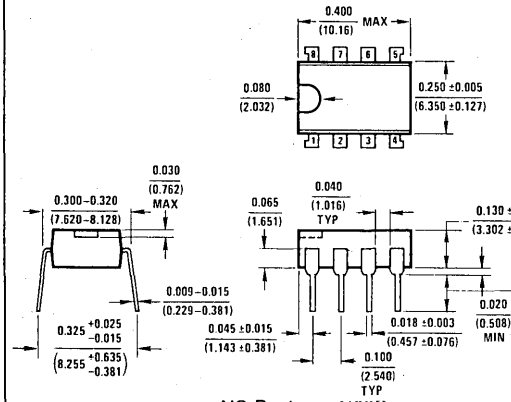


NS Package J16A
16-Lead Cavity DIP (J)

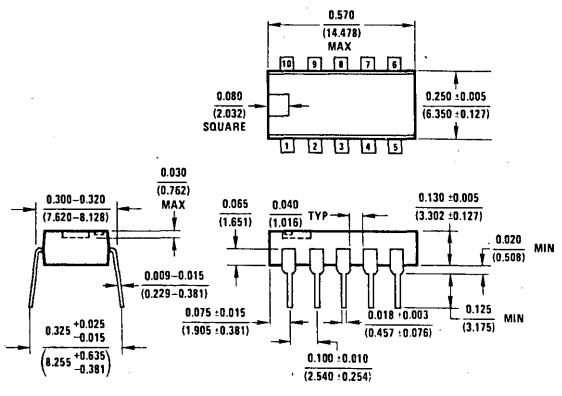




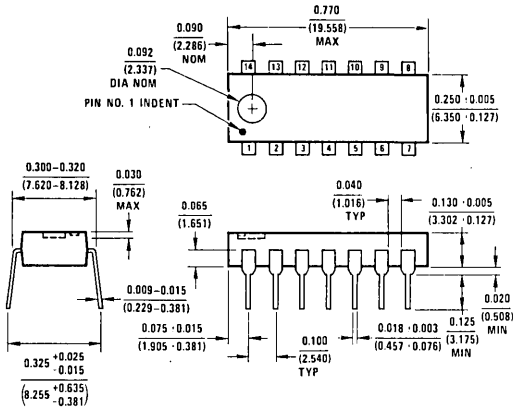
NS Package K08A
8-Lead TO-3 Metal Can Package (K)



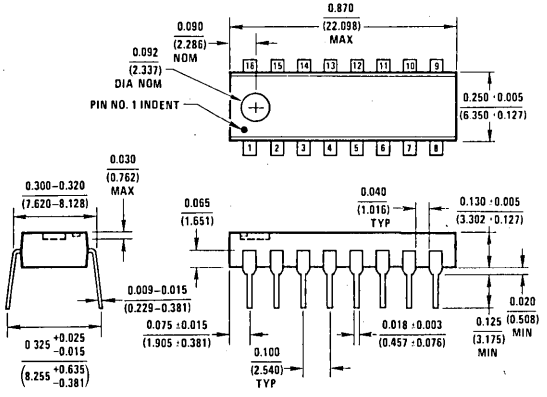
NS Package N08B
8-Lead Cavity Dual DIP (N)



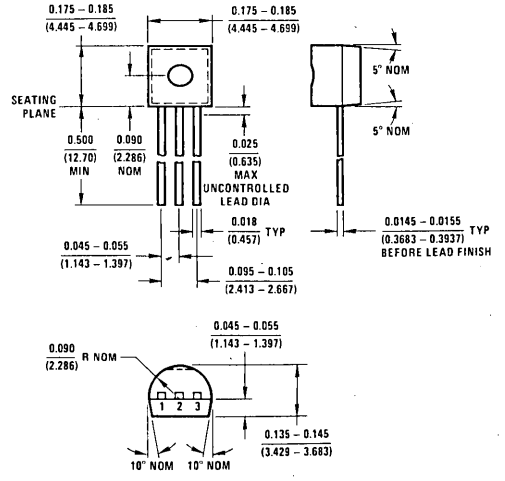
NS Package N10B
10-Lead Molded DIP (N)



NS Package N14A
14-Lead Molded DIP (N)



NS Package N16A
16-Lead DIP (N)



NS Package Z03A
3-Lead TO-92 Plastic Package (Z)

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Appendix III. Heat Sinks & Sockets

Following is a partial list of sockets and heat dissipators for use with various packages shown in this catalog. National assumes no responsibility for their quality or availability.

8-Lead TO-3 Hardware

SOCKETS
- Robinsor Nugent 0002011
- Azimuth 6028 (test socket)
- Wells 6010-20811

HEAT SINKS
- Thermalloy 6002-19
- IERC LAIC3B4CB
- IERC HP1-TO3-33CB (7 °C/W)

MICA WASHERS
- Keystone 4658
- Thermalloy

24-Pin DIP

SOCKETS
- Amphenol/Barnes 821-40012-244
- Robinson Nugent IC 246-S1 or S2

12-Lead TO-8 Hardware

SOCKETS
- Amphenol/Barnes 641-30031-121 (test socket)
  641-01061-121
- Robinson Nugent MP12100S or W
- Textool 212-100-323

HEAT SINKS
- Thermalloy 2240A (33 °C/W)
- Wakefield 215CB (30 °C/W)
- IERC UP-TO8-48CB (15 °C/W)

Amphenol/Barnes
2875 S. 25th Ave.
Broadview, IL 60153

Azimuth Electronics
2377 S. El Camino Real
San Clemente, CA 92672

IERC
135 W. Magnolia Bl.
Burbank, CA 91502

Keystone Electronics Corp.
49 Bleecker St.
New York, NY 10012

Robinson Nugent Inc.
800 E. 8th St.
New Albany, IN 47150

Thermalloy
P.O. Box 34829
Dallas, TX 75234
(214) 243-4321

Wakefield Engineering Inc.
Wakefield, MA 01880

Wells Electronics
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South Bend, IN 46613
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